Zynq Ultrascale+ Based SATA 3.0 Host Controller User Manual

Table of Content

List Of Figures

List Of Tables

1 Introduction

1.1 Purpose

The purpose of this document is to help the user understanding the testing of SATA 3.0 Host controller by using Zynq Ultrascale+ processor. It describes procedure to program and test the SATA 3.0 Host controller.

1.2 Overview

The document describes the Zynq Ultrascale+ environment and testing procedures on the Zynq Ultrascale+ Development Board. Zynq Ultrascale+ is used to accept user test cases to perform required operation and thereby provide required status.

2 Test setup and Testing Procedure

The below figure represents the test setup for the Zynq Ultrascle+ MPSoC Development Board with SATA FMC Daughter card and Intel SSD Device.

Figure 1: Test setup for SATA 3.0 Host Controller

2.1 SATA FMC Daught

Figure 2: SATA FMC Daughter Card.

2.2 Hardware Setup Requirements

- Zynq Ultrascale+ Development Kit
- JTAG Cable for Programming
- UART Cable for user console
- SATA HDD/SSD device
- SATA FMC Daughter Card

2.3 Software Requirements

- Vivado Design tool
- Tera Term

2.4 Programming the Board and Testing the Binaries Zynq Ultrascale+

- Make all the necessary connection as shown in Setup diagram
  - Connect the JTAG Cable to the slot for programming the bit stream.
  - Connect a SATA HDD/SDD Device to the slot.
  - Connect the UART Cable to the slot for user console.
  - When the connections are completed turn on the board.
- Open the Tera term tool for UART print to be displayed on console

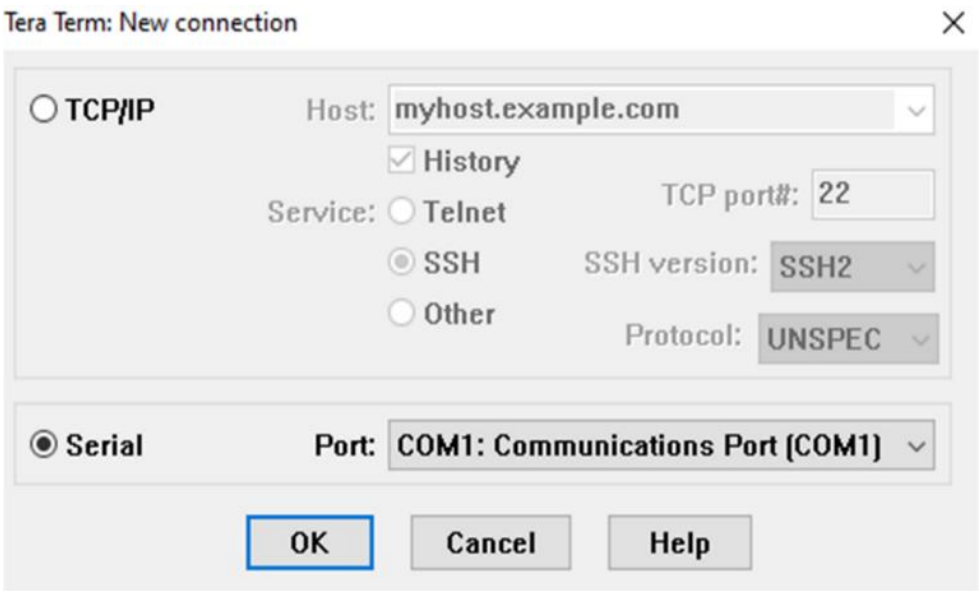

Figure 3: Baud Rate setup step 1

- Select the port **COM7- Silicon Labs Quad CP2108 USB to UART Bridge: Interface 0 (COM7)** then click ok,

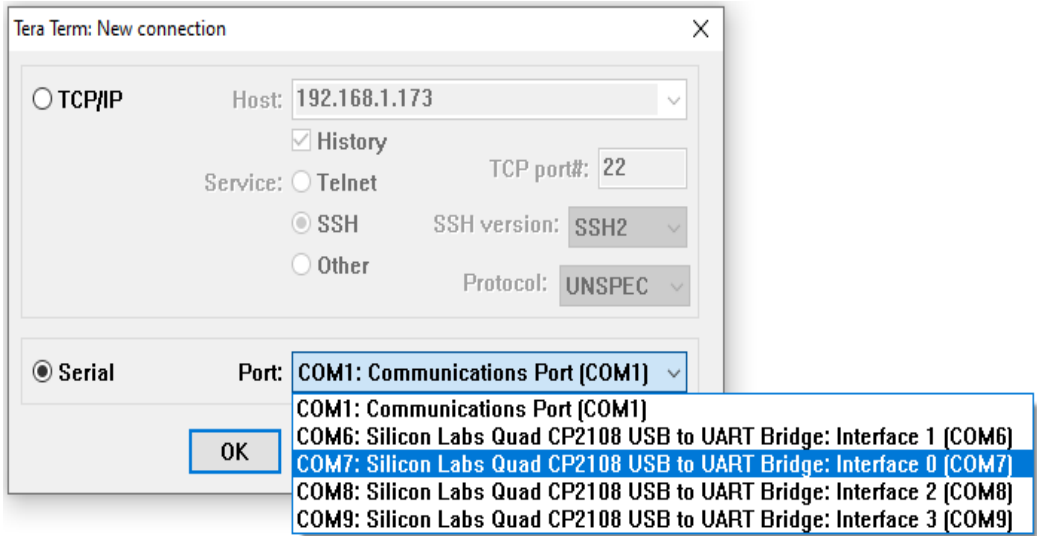

Figure 4: Baud Rate setup step 2

- After that set the Baud rate, In the Tera Term window click the **Setup** and open the **Serial port**

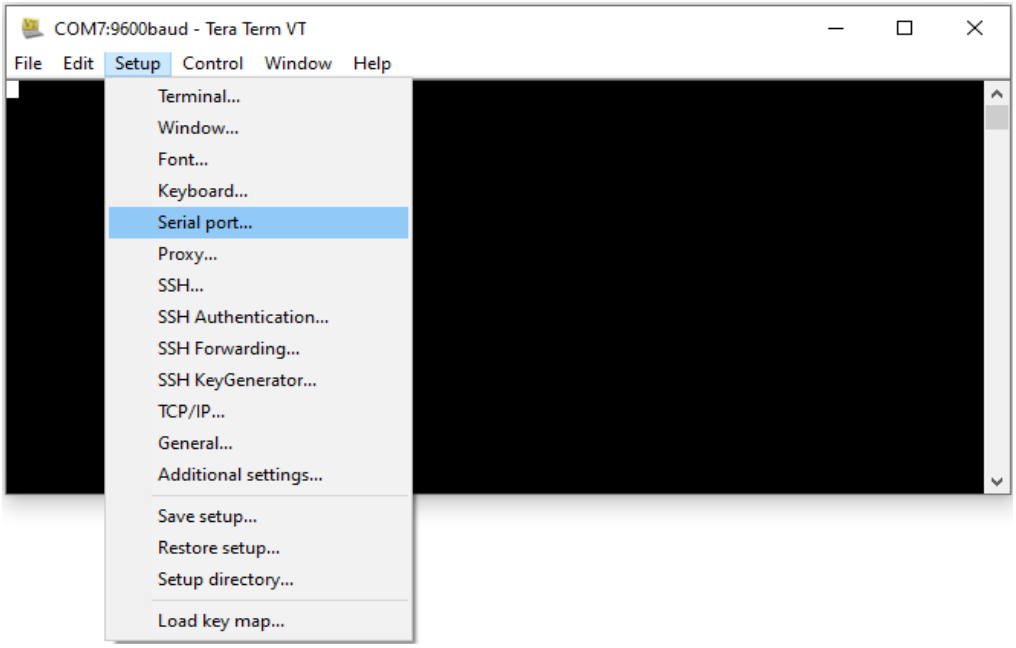

Figure 5: Baud Rate setup step 3

- And set the Baud rate value at **115200**.

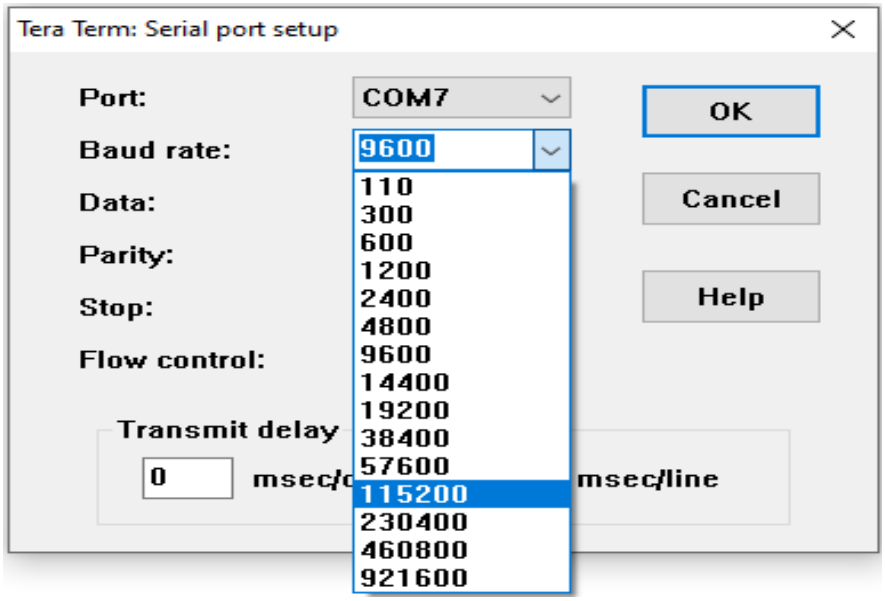

Figure 6: Baud Rate setup step 4

- Once the Baud rate was set then, Open the Vivado tool and then click **Open Hardware Manager** in the task GUI

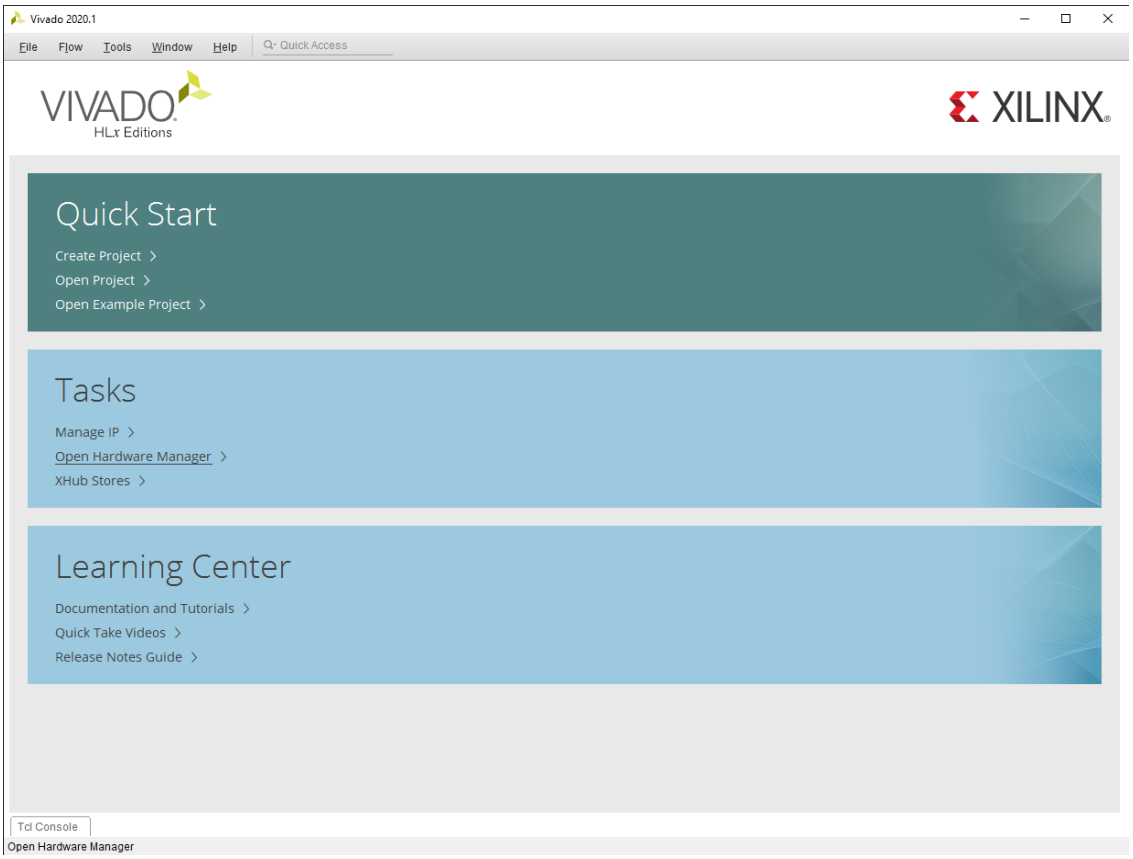

Figure 7: Programming step 1

- There will be a Green Bar on the tool as seen in Figure 26 then click **Open Target** then select the **Auto Connect**.

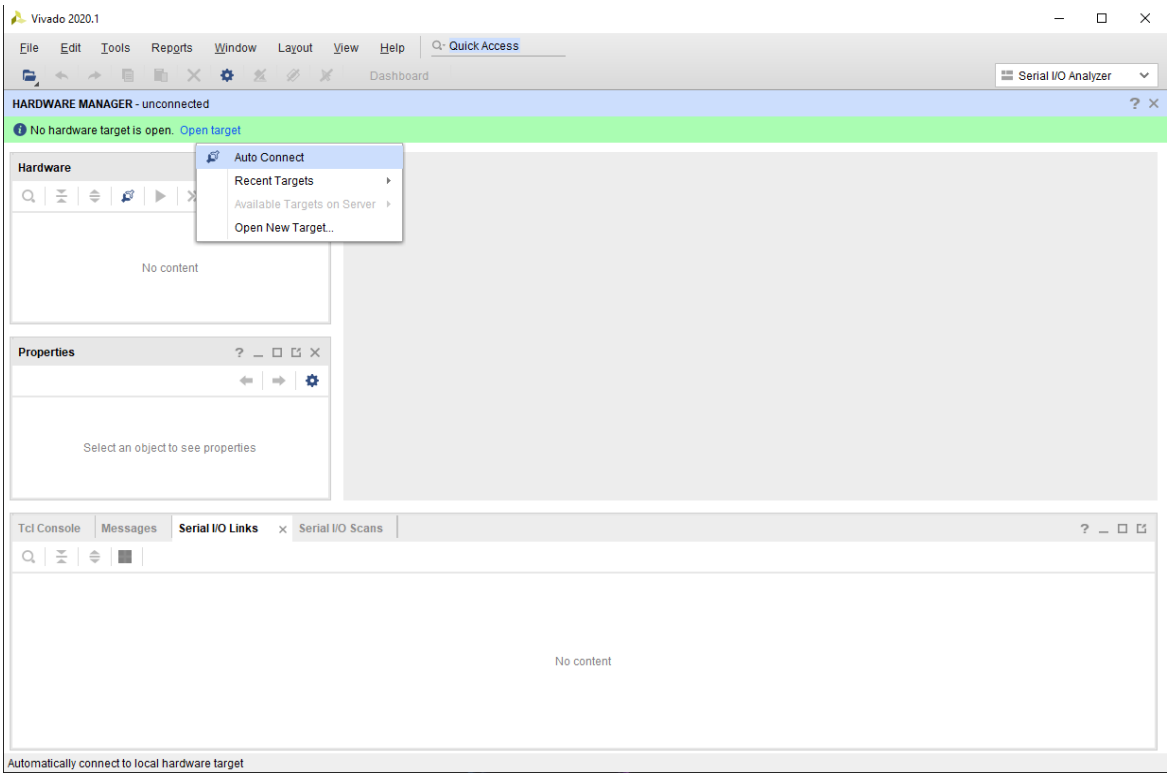

Figure 8: Programming step 2

- Then wait for the device to detect and then user can see on the Green bar there is 2 options now '**Program device**' and '**Refresh Device'.** User can click on the "Program device" on the Green Bar. Then the detected device will be shown in the figure 27. Right click on the detected device after click on Program device and wait for Program device tab to open.

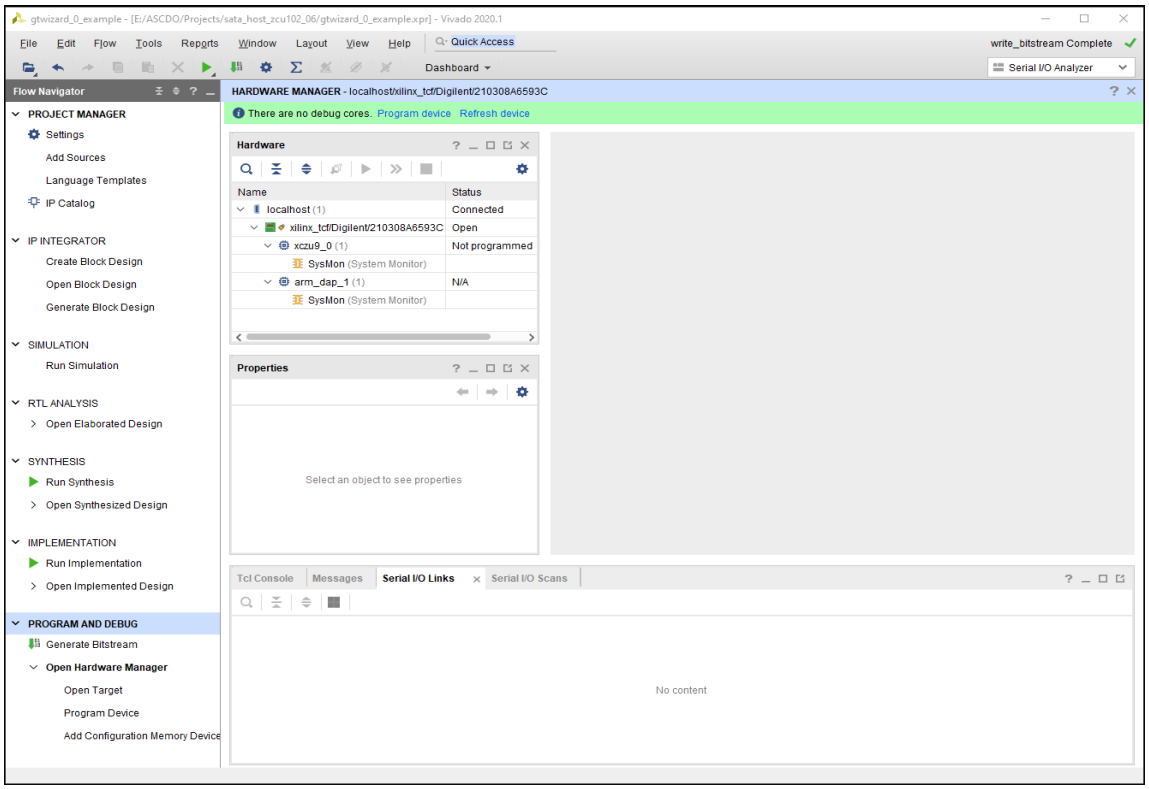

Figure 9: Programming step 3

- Once user gets the program device tab as shown in the Figure 28. User can see a “Bitstream file” required, So the binaries what have been downloaded or already have by the user sent from the iWave that particular path need to be given and browsed in order to get “sata_top.bit” file. After that click on Program.

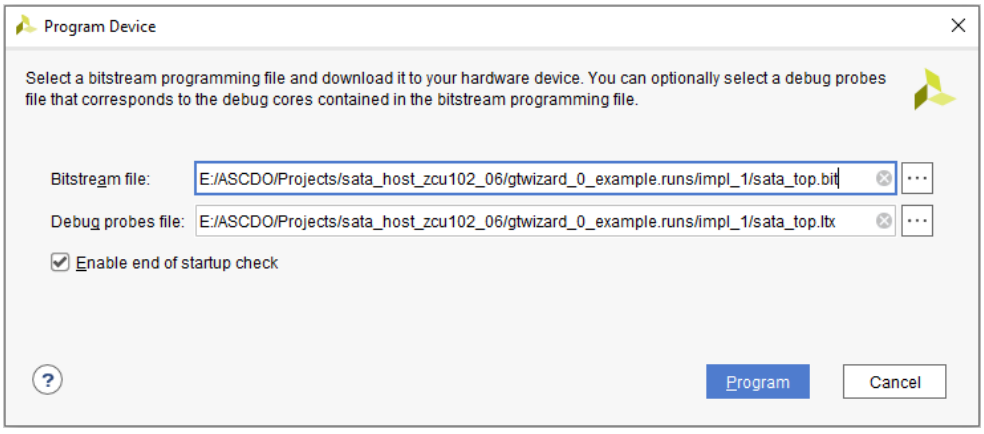

Figure 10: Programming step 4

- It will program the detected device and user can observe in Hardware tab the status of the device is programmed/not

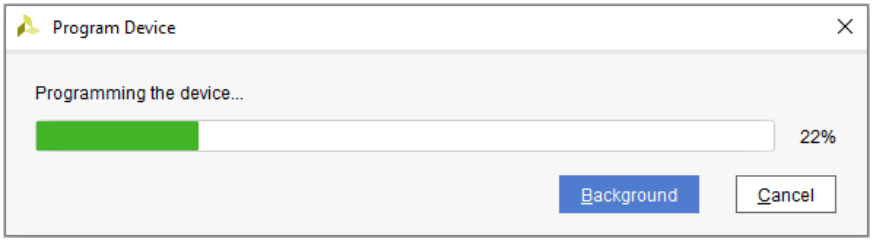

Figure 11: Programming step 5

- After programming, check the Tera Term as shown in Figure 30.

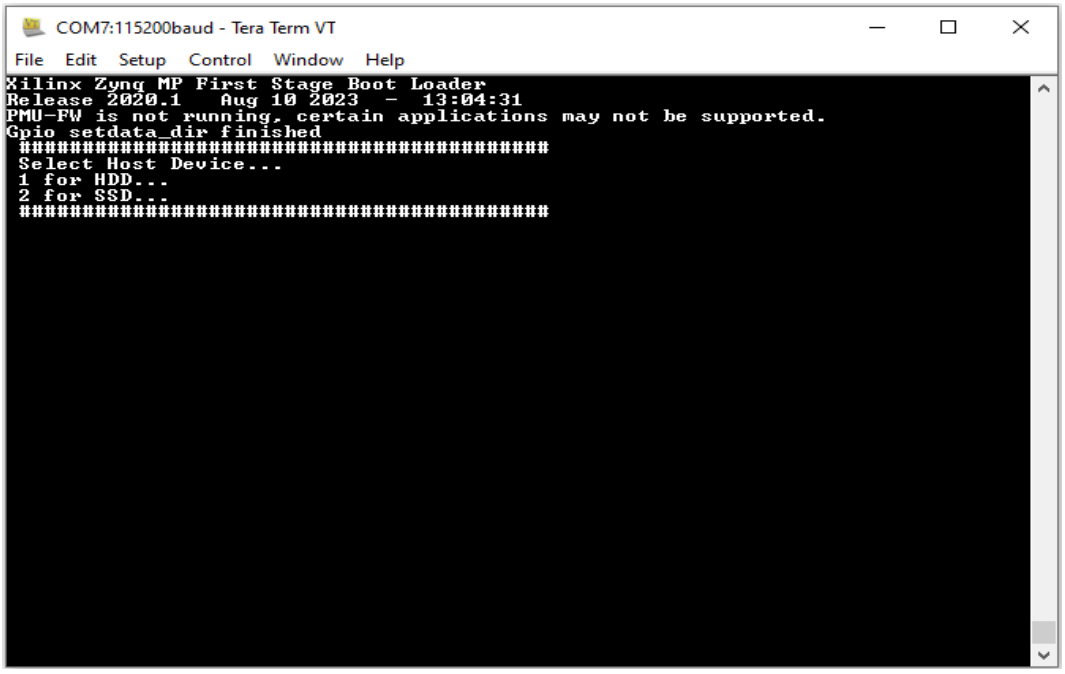

Figure 12: Test step 1

- Then choose which Device used in the test setup, For HDD press '**1**' and SDD press '**2**'.Then press '1' for Identify the device.

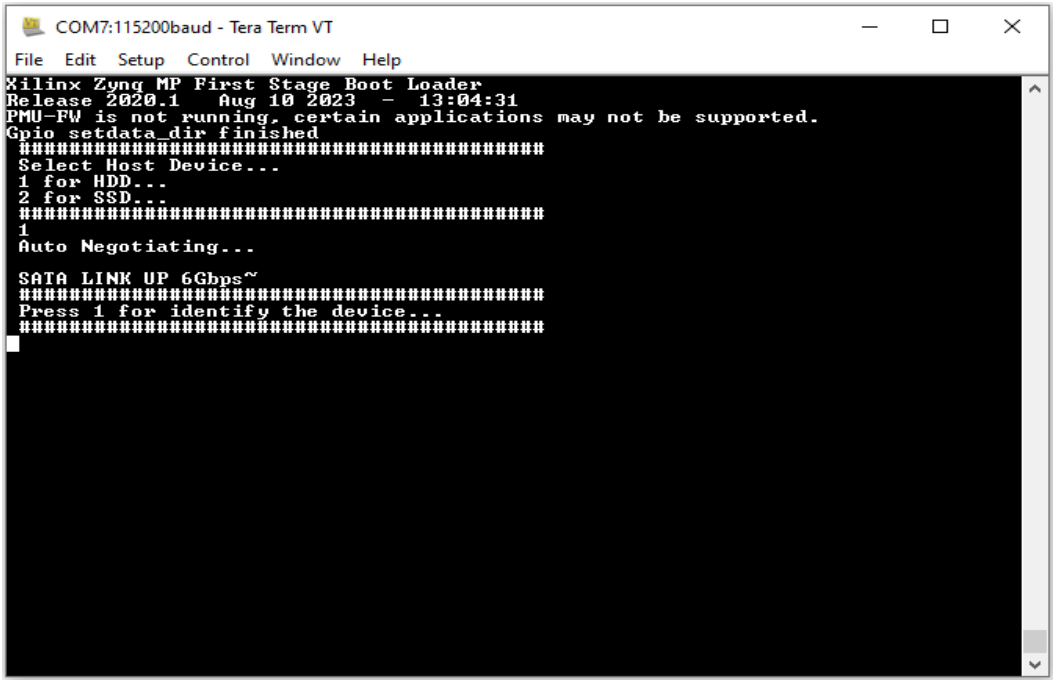

Figure 13: Test step 2

- Then the link speed and device information were displayed.

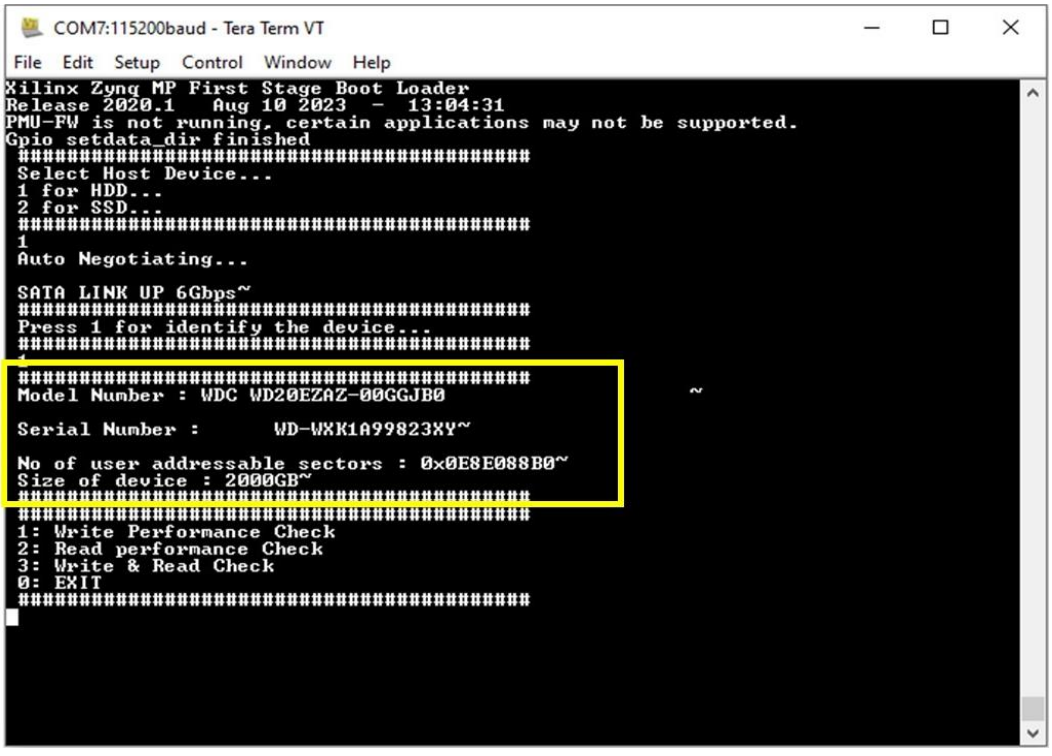

Figure 14: Test step 3

- For write performance, click **1** and press **Enter.** Then give it to the sector count and click “Enter”, afterwards given to the address and size of the data then the operation will be started. And the data will be shown in Figure 33.

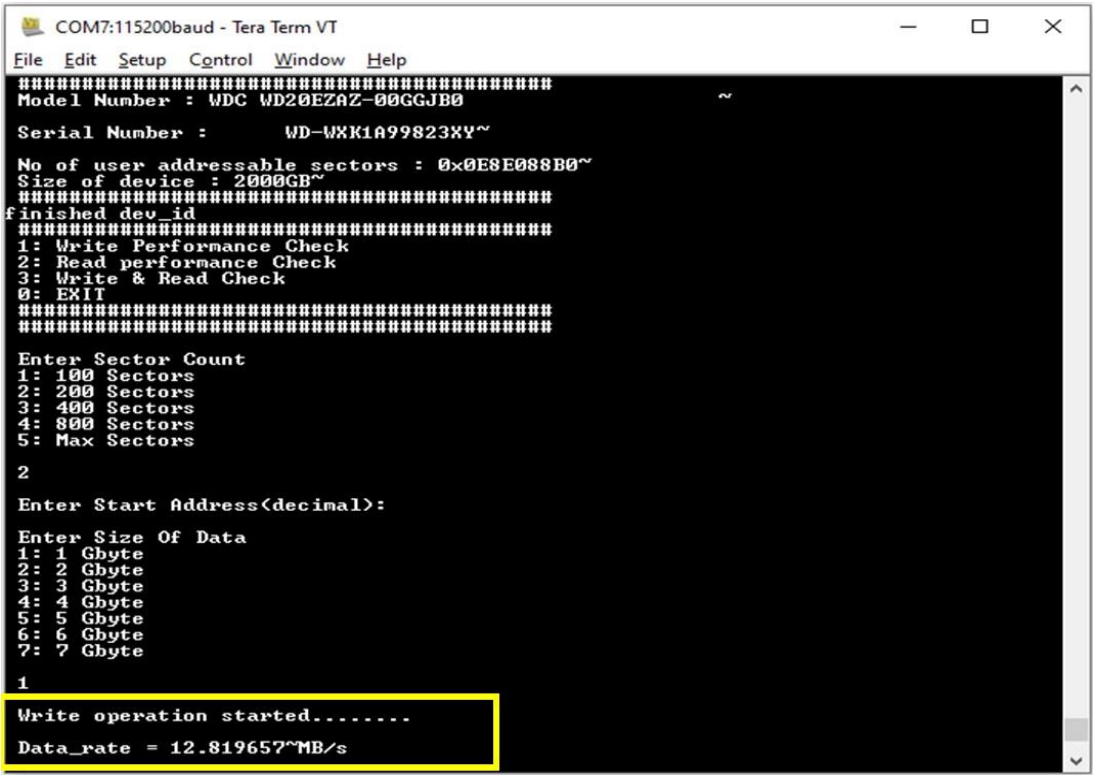

Figure 15: Test step 4

- For Read Performance, use **2** and press **Enter**. Procedure to check the Read performance as same as previous method.

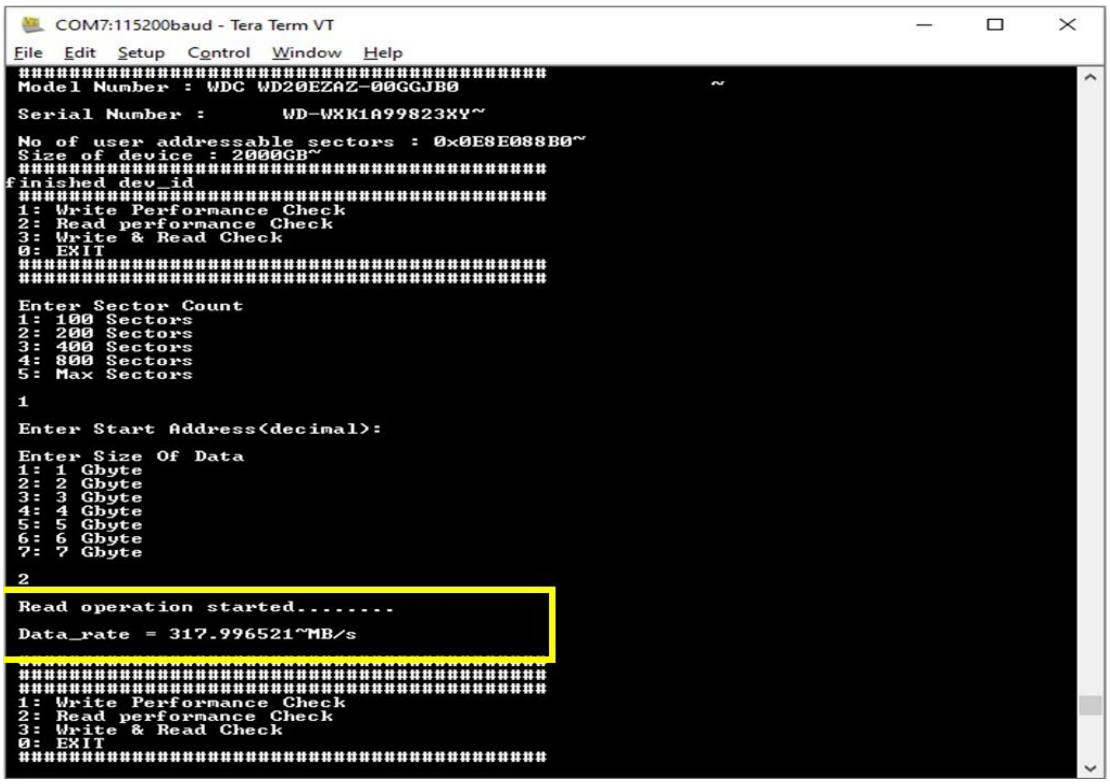

Figure 16: Test step 5

- For Read/Write Performance check, use **3**.

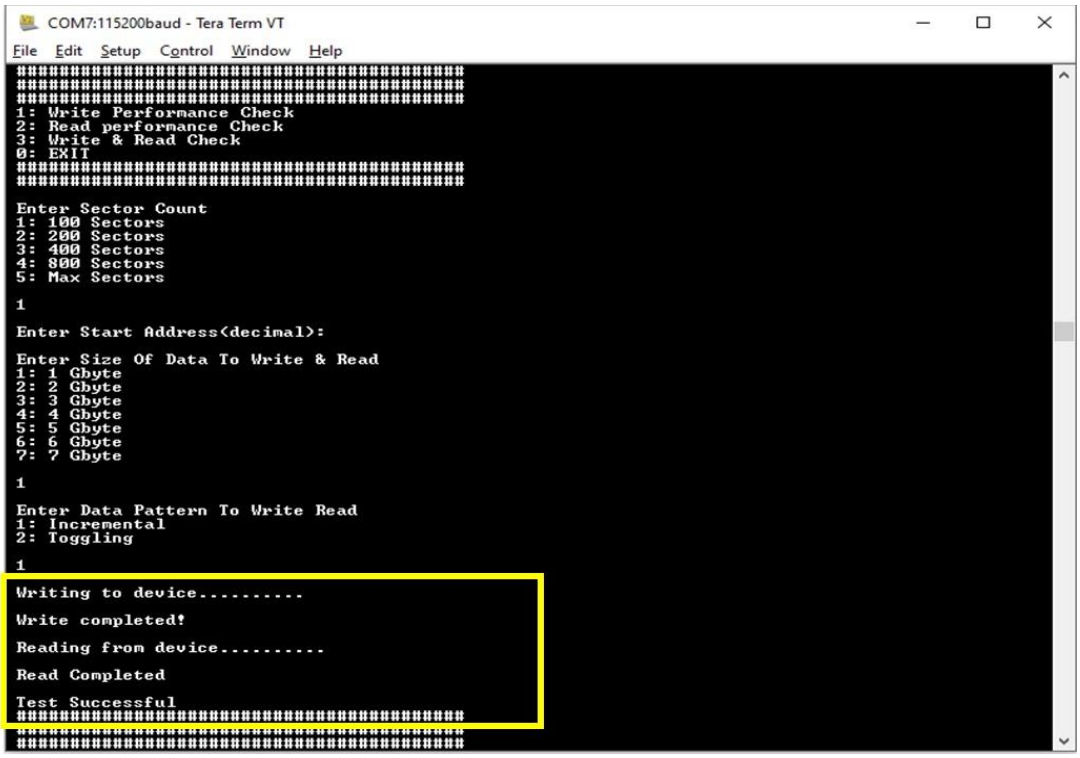

Figure 17: Test step 6

- Incase the user given the invalid input, it shows that as **Not a valid input.**

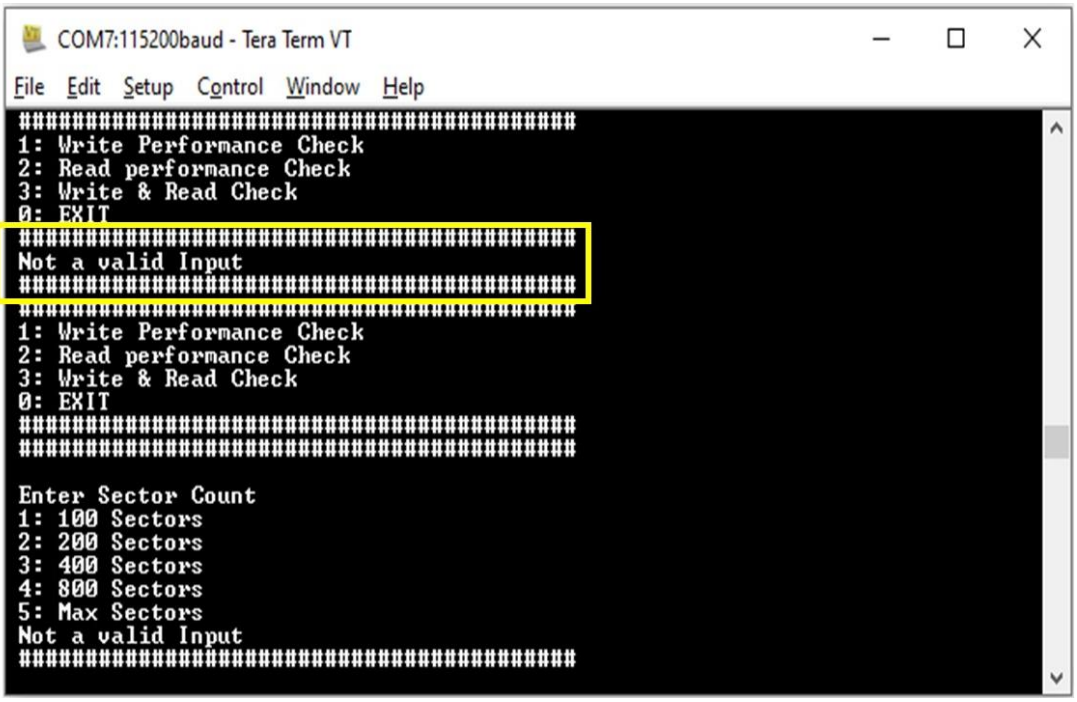

Figure 18: Test step 7

- For Exiting the test, use **0.**

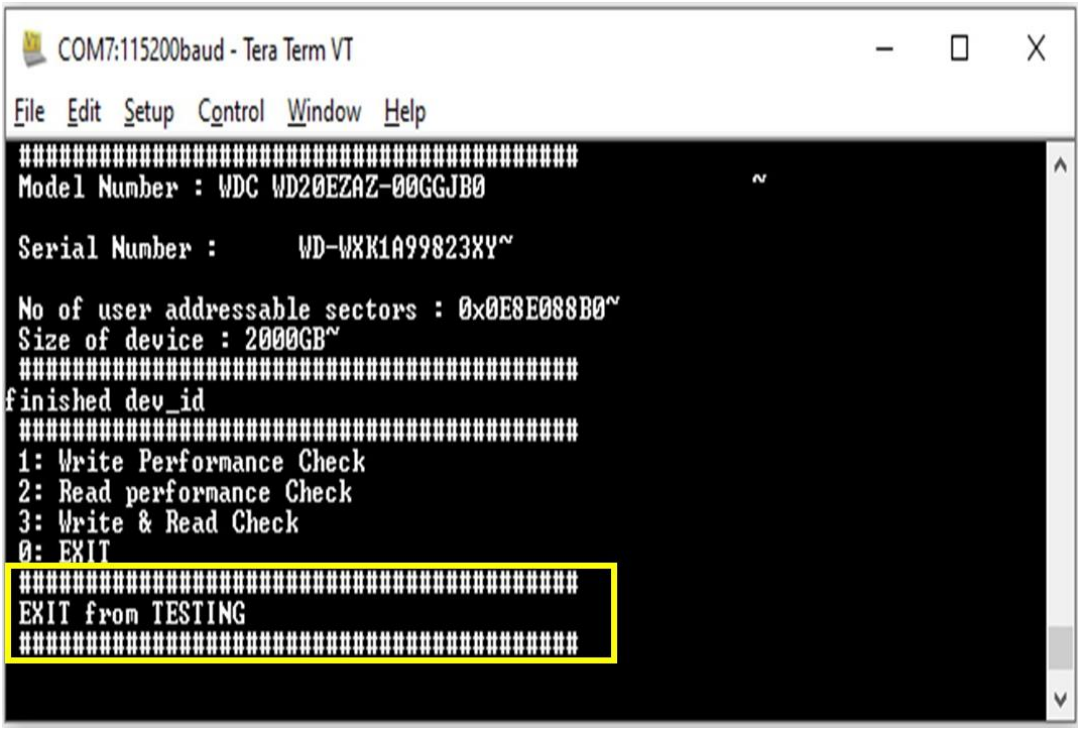

Figure 19: Test step 8

3 Resource Utilization

The table below shows the resource utilization summary for Zynq Ultrascale+ MPSoC development kit for SATA 3.0 Host Controller IP.

Table 1 :Resource Utilization for Zynq Ultrascale+ MPSoC development Kit device.

Resource	Utilization	Available
LUT	11592	274080
LUTRAM	1024	144000
FF	14222	548160
BRAM	26.50	912