iW-RainboW-G34D/G37D
i.MX 8M Mini or i.MX 8M Nano SODIMM
Development Platform
Hardware User Guide
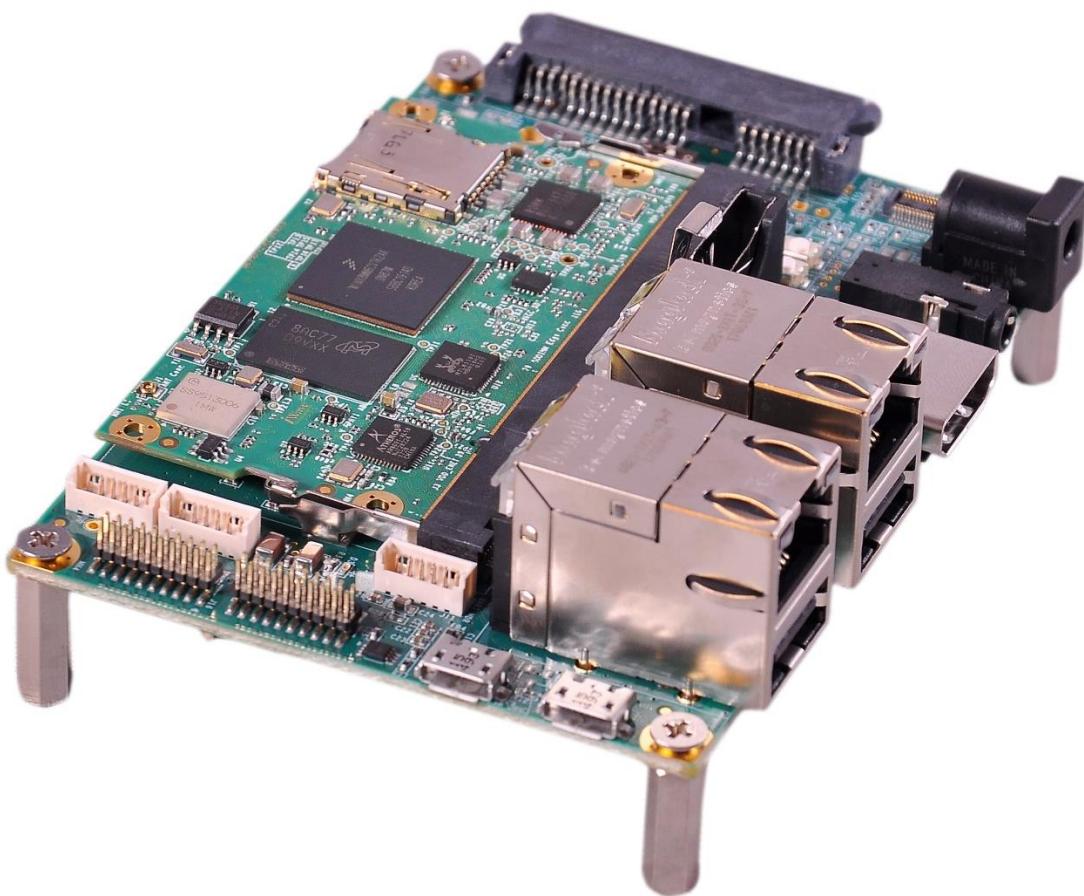
iWave
Embedding Intelligence

Document Revision History

Document Number	iW-PREVD-UM-01-R2.1-REL1.1-i.MX 8M Mini-Nano_DevKit	
Revision	Date	Change Description
1.0	20th Nov 2019	Initial Release Version
1.1	01st July 2022	Removed SODIMM MIPI Daughter Board information

Disclaimer

iWave Systems reserves the right to change details in this publication including but not limited to any Product specification without notice.

No warranty of accuracy is given concerning the contents of the information contained in this publication. To the extent permitted by law no liability (including liability to any person by reason of negligence) will be accepted by iWave Systems, its subsidiaries or employees for any direct or indirect loss or damage caused by omissions from or inaccuracies in this document.

SOC and other major components used in this product may have several silicon errata associated with it. Under no circumstances, iWave Systems shall be liable for the silicon errata and associated issues.

Trademarks

All registered trademarks, product names mentioned in this publication are the property of their respective owners and used for identification purposes only.

Certification

iWave Systems Technologies Pvt. Ltd. is an ISO 9001:2015 Certified Company.

Warranty & RMA

Warranty support for Hardware: 1 Year from iWave or iWave's EMS partner.

For warranty terms, go through the below web link,

http://www.iwavesystems.com/support/warranty.html

For Return Merchandise Authorization (RMA), go through the below web link,

http://www.iwavesystems.com/support/rma.html

Technical Support

iWave Systems technical support team is committed to provide the best possible support for our customers so that our Hardware and Software can be easily migrated and used.

For assistance, contact our Technical Support team at,

Email	: support.ip@iwavesystems.com
Website	: www.iwavesystems.com
Address	: iWave Systems Technologies Pvt. Ltd.
	# 7/B, 29th Main, BTM Layout 2nd Stage,
	Bengaluru, Karnataka,
	India – 560076

Table of Contents

List of Figures

List of Tables

1. INTRODUCTION

1.1 Purpose

The i.MX 8M Mini or i.MX 8M Nano SODIMM development platform incorporates i.MX 8M Mini or i.MX 8M Nano SOC based SODIMM SOM and SODIMM Carrier board for complete validation of i.MX 8M Mini or i.MX 8M Nano SOC functionality. This document is the hardware user guide for the i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board. This guide provides detailed information on the overall design and usage of the SODIMM carrier board from a hardware system perspective. The details about the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM hardware is explained in i.MX 8M Mini or i.MX 8M Nano SOM user manual document "iW-RainboW-G34M_G37M-i.MX_8M_Mini_Nano-SODIMM-SOM-HardwareUserGuide-R1.0-REL1.x.pdf".

1.2 Overview

The SODIMM is a versatile small form factor computer Module targeting applications that require low power, low cost and high performance.

iW-RainboW-G34D Development Platform comes with SODIMM Carrier board and i.MX 8M Mini or i.MX 8M Nano based SODIMM SOM. The development board can be used for quick prototyping of various applications targeted by the i.MX 8M Mini or i.MX 8M Nano processor. With the 100mmx720mm Pico ITX size, SODIMM carrier board is highly packed with all the necessary on-board connectors to validate the features of i.MX 8M Mini or i.MX 8M Nano SODIMM SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
Hz	Hertz
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound

Acronyms	Abbreviations
IC	Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signalling
Mbps	Megabits per sec
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
NC	Not Connected
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PWM	Pulse Width Modulation
ROHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SDIO	Secure Digital Input Output
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4   Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
MIPI	Mobile Industry Processor Interface signals
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.5   References

- IMX8MMIEC_Rev_x.pdf
- IMX8MNIEC_Rev_x.pdf

2. ARCHITECTURE AND DESIGN-SODIMM CARRIER BOARD

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano SODIMM development platform carrier board features with high level block diagram and detailed information about each block.

2.1 i.MX 8M Mini or i.MX 8M Nano SODIMM Development Platform Block Diagram

Note:
1.IMX 8M Mini PCIe interface is shared with Mini PCIe Connector and on-SOM PCIe to Ethernet PHY. By default Mini PCIe is supported and RJ45 Mag Jack2 is Optional.
2.Not available in Nano.
*Optional

mktg@iwavesystems.com   iWave Systems Technologies Pvt. Ltd.
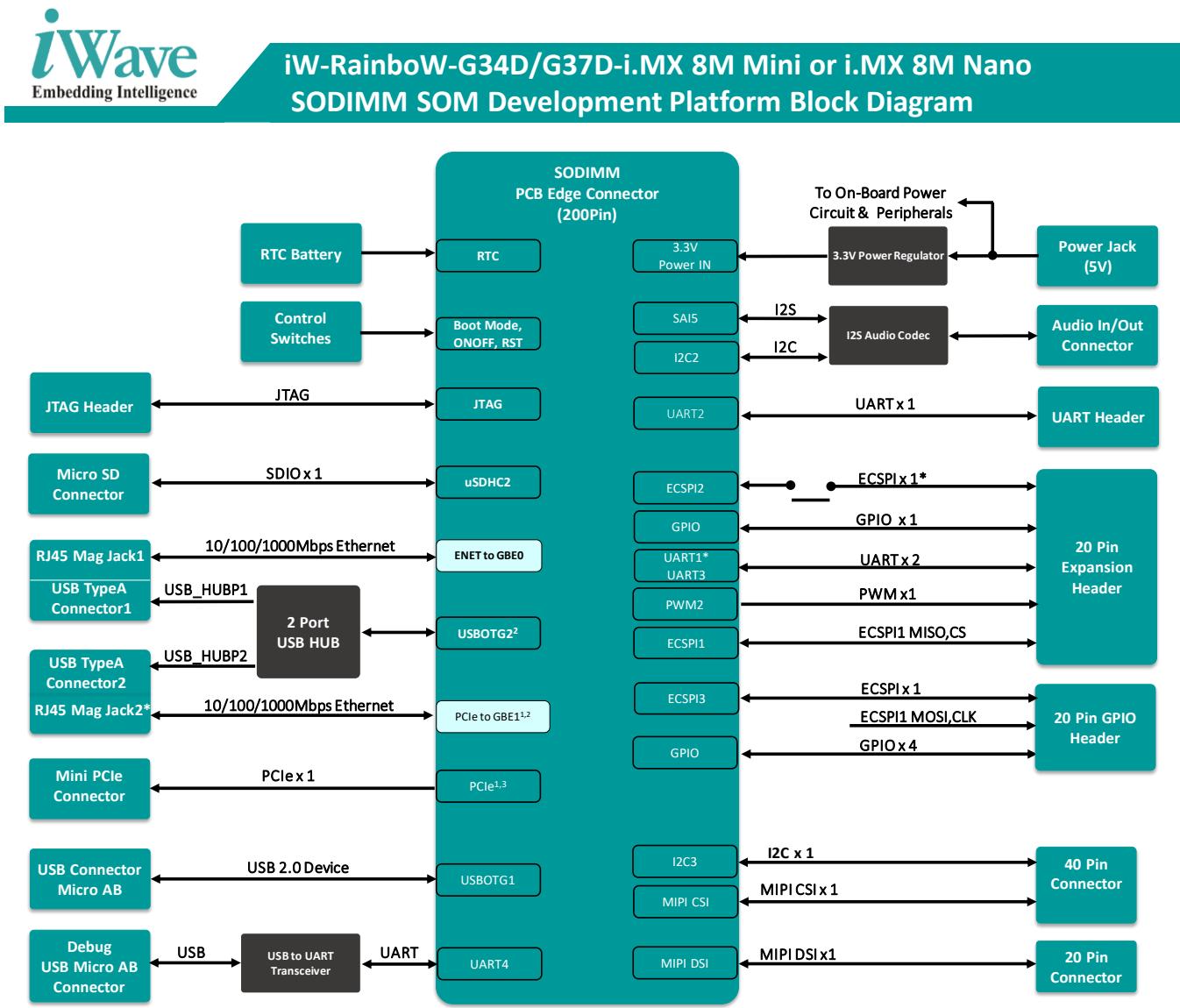
Figure 1: i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Development Platform Block Diagram

2.2   i.MX 8M Mini or i.MX 8M Nano SODIMM Development Platform Features

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier board supports the following features to support various interfaces from i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Edge connector

Serial Interface Features

- Debug UART through USB Micro AB Connector
- DATA UART x 1 Port through Header

Communication Features

- 10/100/1000 Mbps Ethernet through RJ45MagJack-1
- 10/100/1000 Mbps PCIe to Ethernet PHY through RJ45MagJack-2 (Optional) (Not available in Nano)[1]
- USB 2.0 OTG as a device x 1 Port through Micro AB Connector
- USB 2.0 Host x 2 Ports through USB Type-A Connector (Not available in Nano)
- SD x 1 Port through Micro SD Connector

High Speed Interfaces

- Mini PCIe x 1 Port (Not available in Nano)[1]

Audio/Video Features

- I2S Audio Codec with 3.5mm Audio IN/OUT jack

Additional Features

- MIPI CSI FPC Connector (40Pin)
- MIPI DSI Connector (20Pin)
- Boot Mode Switch
- Reset Switch
- Power On/off Switch
- 20-Pin JTAG Connector
- RTC Coin Cell Holder

20Pin Expansion Header

- Data UART x 2 Port[2] (One is Optional)
- PWM x 1 Port
- ECSPI x 2 Port (One is Optional)

20Pin GPIO Header

- ECSPI x 1
- GPIOs

General Specification

- Power Supply   : 5V,2.5A Power Input Jack

- Form Factor   : 100mm X 72m Pico ITX

[1] *i.MX 8M Mini SOC's PCIe interface, by default is connected to Mini PCIe Port of the Development board and is optionally connected to On-SOM PCIe to Ethernet PHY controller.*

[2] *UART1 is optionally connected to On-SOM Wifi module through resistor and by default not populated, if On SOM Wifi module is used, UART1 interface cannot be supported in 20Pin Expansion Connector of SODIMM carrier card.*

2.3 SODIMM Edge Connector

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier board supports 200 Pin SODIMM Edge mating connector for SODIMM SOM attachment. This standard 200-pin robust connector is capable of handling high-speed signals and can be used for size constrained embedded applications. This SODIMM Edge mating connector (J14) is physically located at the top of the board as shown below.
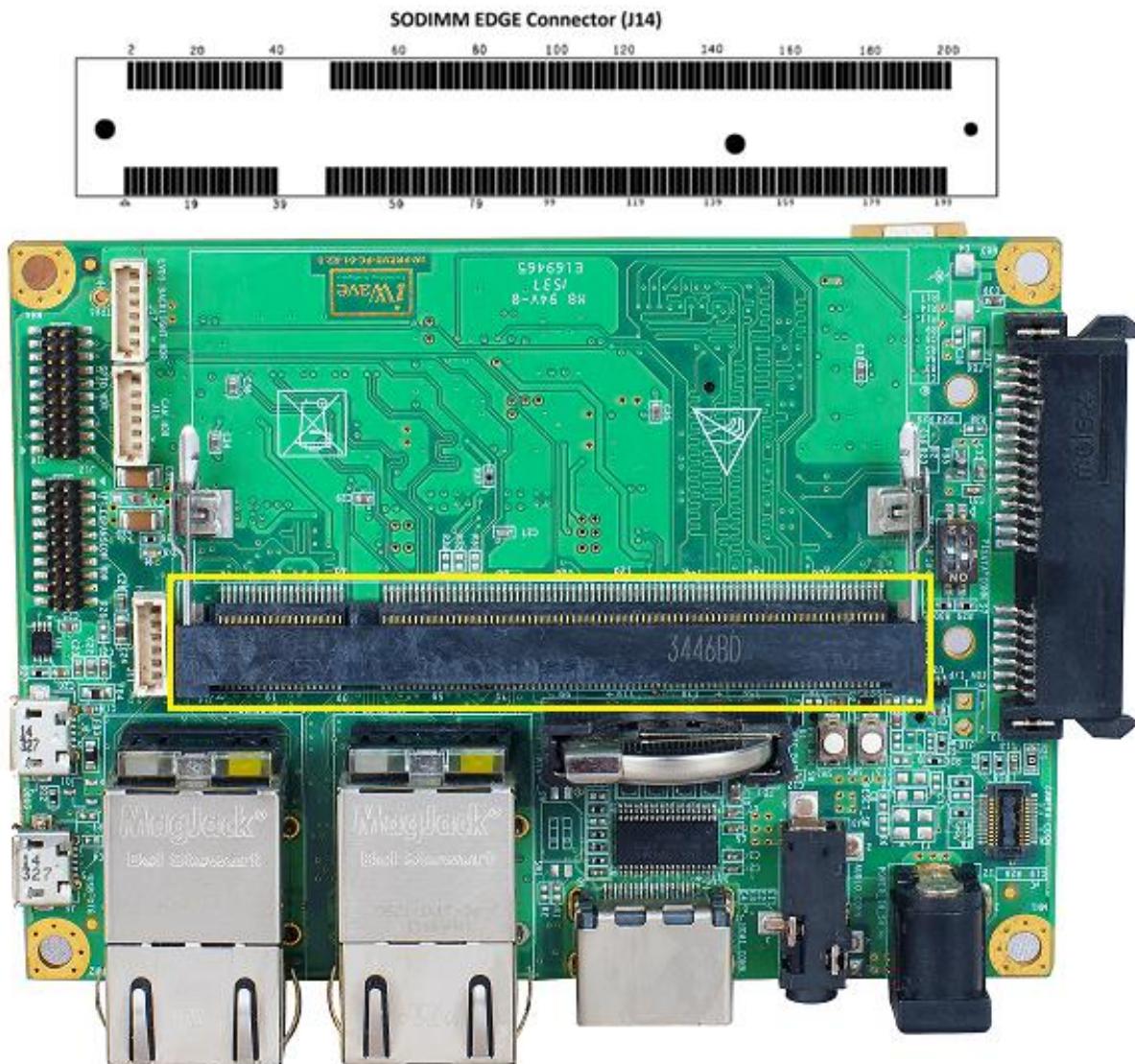
Figure 2: SODIMM Connector

Table 3: 200-Pin PCB Edge Connector Pin Assignment

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	NA	Power	Ground.
2	GPHY1_ATXRXM	NA	IO, DIFF	Gigabit Ethernet differential pair 1 negative.
3	VDVDH_GPHY1*	NA	O, Power	Power for Centre Tap. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
4	GPHY1_ATXRXP	NA	IO, DIFF	Gigabit Ethernet differential pair 1 positive.
5	GND	NA	Power	Ground.
6	GPHY1_BTXRXM	NA	IO, DIFF	Gigabit Ethernet differential pair 2 negative
7	UART3_RXD	UART3_RXD/E18	I, 3.3V CMOS	UART3 serial data receiver.
8	GPHY1_BTXRXP	NA	IO, DIFF	Gigabit Ethernet differential pair 2 positive.
9	UART3_TXD	UART3_TXD/D18	O, 3.3V CMOS	UART3 serial data transmitter.
10	NC	NA	-	NC.
11	GPHY1_LINK_LED2	NA	O, 2.5V CMOS	Ethernet link status LED.
12	GPHY1_ACTIVITY_LED1	NA	O, 2.5V CMOS	Ethernet Activity status LED.
13	GND	NA	Power	Ground.
14	GPHY1_CTXRXM	NA	IO, DIFF	Gigabit Ethernet differential pair 3 negative.
15	GPHY1_DTXRXM	NA	IO, DIFF	Gigabit Ethernet differential pair 4 negative
16	GPHY1_CTXRXP	NA	IO, DIFF	Gigabit Ethernet differential pair 3 positive.
17	GPHY1_DTXRXP	NA	IO, DIFF	Gigabit Ethernet differential pair 4 positive.
18	I2C3_SCL*	I2C3_SCL/E10	O, 3.3V OD/4.7K PU	I2C3 Clock signal. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
19	I2C3_SDA*	I2C3_SDA/F10	IO, 3.3V OD/4.7K PU	I2C3 Data signal. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
20	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
21	NC	NA	NA	NC.
22	NC	NA	NA	NC.
23	NC	NA	NA	NC.
24	NC	NA	NA	NC.
25	NC	NA	NA	NC.
26	NC	NA	NA	NC.
27	GND	NA	Power	Ground.
28	NC	NA	NA	NC.
29	NC	NA	NA	NC.
30	GPHY2_ACTIVITY_LED1 (NC in Nano) *	NA	O, 3.3V CMOS	Second Ethernet Activity status LED. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
31	NC	NA	NA	NC.
32	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
33	GPHY2_LINK_LED2 (NC in Nano) *	NA	O, 3.3V CMOS	Second Ethernet link status LED. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
34	GPHY2_ATXRXM (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 1 negative. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
35	GPHY2_BTXRXM (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 2 negative. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
36	GPHY2_ATXRXP (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 1 positive. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
37	GPHY2_BTXRXP (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 2 positive. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
38	UART2_CTS_B(SAI3_RXC)	SAI3_RXC/AG7	O, 3.3V CMOS	UART2 Clear to Send.
39	USB2_OTG_OC(GPIO1_15)	GPIO1_IO15/AB9	I, 3.3V CMOS	Over current sense for USB2 Host Port.
40	GND	NA	Power	Ground.
41	GND	NA	Power	Ground.
42	GPHY2_CTXRXM (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 3 negative. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
43	GPHY2_DTXRXM (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 4 negative. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
44	GPHY2_CTXRXP (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 3 positive. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
45	GPHY2_DTXRXP (NC in Nano) *	NA	IO, DIFF	Second Gigabit Ethernet differential pair 4 positive. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
46	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
47	SAI1_RXD0 (NC in Nano)	SAI1_RXD0/AG15	I, 3.3V CMOS/ 4.7K PU	SAI1 Receiver Data 0. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
48	MIPI_DSI_DATA0_N	MIPI_DSI_D0_N/ A9	O, MIPI	MIPI DSI differential data lane0 negative.
49	VDVDH_GPHY2 (NC in Nano) *	NA	NC	NC. *This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
50	MIPI_DSI_DATA0_P	MIPI_DSI_D0_P/B9	O, MIPI	MIPI DSI differential data lane0 positive.
51	GND	NA	Power	Ground.
52	MIPI_DSI_DATA1_N	MIPI_DSI_D1_N/ A10	O, MIPI	MIPI DSI differential data lane1 negative.
53	MIPI_DSI_DATA2_N	MIPI_DSI_D2_N/ A12	O, MIPI	MIPI DSI differential data lane2 negative.
54	MIPI_DSI_DATA1_P	MIPI_DSI_D1_P/B10	O, MIPI	MIPI DSI differential data lane1 positive.
55	MIPI_DSI_DATA2_P	MIPI_DSI_D2_P/B12	O, MIPI	MIPI DSI differential data lane2 positive.
56	MIPI_DSI_DATA3_N	MIPI_DSI_D3_N/ A13	O, MIPI	MIPI DSI differential data lane3 negative.
57	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N/ A11	O, MIPI	MIPI DSI differential Clock negative.
58	MIPI_DSI_DATA3_P	MIPI_DSI_D3_P/B13	O, MIPI	MIPI DSI differential data lane3 positive.
59	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P/ B11	O, MIPI	MIPI DSI differential Clock positive.
60	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
61	SAI5_RX_DATA0(SAI5_RXD0)	SAI5_RXD0/AD18	I, 3.3V CMOS	SAI5 Receive Data Lane 0.
62	ECSPI2_SS0	ECSPI2_SS0/A6	O, 3.3V CMOS	SPI2 Chip select signal.
63	ECSPI2_MISO	ECSPI2_MISO/A8	I, 3.3V CMOS	SPI2 Master Input Slave Output.
64	GPIO_CLK(SAI5_MCLK)	SAI5_MCLK/AD15	O, 3.3V CMOS	Master Clock for Audio codec.
65	GND	NA	Power	Ground.
66	ECSPI2_SCLK	ECSPI2_SCLK/E6	O, 3.3V CMOS	SPI2 clock signal.

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
67	SAI5_TX_DATA0(SAI5_RXD3)	SAI5_RXD3/AC13	O, 3.3V CMOS	SAI5 Transmit Data Lane 0.
68	SAI1_RXD2 (NC in Nano)	SAI1_RXD2/AG17	I, 3.3V CMOS 100k PD	SAI1 Receiver Data 2. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
69	NC	NA	NA	NC.
70	ECSPI2_MOSI	ECSPI2_MOSI/B8	O, 3.3V CMOS	SPI2 Master Output Slave Input.
71	GPIO1_6	GPIO1_IO06/AG11	IO, 3.3V CMOS	General Purpose Input Output.
72	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
73	GPIO1_7	GPIO1_IO07/AF11	IO, 3.3V CMOS	General Purpose Input Output.
74	SAI1_RXC (NC in Nano)	SAI1_RXC/AF16	I, 3.3V CMOS	SAI1 Receiver Clock Input. *Note: This signal is by default configured as General-Purpose Input Output.*
75	UART2_RTS_B(SAI3_RXD)	SAI3_RXD/AF7	I, 3.3V CMOS	UART2 Request to Send.
76	USB1_OTG_OC(GPIO1_13)	GPIO1_IO13/AD9	I, 3.3V CMOS	USB1 OTG port Over current sense.
77	USB1_ID	USB1_ID/D22	I, 3.3V CMOS	USB1 OTG ID to identify Host & Device.
78	USB1_OTG_PWR(GPIO1_12)	GPIO1_IO12/AB10	O, 3.3V CMOS	USB OTG1 Power enable GPIO
79	GND	NA	Power	Ground.
80	ECSPI1_SCLK	ECSPI1_SCLK/D6	O, 3.3V CMOS	SPI1 clock signal.
81	USB1_DP	USB1_DP/B22	IO, USB	USB1 2.0 OTG High Speed Data Positive.
82	CLKOUT1	CLKOUT1/ H26	O, 3.3V CMOS	Clock OUT1 from SOC
83	USB1_DN	USB1_DN/A22	IO, USB	USB1 2.0 OTG High Speed Data Negative.
84	CLKOUT2	CLKOUT2/J26	O, 3.3V CMOS	Clock OUT2 from SOC
85	CLKIN1	CLKIN1/ H27	I, 3.3V CMOS	Clock IN1 to SOC
86	NC	NA	NA	NC.
87	CLKIN2	CLKIN2/ J27	I, 3.3V CMOS	Clock IN2 to SOC
88	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
89	SAI5_TX_SYNC(SAI5_RXD1)	SAI5_RXD1/AC14	O, 3.3V CMOS	SAI5 Transmitter Frame Sync
90	SAI5_TX_BCLK(SAI5_RXD2)	SAI5_RXD2/AD13	O, 3.3V CMOS	SAI5 Transmitter Bit Clock
91	SAI5_RX_BCLK(SAI5_RXC)	SAI5_RXC/AC15	I, 3.3V CMOS	SAI5 Receiver Bit Clock.

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
				Note: This signal is by default configured as General-Purpose Input Output.
92	SAI5_RX_SYNC(SAI5_RXFS)	SAI5_RXFS/AB15	I, 3.3V CMOS	SAI5 Receiver Frame Sync. *Note: This signal is by default configured as General-Purpose Input Output.*
93	NC	NA	NA	NC.
94	ECSPI1_MISO	ECSPI1_MISO/A7	I, 3.3V CMOS	SPI1 Master Input Slave Output.
95	GND	NA	Power	Ground.
96	ECSPI1_MOSI	ECSPI1_MOSI/B7	O, 3.3V CMOS	SPI1 Master Output Slave Input.
97	ECSPI1_SS0	ECSPI1_SS0/B6	O, 3.3V CMOS	SPI1 Chip select signal.
98	UART1_TXD*	SAI2_RXFS/AC19	O, 3.3V CMOS	UART1 serial data transmitter. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
99	UART1_RXD*	SAI2_RXC/AB22	I, 3.3V CMOS	UART1 serial data receiver. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
100	UART1_CTS_B*	SAI2_TXFS/AD23	O, 3.3V CMOS	UART1 Clear to Send. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
101	UART1_RTS_B*	SAI2_RXD0/AC24	I, 3.3V CMOS	UART1 Request to Send. *Note: This Signal is Optionally Connected to SODIMM Edge. Default not Populated*
102	UART2_TX(SAI3_TXC)	SAI3_TXC/AG6	O, 3.3V CMOS	UART2 serial data transmitter.
103	UART2_RX(SAI3_TXFS)	SAI3_TXFS/AC6	I, 3.3V CMOS	UART2 serial data receiver.
104	SAI1_RXFS (NC in Nano)	SAI1_RXFS/AG16	I, 3.3V CMOS	SAI1 Receiver Frame Sync *Note: This signal is by default configured as General-Purpose Input Output.*
105	SD2_CD_B	SD2_CD_B/AA26	I, 3.3V/1.8V CMOS	SD Card Detect
106	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
107	SD2_DATA0	SD2_DATA0/AB23	IO, 3.3V/1.8V CMOS	SD data 0 line.
108	SD2_CMD	SD2_CMD/W24	IO, 3.3V/1.8V CMOS	SD command line.
109	SD2_CLK	SD2_CLK/W23	O, 3.3V/1.8V CMOS	SD Clock Line.
110	NC	NA	NA	NC.
111	SD2_DATA1	SD2_DATA1/AB24	IO, 3.3V/1.8V CMOS	SD data 1 line.
112	SD2_DATA2	SD2_DATA2/V24	IO, 3.3V/1.8V CMOS	SD data 2 line
113	GND	NA	Power	Ground.

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
114	SD2_DATA3	SD2_DATA3/V23	IO, 3.3V/1.8V CMOS	SD data 3 line.
115	I2C2_SDA	I2C2_SDA/D9	IO, 3.3V OD/4.7K PU	I2C2 Data signal.
116	I2C2_SCL	I2C2_SCL/D10	O, 3.3V OD/4.7K PU	I2C2 Clock signal.
117	UART4_RXD	UART4_RXD/F19	I, 3.3V CMOS	Debug UART Receiver.
118	UART4_TXD	UART4_TXD/F18	O, 3.3V CMOS	Debug UART Transmitter
119	NC	NA	NA	NC.
120	NC	NA	NA	NC.
121	BCONFIG_1(GPIO5_1) *	SAI3_TXD/AF6	IO,3.3V CMOS 10 PU & PD	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting. Optionally Connected to SODIMM Edge. Default not Populated*
122	NC	NA	NA	NC.
123	SAI1_RXD5 (NC in Nano)	SAI1_RXD5/AF18	I, 3.3V CMOS 4.7K PU	SAI1 Receiver Data 5. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
124	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
125	PWM2_OUT(I2C4_SCL)	I2C4_SCL/D13	O, 3.3V CMOS	Pulse Width Modulation 2 Output
126	BCONFIG_0(GPIO1_9) *	GPIO1_IO09/ AF10	IO,1.8/3.3V CMOS	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting. Optionally Connected to SODIMM Edge. Default not Populated*
127	PCIE_TXP (NC in Nano)	PCIE_TXN_P/B20	O, PCIe/ 0.1uF AC Coupled	PCIe Transmit Positive.
128	PCIE_RXP (NC in Nano)	PCIE_RXN_P/B19	I, PCIe	PCIe Receive Positive
129	PCIE_TXN (NC in Nano)	PCIE_TXN_N/A20	O, PCIe/ 0.1uF AC Coupled	PCIe Transmit Negative.
130	PCIE_RXN (NC in Nano)	PCIE_RXN_N/A19	I, PCIe	PCIe Receive Negative
131	GND	NA	Power	Ground.
132	GPIO_RESET(GPIO5_2)	SAI3_TXD/AF6	O, 3.3V CMOS	General Purpose Reset Output.

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
133	W_DISABLE(GPIO1_11)	GPIO1_IO11/AC10	IO, 3.3V CMOS	General Purpose Input/Output. *Note: This signal is used PCIe W_DISABLE.*
134	PCIE_WAKE_B(GPIO1_10)	GPIO1_IO10/AD10	I, 3.3V CMOS	Used for PCIe WAKE.
135	PCIE_REFCLK_DP (NC in Nano)	NA	O, HCSL	PCIe Clock Positive.
136	GPIO1_1	GPIO1_IO01/AF14	IO, 3.3V CMOS	General Purpose Input Output.
137	PCIE_REFCLK_DM (NC in Nano)	NA	O, HCSL	PCIe Clock Negative.
138	PWM1_OUT(I2C4_SDA)	I2C4_SDA/E13	O, 3.3V CMOS	Pulse Width Modulation 1 Output
139	USB2_ID (NC in Nano)	NC	I,3.3V CMOS	USB2 OTG ID.
140	USB2_OTG_PWR(GPIO1_14)	GPIO1_IO14/AC9	O, 3.3V CMOS	Used for USB OTG1 Power enable
141	USB_OTG2_VBUS (NC in Nano)	NC	I, Power 5V	USB2 VBUS Power.
142	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
143	SAI1_TXFS (NC in Nano)	SAI1_TXFS/AB19	O, 3.3V CMOS	SAI1 Transmitter Frame Sync. *Note: This signal is by default configured as General-Purpose Input Output.*
144	SAI1_RXD7 (NC in Nano)	SAI1_RXD7/AF19	I, 3.3V CMOS/ 100K PD	SAI1 Receiver Data 7. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
145	SAI1_MCLK (NC in Nano)	SAI1_MCLK/AB18	O, 3.3V CMOS	SAI1 Master Clock. *Note: This signal is by default configured as General-Purpose Input Output.*
146	GPIO1_8	GPIO1_IO08/AG10	IO, 3.3V CMOS	General Purpose Input Output.
147	GPIO1_5	GPIO1_IO05/AF12	IO, 3.3V CMOS	General Purpose Input Output.
148	SAI1_RXD3 (NC in Nano)	SAI1_RXD3/AF17	I, 3.3V CMOS 100K PD	SAI1 Receiver Data 3. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
149	SAI1_RXD4 (NC in Nano)	SAI1_RXD4/AG18	I, 3.3V CMOS 100K PD	SAI1 Receiver Data 4. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no*

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
				external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration
150	MIPI_CSI_CLK_N	MIPI_CSI_CLK_N/ A16	I, MIPI	MIPI CSI differential Clock Negative.
151	GND	NA	Power	Ground.
152	MIPI_CSI_CLK_P	MIPI_CSI_CLK_P/ B16	I, MIPI	MIPI CSI differential Clock Positive.
153	I2C3_SCL	I2C3_SCL/E10	O, 3.3V OD/4.7K PU	I2C3 Clock signal.
154	SAI1_TXD7 (NC in Nano)	SAI1_TXD7/AF23	O, 3.3V CMOS 100K PD	SAI1 Transmit Data 7. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
155	I2C3_SDA	I2C3_SDA/F10	IO, 3.3V OD/4.7K PU	I2C3 Data signal.
156	SAI1_TXD0 (NC in Nano)	SAI1_TXD0/AG20	O, 3.3V CMOS 100K PD	SAI1 Transmit Data 0. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
157	SAI1_TXC (NC in Nano)	SAI1_TXC/AC18	O, 3.3V CMOS	SAI1Transmit Clock Output. *Note: This signal is by default configured as General-Purpose Input Output.*
158	SAI1_RXD1 (NC in Nano)	SAI1_RXD1/AF15	I, 3.3V CMOS 4.7K PU	SAI1 Receiver Data 1. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
159	MIPI_CSI_DATA1_N	MIPI_CSI_D1_N/A 15	I, MIPI	MIPI CSI differential data lane 1 negative
160	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
161	MIPI_CSI_DATA1_P	MIPI_CSI_D1_P/B 15	I, MIPI	MIPI CSI differential data lane 1 positive
162	MIPI_CSI_DATA2_N	MIPI_CSI_D2_N/A 17	I, MIPI	MIPI CSI differential data lane 2 negative
163	SAI1_TXD4 (NC in Nano)	SAI1_TXD4/AG22	O, 3.3V CMOS 100K PD	SAI1 Transmit Data 4. *Note: These signals are also used for i.MX8M Mini*

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
				SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration
164	MIPI_CSI_DATA2_P	MIPI_CSI_D2_P/B17	I, MIPI	MIPI CSI differential data lane 2 positive
165	SAI1_TXD5 (NC in Nano)	SAI1_TXD5/AF22	O, 3.3V CMOS 4.7K PU	SAI1 Transmit Data 5. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
166	SAI1_TXD1 (NC in Nano)	SAI1_TXD1/AF20	O, 3.3V CMOS 4.7K PU	SAI1 Transmit Data 1. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
167	SAI1_TXD2 (NC in Nano)	SAI1_TXD2/AG21	O, 3.3V CMOS 100K PD	SAI1 Transmit Data 2. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
168	MIPI_CSI_DATA0_N	MIPI_CSI_D0_N/A14	I, MIPI	MIPI CSI differential data lane 0 negative
169	GND	NA	Power	Ground.
170	MIPI_CSI_DATA0_P	MIPI_CSI_D0_P/B14	I, MIPI	MIPI CSI differential data lane 0 positive
171	SAI1_TXD6 (NC in Nano)	SAI1_TXD6/AG23	O, 3.3V CMOS	SAI1 Transmit Data 6. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
172	MIPI_CSI_DATA3_N	MIPI_CSI_D3_N/A18	I, MIPI	MIPI CSI differential data lane 3 negative
173	SAI1_TXD3 (NC in Nano)	SAI1_TXD3/AF21	O, 3.3V CMOS 4.7K PU	SAI1 Transmit Data 3. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be*

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
				connected to these pins which will change the boot configuration
174	MIPI_CSI_DATA3_P	MIPI_CSI_D3_P/B18	I, MIPI	MIPI CSI differential data lane 3 positive
175	SAI1_RXD6 (NC in Nano)	SAI1_RXD6/AG19	I, 3.3V CMOS 100K PD	SAI1 Receiver Data 6. *Note: These signals are also used for i.MX8M Mini SOC boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
176	SPDIF_EXT_CLK	SPDIF_EXT_CLK/AF8	O, 3.3V CMOS	Sony/Philips Digital Interface Clock. *Note: This signal is by default configured as General-Purpose Input Output.*
177	SPDIF_RX	SPDIF_RX/AG9	I, 3.3V CMOS	Sony/Philips Digital Interface Receive. *Note: This signal is by default configured as General-Purpose Input Output.*
178	SPDIF_TX	SPDIF_TX/AF9	O, 3.3V CMOS	Sony/Philips Digital Interface Transmit. *Note: This signal is by default configured as General-Purpose Input Output.*
179	ON_OFF	ONOFF/A25	I, 3.3V CMOS	This signal is Connected to SOC ONOFF Pin
180	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
181	ECSPI3_SS0(UART2_TXD)	UART2_TXD/E15	O, 3.3V CMOS	SPI3 Chip select signal.
182	BOOT_MODE0	BOOT_MODE0/G26	I, 3.3V CMOS	Boot mode selection pin 0 *Note: This pin is connected from two-bit DIP switch for selecting the desired boot mode.*
183	VRTC_3V0	NA	I, 3V Power	3V backup coin cell input for RTC.
184	BOOT_MODE1	BOOT_MODE1/G27	I, 3.3V CMOS	Boot mode selection pin 1 *Note: This pin is connected from two-bit DIP switch for selecting the desired boot mode.*
185	GND	NA	Power	Ground.
186	GND	NA	Power	Ground.
187	N_RST_OUT	NA	I, 3.3V CMOS	This Pin is used for Carrier Hard Reset
188	USB2_DP (NC in Nano)	USB2_DP/B23	IO, USB	USB2 OTG High Speed Data Positive.
189	ECSPI3_SCLK(UART1_RXD)	UART1_RXD/E14	O, 3.3V CMOS	SPI3 clock signal.
190	USB2_DN (NC in Nano)	USB2_DN/A23	IO, USB	USB2 OTG High Speed Data Positive.
191	JTAG_TDO	JTAG_TDO/E26	O, 3.3V CMOS	JTAG Test Data Output.
192	VIN_3V3	NA	I, 3.3V Power	Supply Voltage.
193	JTAG_TRST_B(BOOT_MODE2)	JTAG_TRST_B/C27	I, 3.3V CMOS	JTAG Test Reset.

Pin No.	SODIMM Edge Connector Signal Name	SOC Ball Name/ Pin Number	Signal Type/ Termination	Description
194	ECSPI3_MOSI(UART1_TXD)	UART1_TXD/F13	O, 3.3V CMOS	SPI3 Master Output Slave Input.
195	JTAG_TDI	JTAG_TDI/E27	I, 3.3V CMOS	JTAG Test Data Input.
196	ECSPI3_MISO(UART2_RXD)	UART2_RXD/F15	I, 3.3V CMOS	SPI3 Master Input Slave Output.
197	JTAG_TCK	JTAG_TCK/F26	I, 3.3V CMOS	JTAG Test Clock.
198	GND	NA	Power	Ground.
199	JTAG_TMS	JTAG_TMS/F27	I, 3.3V CMOS	JTAG Test Mode Select.
200	USB_OTG1_VBUS	NC	I, Power 5V	USB1 VBUS Power.

Optional feature, by default not supported.

2.4 Serial Interface Features

2.4.1 Debug UART

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board supports debug interface through i.MX 8M Mini or i.MX 8M Nano UART4 interface. This UART4 signals from SODIMM Edge connector is connected to UART to USB Convertor "FT232RQ-REEL" and to USB Micro AB Connector (J8). This USB Micro AB Connector can be used for debug purpose which is physically located at the top of the board as shown below.
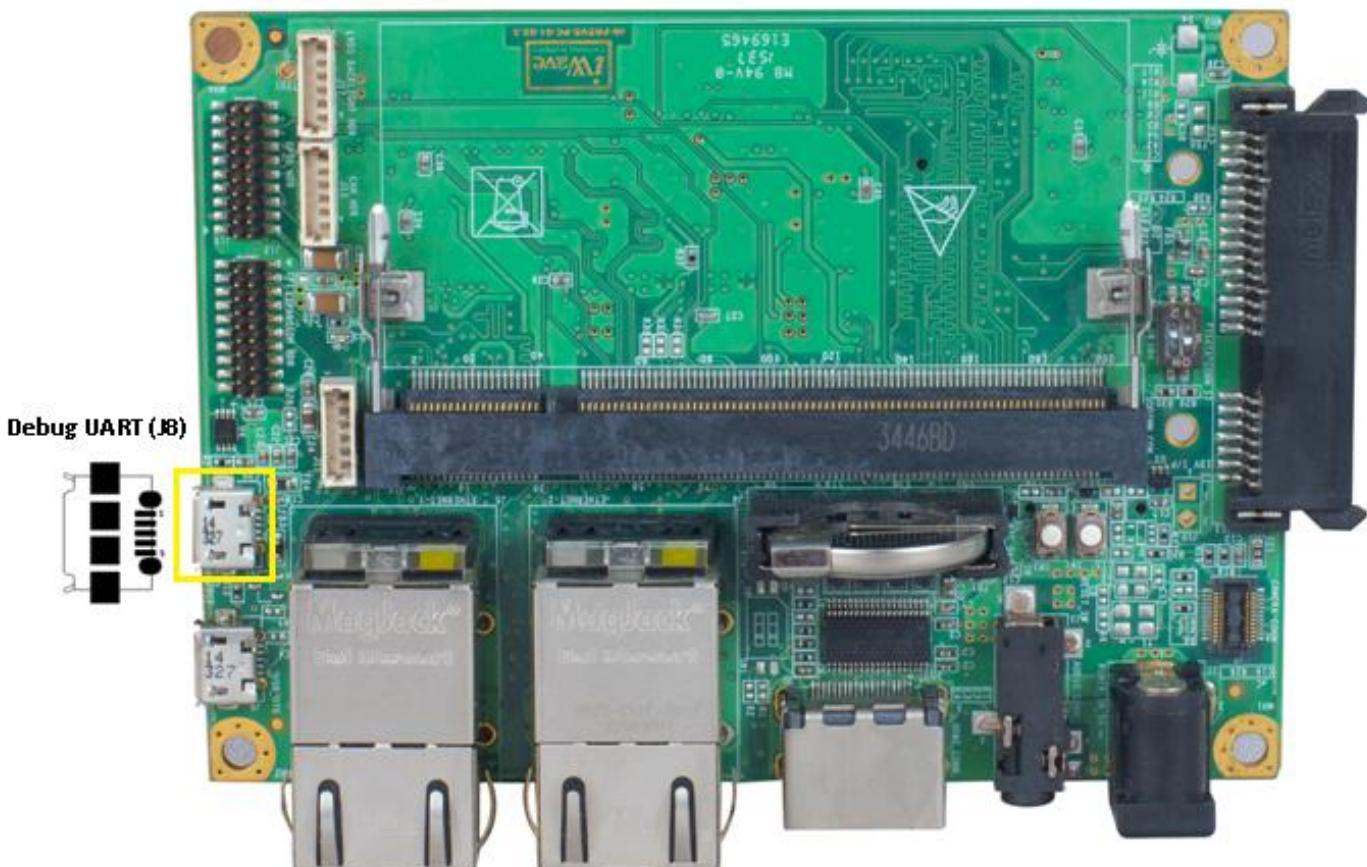
Figure 3: Debug UART

Table 4: Debug UART Connector Pin Out

Pin No	Pin Name	Signal Type / Termination	Description
1	V_DBG_5V	I, 5V Power	5V Power.
2	DBUG_USB_DM	IO, Diff	Debug USB Data negative.
3	DBUG_USB_DP	IO, Diff	Debug USB Data positive.
4	DBUG_USB_ID	NC	No connect.
5	DBUG_USB_GND	Power	Ground.

2.4.2 Data UART Header

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports full functional Data UART interface through i.MX 8M Mini or i.MX 8M Nano SOC's UART2 interface. These UART signals from SODIMM Edge connector is connected directly to 6pin Header (J11) for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins   : 6

Connector Part number : 53047-0610

Mating Connector   : 51021-0600 from Molex

Figure 4: Data UART Header

Table 5: Data UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	UART2_CTS_B(SAI3_RXC)	O, 3.3V CMOS	UART2 Interface Clear To Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART_TXD	UART2_TX(SAI3_TXC)	O, 3.3V CMOS	UART2 Interface Transmit signal.
5	UART_RXD	UART2_RX(SAI3_TXFS)	I, 3.3V CMOS	UART2 Interface Receive signal.
6	UART_RTS#	UART2_RTS_B(SAI3_RXD)	I, 3.3V CMOS	UART2 IPterface Ready to Send signal.

2.5   Communication Features

2.5.1 10/100/1000Mbps Ethernet -1

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports 10/100/1000Mbps Ethernet interface through on SOM Ethernet PHY. Ethernet PHY output signals from SODIMM Edge connector is connected to RJ45 Magjack1 (J5). The Ethernet Jack supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack connector. This RJ45 Magjack connector is physically located at the top of the board as shown below.
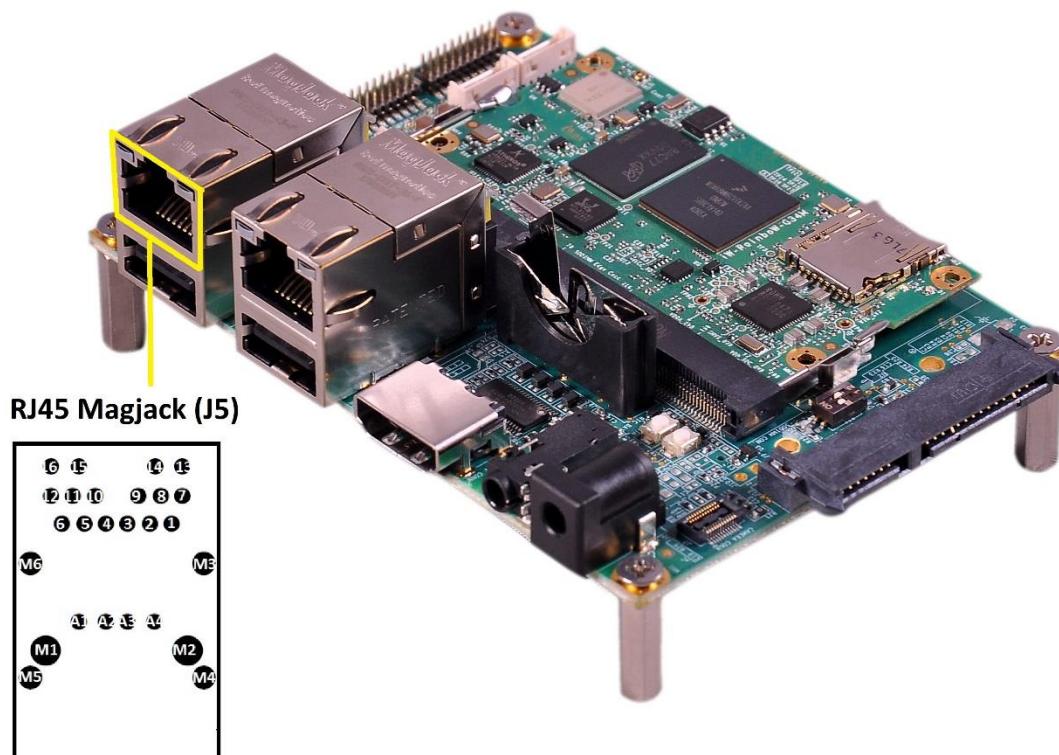

Figure 5: 10/100/1000Mbps RJ45 MagJack -1

2.5.2 10/100/1000 Mbps Ethernet-2 (Optional) (Not available in Nano)

i.MX 8M Mini SODIMM carrier board supports 2nd 10/100/1000Mbps Ethernet interface through on SOM PCIe to Ethernet PHY which supports up to 1Gbps Ethernet. The Ethernet PHY output signals from SODIMM Edge connector is connected to RJ45 Magjack (J4). The Ethernet supports Speed (Green) and Link/Activity (Yellow) LED indications on RJ45 Magjack connector. This RJ45 Magjack connector is physically located at the top of the board.

Note: In i.MX 8M Mini SOM, PCIe lane signals are optionally to connected to PCIe to Ethernet controller and by default connected to SODIMM PCB Edge Connector. So, either one interface can be supported in the i.MX 8M Mini SOM. Please contact iWave, if 10/100/1000Mbps Ethernet interface support is required in 2nd Ethernet Port.
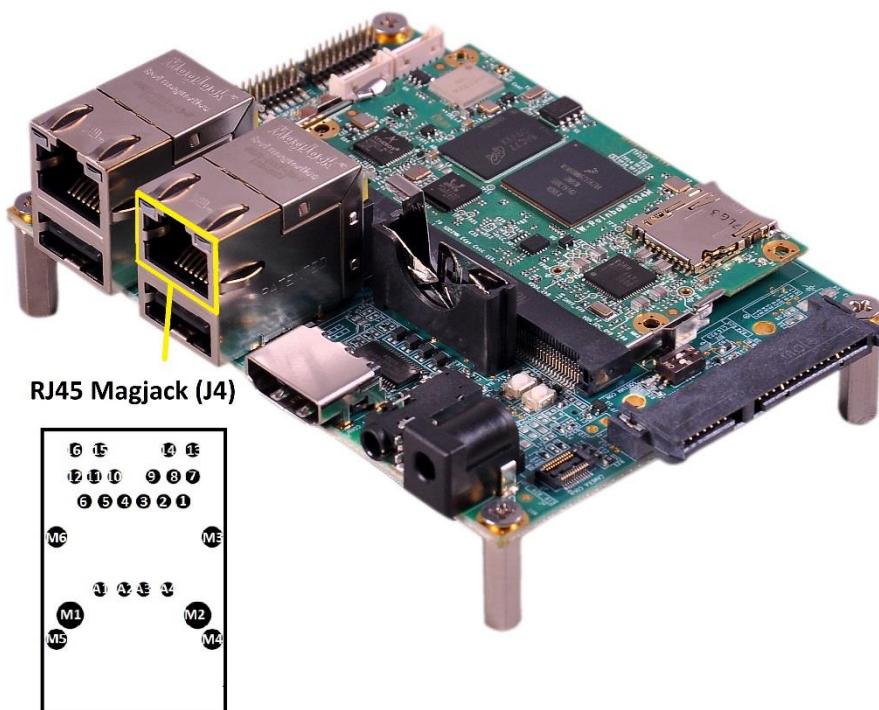
Figure 6: 10/100/1000Mbps RJ45 MagJack-2

Note: Either Mini PCIe connector or 2nd Ethernet Port can be supported at a time.

2.5.3 USB2.0 Device

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports high speed USB2.0 device interface through i.MX 8M Mini or i.MX 8M Nano SOC's USB_OTG1 controller. This USB2.0 signals from SODIMM Edge connector is directly connected to USB Micro AB connector (J6). USB OTG as device functionality is only supported in i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board. This USB Micro AB connector is physically located at the top of the board as shown below.

Figure 7: USB2.0 Device Port

2.5.4 USB2.0 Host (Not available in Nano)

i.MX 8M Mini SODIMM carrier board supports USB2.0 High Speed Host interface through i.MX 8M Mini SOC's USB_OTG2 Controller. This USB host interface signals from SODIMM Edge connector is connected to 2port USB HUB "USB2422/MJ" to support two USB 2.0 high speed host ports in the carrier board. USB host ouput1 of USB Hub is connected to USB Type A connector1 (J5) and USB host ouput2 is connected to USB Type A connector2 (J4).

The VBUS power of these USB2.0 connectors are connected through current limiting power switch which limits the current above 500mA. If the connected USB2.0 host takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of SODIMM Connector. These USB2.0 Type A host connectors are physically located at the top of the board as shown below.

USB HOST 1 (J5)

USB HOST 2 (J4)
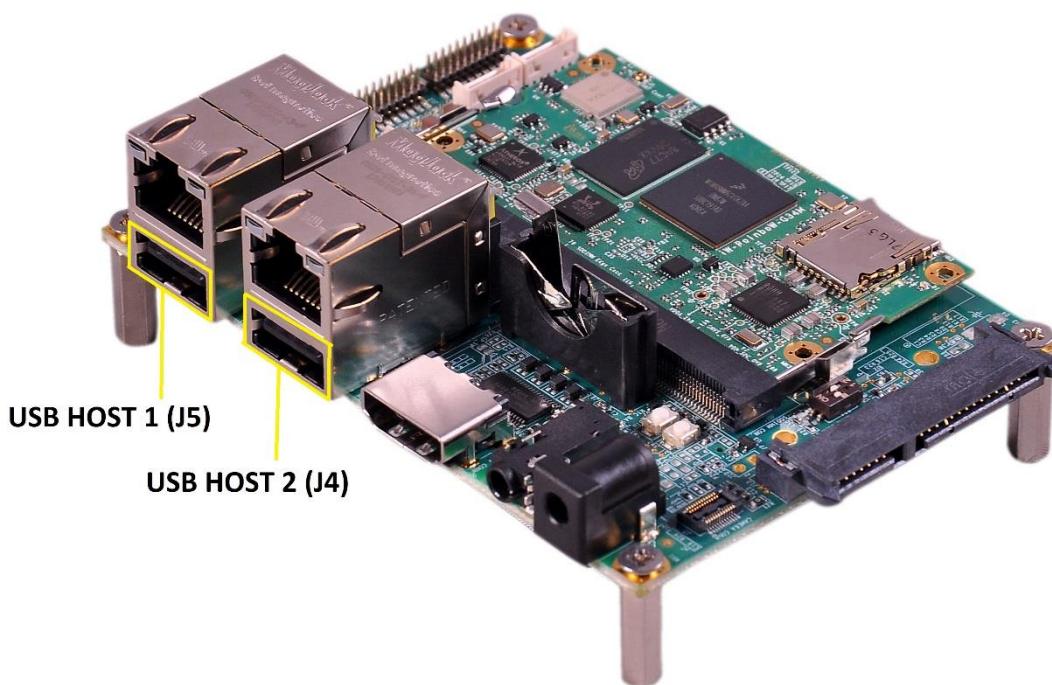
Figure 8: USB 2.0 Host Ports

2.5.5 MicroSD Slot

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports SDIO interface through i.MX 8M Mini or i.MX 8M Nano SOC's USDHC2 interface. This USDHC2 signals from SODIMM Edge connector is connected to Micro SD connector (J19) to support Micro SD storage. The main power to Micro SD connector is 3.3V. This Micro SD connector (J19) is physically located at the bottom of the board as shown below.
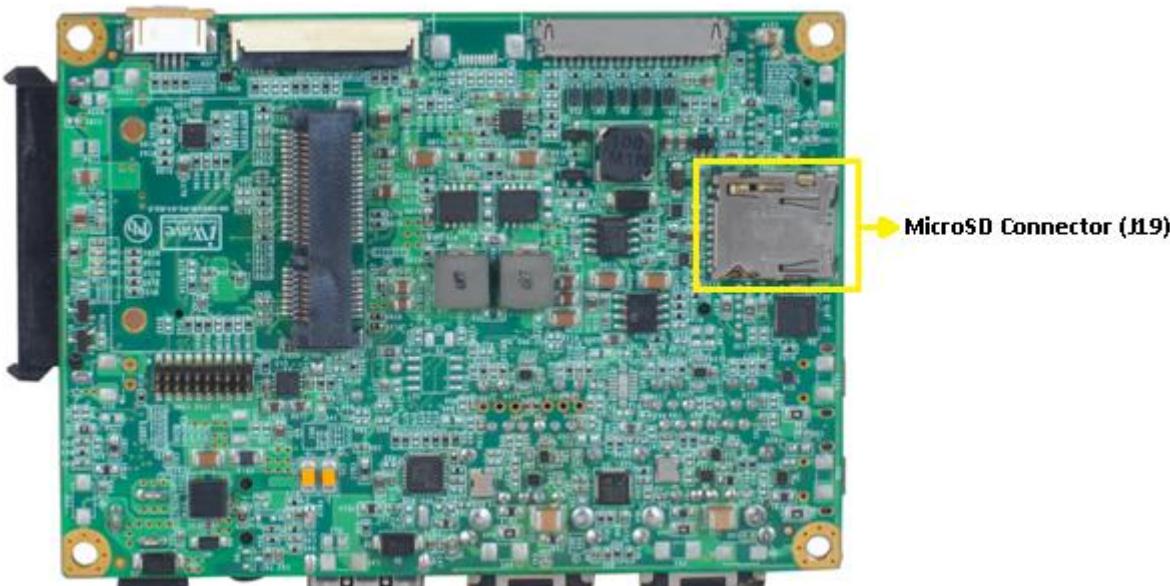

Figure 9: Micro SD Connector

2.6 High Speed Interfaces

2.6.1 Mini PCIe Port

i.MX 8M Mini SODIMM Carrier Board supports Mini PCIe connector to support Mini-PCIe device. Optional 0E resistor R166 for PCIE_RXM and R170 for PCIE_RXP has been populated at the connector receiver signal side for PCIe device coupling option. Mini PCIe connector (J20) is physically located at bottom of the board as shown below
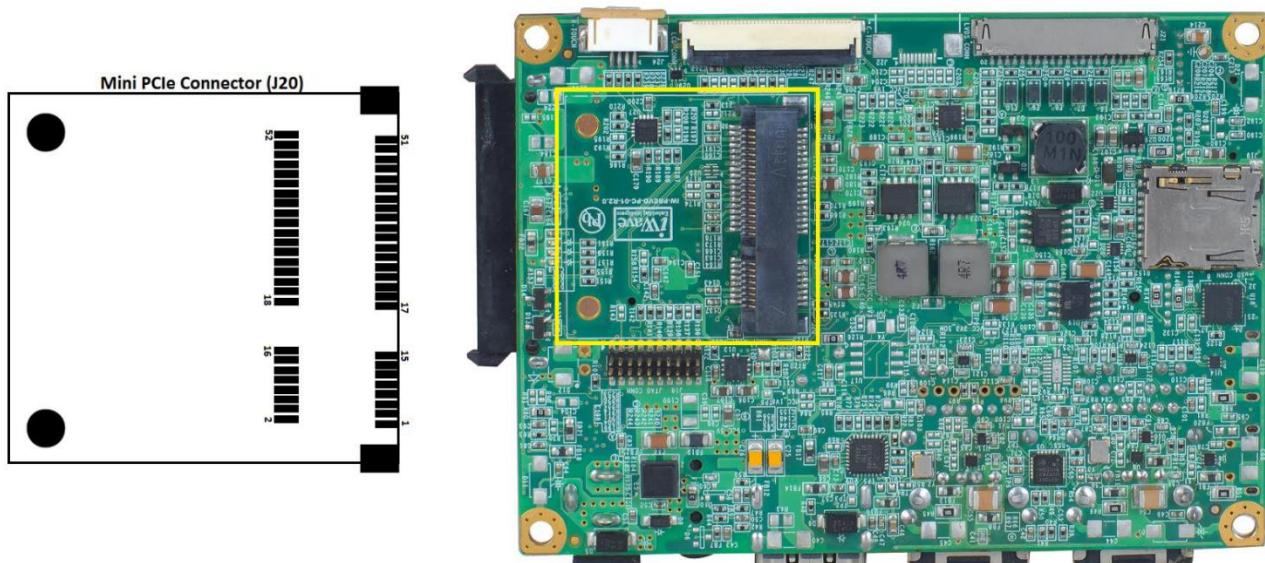
Figure 10: Mini PCIe Slot

Note: Either Mini PCIe connector or 2nd Ethernet Magjack can be supported at a time.

Table 6: Mini PCIe Slot Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	Wake#	PCIe_WAKE_B(GPIO1_10)	I, 3.3V CMOS 10K UP	PCIe interface Wake Up Signal.
2	VCC_PCIe3V3	VCC_PCIe3V3	O, 3.3V Power	3.3V Power Supply.
3	COEX1	NC	-	NC.
4	GND	GND	Power	Ground.
5	COEX2	NC	-	NC.
6	VCC_1V5_3G	VCC_1V5_3G	O, 1.5V	Power Supply for 3G
7	CLKREQ#	NC	-	NC.
8	UIM_PWR	NC	-	NC.
9	GND	GND	Power	Ground.
10	UIM_DATA	NC	-	NC.
11	PCIE_REFCLK_DM(CLK1_N)	PCIE_REFCLK_DM	O, DIFF	PCIe reference clock negative.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
12	UIM_CLK	NC	-	NC.
13	PCIE_REFCLK_DP(CLK1_P)	PCIE_REFCLK_DP	O, DIFF	PCIe reference clock positive.
14	UIM_RESET	NC	-	NC.
15	GND	GND	Power	Ground
16	UIM_VPP	NC	-	NC.
17	RSVD(UIM_C8)	NC	-	NC.
18	GND	GND	Power	Ground.
19	RSVD(UIM_C84	NC	-	NC.
20	GPIO7_IO12(GPIO_17)	W_DISABLE(GPIO1_11)	O, 3.3V CMOS	Wireless Disable.
21	GND	GND	Power	Ground.
22	GPIO7_IO11(GPIO_16)	N_RST_OUT	O, 3.3V CMOS	Reset Input, Active Low. *Note: This GPIO is optionally connected to Mini PCIe Conn.*
23	PCIE_RXM	PCIE_RXN	I, DIFF	PCIe Receive Pair Negative
24	VCC_PCIe3V3	VCC_PCIe3V3	O, 3.3V Power	3.3V Power Supply.
25	PCIE_RXP	PCIE_RXP	I, DIFF	PCIe Receive Pair Positive
26	GND	GND	Power	Ground
27	GND	GND	Power	Ground
28	VCC_1V5_3G	VCC_1V5_3G	O, 1.5V	Power Supply for 3G
29	GND	GND	Power	Ground
30	I2C3_SCL(GPIO_3)	I2C2_SCL	O, 3.3V CMOS	System Management Bus Clock.
31	PCIE_TXM	PCIE_TXN	O, DIFF	PCIe Transmit Pair negative
32	I2C3_SDA(GPIO_6)	I2C2_SDA	IO, 3.3V CMOS	System Management Data.
33	PCIE_TXP	PCIE_TXP	O, DIFF	PCIe Transmit Pair Positive
34	GND	GND	Power	Ground
35	GND	GND	Power	Ground
36	3G_USB_D-	NA	IO, DIFF	USB Host Data negative. This signal is optionally connected to USB hub and J4B USB connector.
37	GND	GND	Power	Ground
38	3G_USB_D+	NA	IO, DIFF	USB Host Data negative. This signal is optionally connected to USB hub and J4B USB connector.
39	VCC_PCIe3V3	VCC_PCIe3V3	O, 3.3V Power	3.3V Power Supply.
40	GND	GND	Power	Ground
41	VCC_PCIe3V3	VCC_PCIe3V3	O, 3.3V	3.3V Power Supply.
42	LED_WWAN#	NA	I, 3.3V CMOS	LED Enable. Connected to green LED D15 and default populated.
43	GND	GND	Power	Ground
44	LED_WLAN#	NA	I, 3.3V CMOS	LED Enable.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
				Connected to green LED D16 and default populated.
45	RSVD	NC	-	NC.
46	LED_WPAN#	NA	I, 3.3V CMOS	LED Enable. Connected to green LED D17 and default populated.
47	RSVD1	NC	-	NC.
48	VCC_1V5_3G	VCC_1V5_3G	O, 1.5V	Power Supply for 3G
49	RSVD2	NC	-	NC.
50	GND	GND	Power	Ground
51	RSVD3	NC	-	NC.
52	VCC_PCIe3V3	VCC_PCIe3V3	O, 3.3V Power	3.3V Power Supply.

2.7   Audio/Video Features

2.7.1 Audio IN/OUT Jack

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports Audio In/Out through i.MX 8M Mini or i.MX 8M Nano SOC's SAI5 interface. This four wire SAI5 signals from SODIMM Edge connector is connected to I2S Audio Codec "SGTL5000XNAA3R2" to support Headphone Stereo output and Mono Mic input which is supported through 3.5mm Audio Jack (J3) with OMTP standard. This Audio Jack is physically located at the top of the board as shown below.
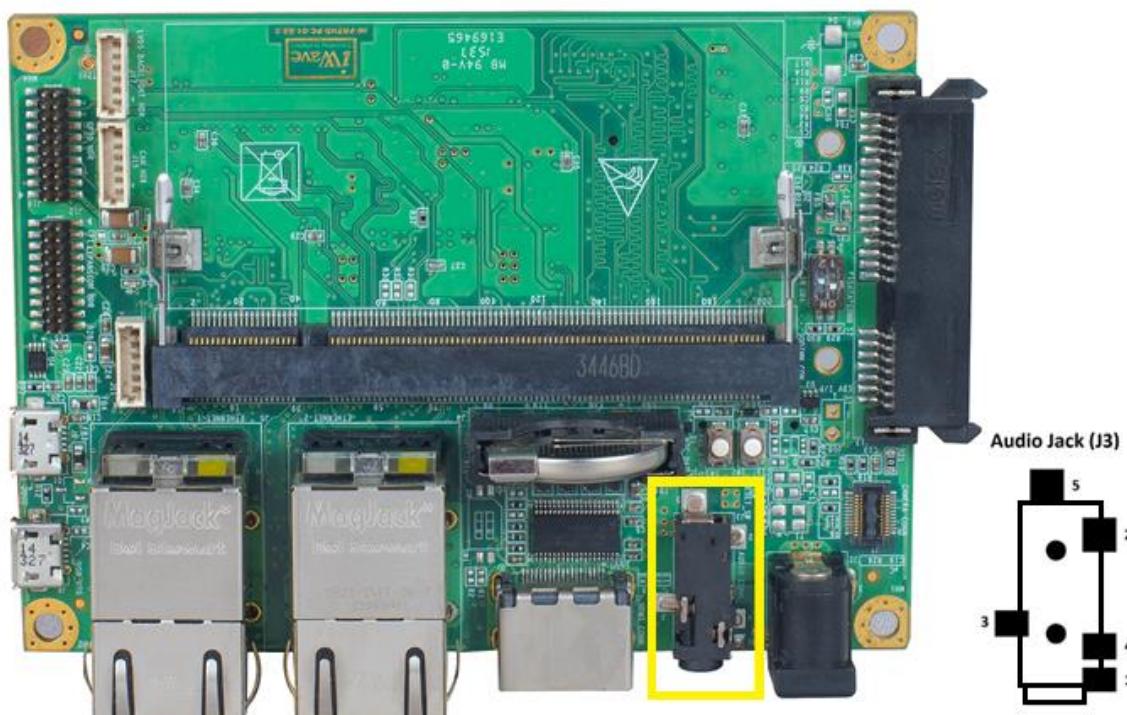

Figure 11: Audio IN/OUT Jack

Table 7: Audio In/Out Jack Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	AGND	GND	Power	Analog Ground.
2	HP_Left	HP_L	O, Analog	Headphone Output Left.
3	HP_Right	HP_R	O, Analog	Headphone Output Right.
4	MIC	MIC	I, Analog	Microphone Input Signal.
5	NC	NC	-	No Connect.

2.8 Additional Features

2.8.1 MIPI CSI Camera Connector

i.MX 8M Mini or i.MX 8M Nano SODIMM development platform supports MIPI CSI Camera interface through i.MX 8M Mini or i.MX 8M Nano SOC's MIPI CSI interface. These signals from SODIMM Edge connector is directly connected to 40pin flip connector (J23) of the Carrier board which comprises of MIPI CSI signals, control signals and GPIOs for MIPI Camera and MIPI Display interface.
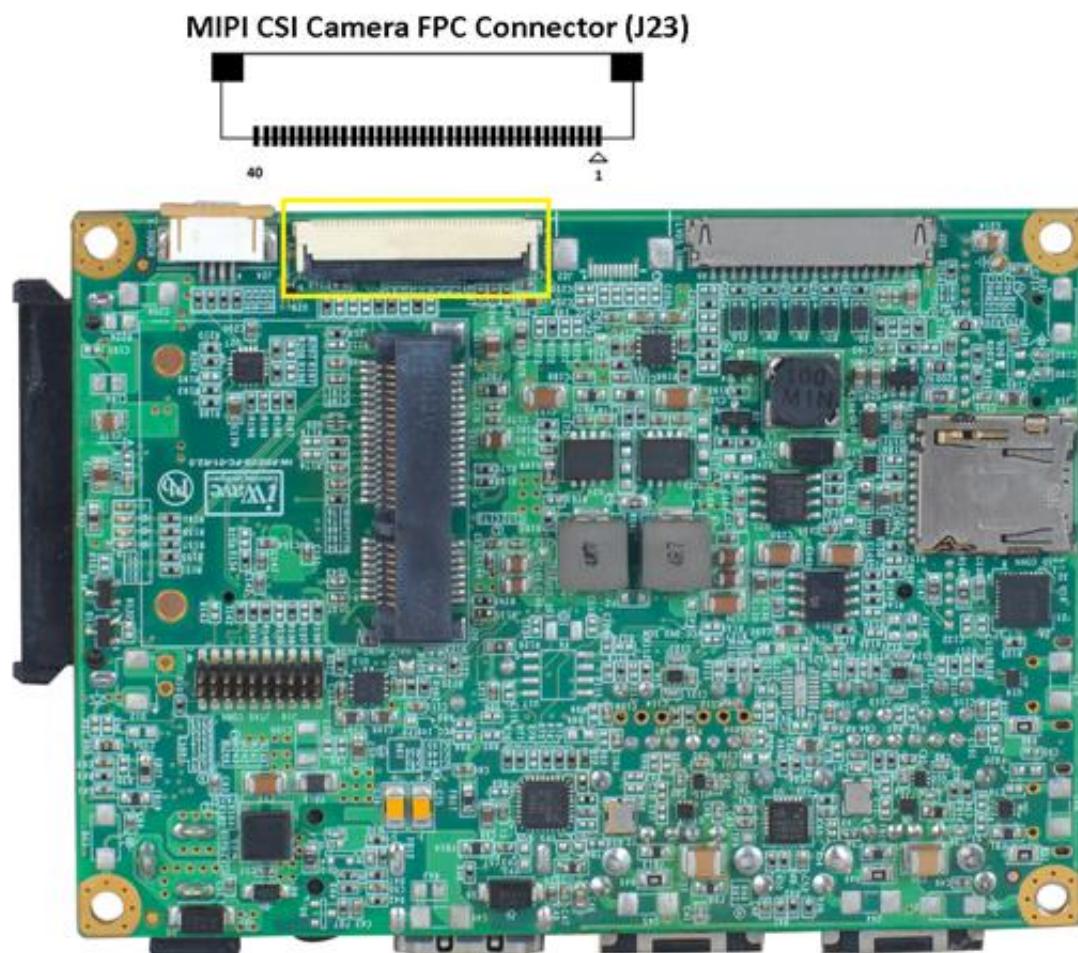

Figure 12: MIPI CSI Camera FPC Connector

Table 8: 40 Pin -MIPI CSI Camera FPC Connector

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VSS1	GND	Power	Ground.
2	VSS2	GND	Power	Ground.
3	VCC1	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
4	VCC2	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
5	PWRCTRL	GPIO1_1	O,3.3V CMOS/ 10K PU	General Purpose Input/Output.
6	LEDCTRL	GPIO1_5	O,3.3V CMOS	General Purpose Input/Output.
7	RESETn/NC1	N_RST_OUT	O,3.3V CMOS	Reset Output.
8	B5	MIPI_CSI_DATA3_P	I, DIFF	MIPI CSI differential data lane 3 positive.
9	B4 (NC in Nano)	SAI1_TXD3	O,3.3V CMOS	SAI1 Transmit 3.
10	B3	MIPI_CSI_DATA3_N	I, DIFF	MIPI CSI differential data lane 3 negative.
11	B2 (NC in Nano)	SAI1_TXD6	O,3.3V CMOS	SAI1 Transmit 6.
12	B1	MIPI_CSI_DATA0_P	I, DIFF	MIPI CSI differential data lane 0 positive.
13	B0	MIPI_CSI_DATA0_N	I, DIFF	MIPI CSI differential data lane 0 negative.
14	VSS3	GND	Power	Ground.
15	G5 (NC in Nano)	SAI1_TXD5	O,3.3V CMOS	SAI1 Transmit 5.
16	G4	MIPI_CSI_DATA2_P	I, DIFF	MIPI CSI differential data lane 2 positive.
17	G3 (NC in Nano)	SAI1_TXD4	O,3.3V CMOS	SAI1 Transmit 4.
18	G2	MIPI_CSI_DATA2_N	I, DIFF	MIPI CSI differential data lane 2 negative
19	G1	MIPI_CSI_DATA1_P	I, DIFF	MIPI CSI differential data lane 1 positive.
20	G0	MIPI_CSI_DATA1_N	I, DIFF	MIPI CSI differential data lane 1 negative
21	VSS4	GND	Power	Ground.
22	R5 (NC in Nano)	SAI1_TXD0	O,3.3V CMOS	SAI1 Transmit 0.
23	R4	I2C3_SDA	O,3.3V CMOS	I2C3 Data.
24	R3 (NC in Nano)	SAI1_TXD7	O,3.3V CMOS	SAI1 Transmit 7.
25	R2	I2C3_SCL	O,3.3V CMOS	I2C3 Clock.
26	R1	MIPI_CSI_CLK_P	I, DIFF	MIPI CSI differential clock positive.
27	R0	MIPI_CSI_CLK_N	I, DIFF	MIPI CSI differential clock negative.
28	DCLK (NC in Nano)	SAI1_MCLK	O,3.3V CMOS	SAI1 Master clock.
29	VSS5	GND	Power	Ground.
30	HSYNC (NC in Nano)	SAI1_RXD7	I,3.3V CMOS	SAI1 Receive 7.
31	VSYNC (NC in Nano)	SAI1_TXFS	O,3.3V CMOS	SAI1 Transmit sync.
32	ENB	GPIO1_8	O,3.3V CMOS	General Purpose Input/Output.
33	ROTATE/NC2 (NC in Nano)	SAI1_TXD1	-	SAI1 Transmit 1.
34	SHUT/STB/NC3 (NC in Nano)	SAI1_TXD2	-	SAI1 Transmit 2.
35	VSS6	GND	Power	Ground.
36	VDD	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
37	YU/NC	NA	-	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
38	XR/NC	NA	-	NC.
39	YD/NC	NA	-	NC.
40	XL/NC	NA	-	NC.

2.8.2 MIPI DSI Display Interface Connector

The i.MX 8M Mini or i.MX 8M Nano SODIMM development platform supports MIPI DSI interface connector from i.MX 8M Mini or i.MX 8M Nano SOC's MIPI_DSI interface from SODIMM Edge connector is used to validate MIPI LCD interface. This MIPI DSI interface signals from SODIMM Edge connector is connected through common mode choke to 20pin MIPI DSI interface connector (J21) of the Carrier Board. This is physically located at the Bottom of the board as shown below.
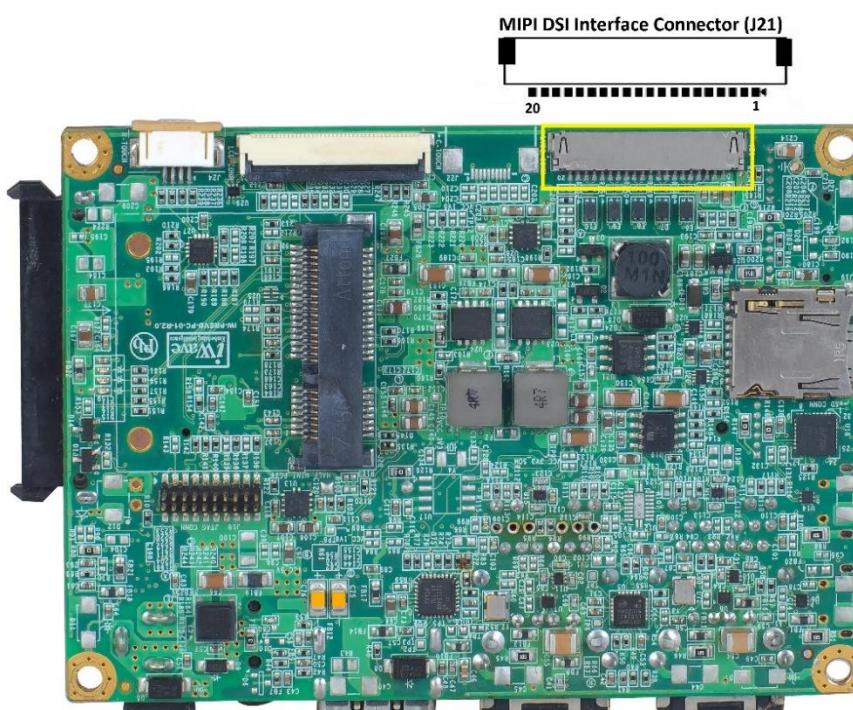

Figure 13: MIPI DSI display interface Connector

Table 9: 20 Pin -MIPI DSI Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VDD	VCC_3V3	Power	3.3V Supply Voltage.
2	VDD	VCC_3V3	Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	GND	GND	Power	Ground.
5	LVDS0_TX0_N	MIPI_DSI_DATA0_N	O, DIFF	MIPI_DSI DATA Lane0 Negative.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
6	LVDS0_TX0_P	MIPI_DSI_DATA0_P	O, DIFF	MIPI_DSI DATA Lane0 Positive.
7	GND	GND	Power	Ground.
8	LVDS0_TX1_N	MIPI_DSI_DATA1_N	O, DIFF	MIPI_DSI DATA Lane1 Negative.
9	LVDS0_TX1_P	MIPI_DSI_DATA1_P	O, DIFF	MIPI_DSI DATA Lane1 Positive.
10	GND	GND	Power	Ground.
11	LVDS0_TX2_N	MIPI_DSI_DATA2_N	O, DIFF	MIPI_DSI DATA Lane2 Negative.
12	LVDS0_TX2_P	MIPI_DSI_DATA2_P	O, DIFF	MIPI_DSI DATA Lane2 Positive.
13	GND	GND	Power	Ground.
14	LVDS0_CLK_N	MIPI_DSI_CLK_N	O, DIFF	MIPI_DSI Clock Negative.
15	LVDS0_CLK_P	MIPI_DSI_CLK_P	O, DIFF	MIPI_DSI Clock Positive.
16	GND	GND	Power	Ground.
17	LVDS0_TX3_N	MIPI_DSI_DATA3_N	O, DIFF	MIPI_DSI DATA Lane3 Negative.
18	LVDS0_TX3_P	MIPI_DSI_DATA3_P	O, DIFF	MIPI_DSI DATA Lane3 Positive.
19	GND	GND	Power	Ground.
20	GND	GND	Power	Ground.

Important Note: HDMI/LVDS can be supported through iWave's MIPI to HDMI/LVDS Daughter Board.

For more information on daughter board please contact iWave.

REL1.1
Page 40 of 55

2.8.3 Boot Mode Switch

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board supports two position Boot Mode Switch (SW4) to select the boot mode setting of i.MX 8M Mini or i.MX 8M Nano SOC. Boot Mode signals in SODIMM Edge connector is directly connected from Boot Mode Switch. This Boot Mode switch is physically located at the top of the board as shown below.
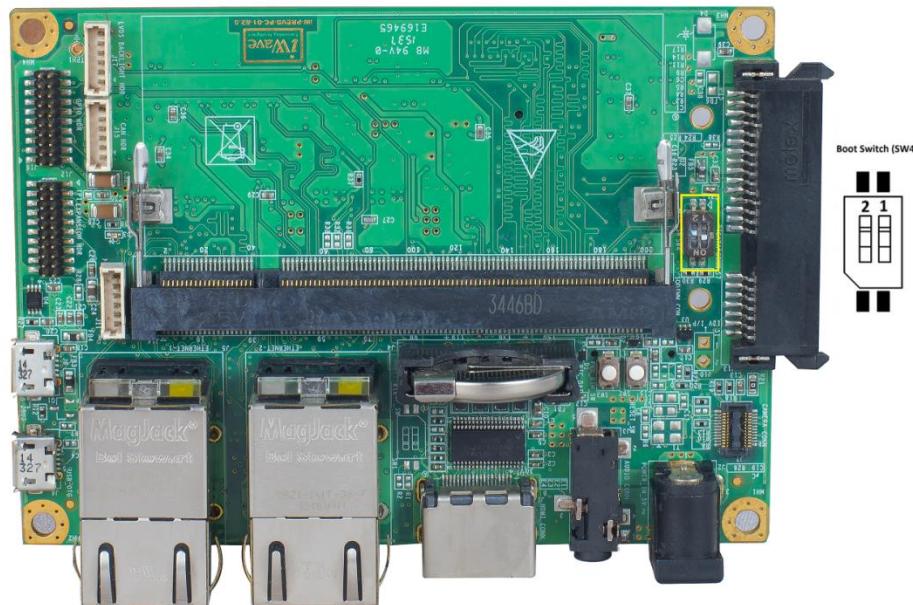

Figure 14: Boot Switch

Table 10: i.MX 8M Mini Boot Mode Settings

Boot Mode Setting of i.MX 8M Mini SOC	Description	SW4 (2 Position Switch)		
		POS1 (BOOT_MODE0)	POS2 (BOOT_MODE1)	Image
Internal Boot Mode (Default)	In this mode, i.MX 8M Mini boot mode is selected by SOC's BOOT_MODE[1:0]Pins.	ON	OFF	
Boot From eFuses	In this mode, i.MX 8M Mini boot media is selected by i.MX 8M Mini eFUSE settings.	ON	ON	
Serial Downloader Mode	In this mode, i.MX 8M Mini boot device can be programmed through its USB OTG interface using UUU Tool.	OFF	ON	

Table 11: i.MX 8M Nano Boot Mode Settings

Boot Mode Setting of i.MX 8M Nano SOC	Description	SW4 (2 Position Switch)		
		POS1 (BOOT_MODE0)	POS2 (BOOT_MODE1)	Image
Boot from internal fuses	In this mode, i.MX 8M Nano boot media is selected by i.MX 8M Nano eFUSE settings.	ON	ON	
eMMC Boot (**default**)	In this mode, i.MX 8M Nano boots from eMMC.	ON	OFF	
Serial Dow nloader Mode	In this mode, i.MX 8M Nano boot device can be programmed through its USB OTG interface using UUU Tool.	OFF	ON	
SD Boot (USDHC2)	In this mode, i.MX 8M Nano boots from SD Card (USDHC2)	OFF	OFF	

2.8.4 Reset Switch

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports Reset Push button switch (SW2) to reset the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM. "n_RST_OUT" signal in SODIMM Edge connector is directly connected from Reset Push button switch. This Reset Push button switch (SW2) is physically located at the top of the board as shown below.

Figure 15: Reset Switch

2.8.5 Power On/Off Switch

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board supports Power On/Off Push button switch (SW3) to power On/Off the SOM. "ON_OFF" signal in SODIMM Edge connector is directly connected from Power On/Off Push button switch which is physically located at the top of the board as shown below.

Figure 16: Power On/Off Switch

When the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM power is On, press Power On/Off Push button for greater than 5s results in a direct hardware SOM power down. When the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM power is Off, press Power On/Off Push button for greater than 750ms results in SOM power up.

2.8.6 JTAG Header

A customized 20-pin ARM JTAG connector is available in i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board for debug purpose. JTAG connector (J18) is physically located at the bottom of the board as shown below.

Figure 17: JTAG Header

Table 12: JTAG Header

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_3V3	O, 3.3V Power	VREF reference Voltage.
2	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	JTAG_TRSTB	I, 3.3V CMOS	JTAG test reset signal. *Note: In SOM this signal is not connected to SODIMM Edge*
4	GND	Power	Ground.
5	JTAG_TDI	I, 3.3V CMOS	JTAG test data Input.
6	GND	Power	Ground.
7	JTAG_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground.
9	JTAG_TCK	I, 3.3V CMOS/ 10K PD	JTAG test clock.
10	GND	Power	Ground.
11	-	10K PD	This pin is connected to ground through 10K pull down resistor.
12	GND	Power	Ground.
13	JTAG_TDO	O, 3.3V CMOS	JTAG test data Output.
14	GND	Power	Ground.
15	PWRON_B	I,3.3V CMOS/ 10K PU	Reset Signal.
16	GND	Power	Ground.
17	NC	-	No Connect.
18	GND	Power	Ground.

19	-	10K PD	This pin is connected to ground through 10K pull down resistor.
20	GND	Power	Ground.

2.8.7 RTC Coin Cell Holder

The i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports RTC coin cell holder (J9) to connect 3V coin cell battery. "VRTC_3V0" power in SODIMM Edge connector is directly connected from RTC coin cell holder to provide backup voltage for i.MX 8M Mini or i.MX 8M Nano SODIMM SOM Real Time Clock. This RTC coin cell holder is physically located at the top of the board as shown below.

Figure 18: RTC Coin Cell Holder

Table 13: RTC Coin Cell Holder Pin Out

Pin No	Pin Name	Signal Type / Termination	Description
1	VRTC_3V0	I, 3V Power	3V RTC coin cell power.
2	VRTC_3V0	I, 3V Power	3V RTC coin cell power.
3	GND	Power	Ground.

2.9   Expansion Header

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports 20pin Expansion Header (J12) for accessing additional IO interfaces like UART, ECSPI, PWM, GPIO interface signals from i.MX 8M Mini or i.MX 8M Nano SOC is available in this header. This Expansion Header (J12) is physically located at the top of the board as shown below.
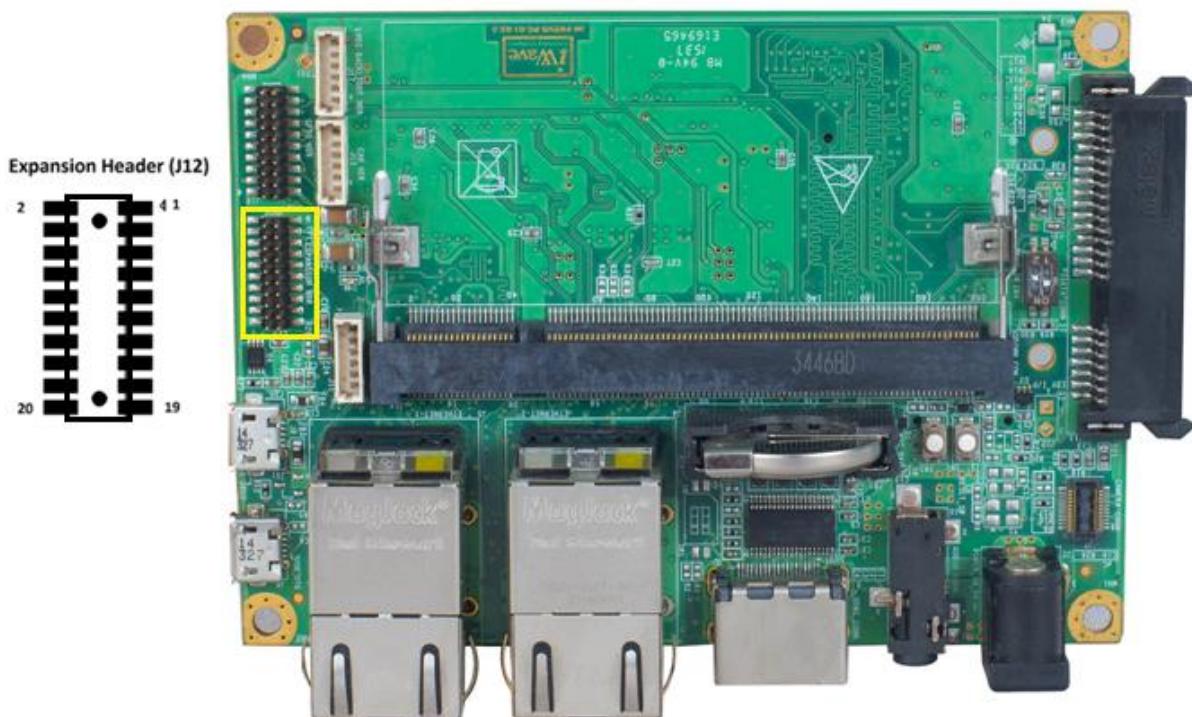
Figure 19: Expansion Header

Table 14: Expansion Header Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	UART1_TXD*	O,3.3V CMOS	UART1 Interface Transmit Signal.
4	UART1_RXD*	I, 3.3V CMOS	UART1 Interface Receive Signal.
5	UART1_RTS_B*	I, 3.3V CMOS	UART1 Interface Ready To Send Signal.
6	UART1_CTS_B*	O,3.3V CMOS	UART1 Interface Clear To Send Signal.
7	SPDIF_RX	I, 3.3V CMOS	Sony/Philips Digital Interface Receive. *Note: This signal is default configured as GPIO. Please refer SOM User Manual for IOMUX Configuration.*
8	SAI1_RXD6 (NC in Nano) [1]	I, 3.3V CMOS	SAI1 Receive Signal 6. *Note: This signal is also used for SOC boot media setting on i.MX 8M Mini SODIMM SOM and no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration*
9	UART3_TXD	O, 3.3V CMOS	UART3 Interface Transmit Signal.
10	UART3_RXD	I, 3.3V CMOS	UART3 Interface Receive Signal.
11	ECSPI1_MISO	O, 3.3V CMOS	ECSPI1 Master In Slave Out.

12	ECSPI1_SS0	I,3.3V CMOS	ECSPI1 Chip Select 0
13	NC	-	NC.
14	NC	-	NC.
15	NC	-	NC.
16	GPIO1_6	IO, 3.3V CMOS	General Purpose Input/Output.
17	NC	-	NC.
18	PWM2_OUT(I2C4_SCL)	O, 3.3V CMOS	PWM2 output
19	GND	Power	Ground.
20	GND	Power	Ground.

Optional feature, by default not supported.

2.10 GPIO Header

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board supports another 20pin Header (J16) for providing additional GPIO pins from the i.MX 8M Mini or i.MX 8M Nano SOC. 4 GPIOs, SAI1 signals (available in Mini only), ECSPI interface signals pins SODIMM Edge is directly connected to this GPIO Header. This GPIO Header (J16) is physically located at the top of the board as shown below.

Figure 20: GPIO Header

Table 15: GPIO Header Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_3V3	O, 3.3 Power	3.3V Supply Voltage.
3	SAI1_TXD1 (NC in Nano) [1]	O,3.3V CMOS	SAI1 Transmit 1.
4	SAI1_TXD2 (NC in Nano) [1]	O,3.3V CMOS	SAI1 Transmit 2.
5	SAI1_TXC (NC in Nano)	IO,3.3V CMOS	General Purpose Input/Output.
6	SAI1_RXD1 (NC in Nano) [1]	I,3.3V CMOS	SAI1 Receive 1.
7	SAI1_RXD3 (NC in Nano) [1]	I,3.3V CMOS	SAI1 Receive 3.
8	SAI1_RXD4 (NC in Nano) [1]	I,3.3V CMOS	SAI1 Receive 4.
9	SAI1_RXC (NC in Nano)	I,3.3V CMOS	General Purpose Input/Output.
10	SAI5_RX_BCLK(SAI5_RXC)	IO, 3.3V CMOS	General Purpose Input/Output.
11	SAI5_RX_SYNC(SAI5_RXFS)	IO, 3.3V CMOS	General Purpose Input/Output.
12	ECSPI1_SCLK	I,3.3V CMOS	ECSPI1 Clock
13	ECSPI1_MOSI	O,3.3V CMOS	ECSPI1 Master Out Slave In
14	USB2_ID	I,3.3V CMOS	USB OTG 2 ID
15	ECSPI3_SS0(UART2_TXD)	O,3.3V CMOS	ECSPI3 Chip Select.
16	ECSPI3_SCLK(UART1_RXD)	O,3.3V CMOS	ECSPI3 Clock.
17	ECSPI3_MOSI(UART1_TXD)	O,3.3V CMOS	ECSPI3 Master Out Slave In.
18	ECSPI3_MISO(UART2_RXD)	I,3.3V CMOS	ECSPI3 Master In Slave Out.
19	GND	Power	Ground.
20	GND	Power	Ground.

. [1]*Important Note: These signals are also used for SOC boot media setting on i.MX 8M Mini SODIMM SOM and no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration.*

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8M Mini or i.MX 8M Nano Carrier Board is designed to work with a +5V external power and uses on board voltage regulators for internal power management. 5V power input from an external power supply is connected to the SODIMM carrier board through Power Jack (J2). This 1.3mm x 3.8mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 1.35mm and an outer dimension of 3.5mm. This connector is physically placed at the top of the board as shown below.
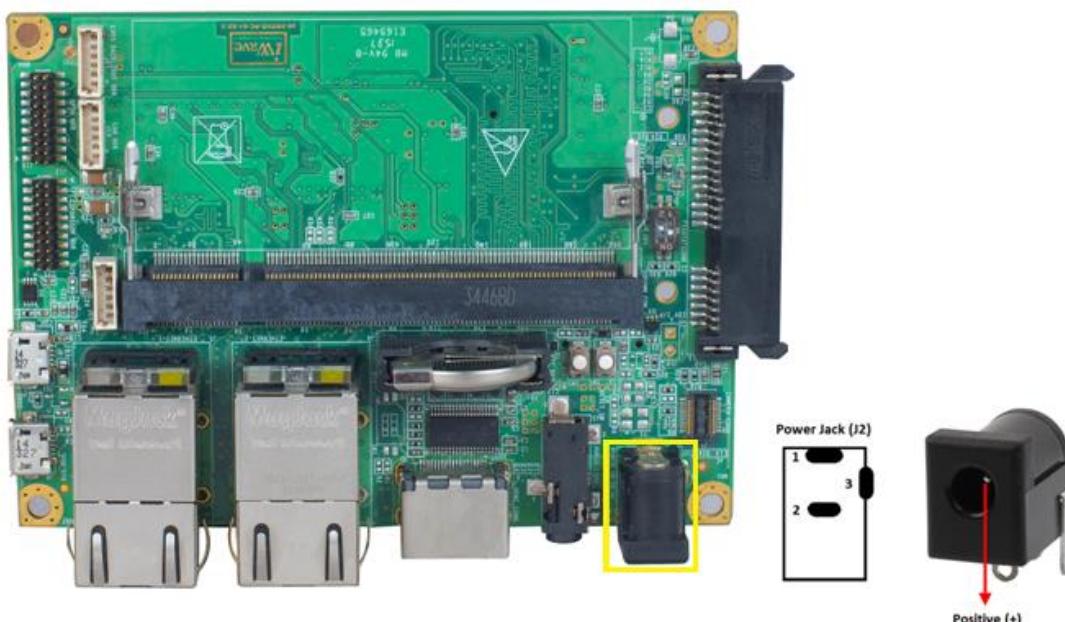

Figure 21: Power Jack

Table 16: Power Jack Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC	5V, Power	Input Supply Voltage.
2	GND	Power	Ground.
3	GND	Power	Ground.

The below table provides the Power Input Requirement of i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board.

Table 17: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20 mV

[1] *i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board is designed to work with 5V, 2.5A input power from External Power Adapter.*

[2] *This voltage is from Coin cell holder and used as backup power source in RTC of i.MX 8M Mini or i.MX 8M Nano SODIMM SOM when VCC is off. This is an optional power and required only if RTC functionality is used.*

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/bootup issues due to reverse current flows. NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.2   Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board.

Table 18: Environmental Specification

Parameters	Min	Max
Operating temperature range (Commercial)[1]	0°C	60°C
Humidity – Operating[2]	10%RH	90%RH

[1] *5V AC Adaptor and Type A Male to Micro B Male cable has lower temperature range. iWave guarantees other component selection for the given operating temperature.*

[2] *To meet this humidity specification, conformal coating needs to be done on the boards. By default, iWave boards doesn't come with conformal coating. Please contact iWave to support conformal coating.*

3.2.2 RoHS Compliance

iWave's i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the board except at an electrostatic free workstation.

3.3   Mechanical Characteristics

3.3.1 i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board Mechanical Dimensions

i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board PCB size is 100mm x 72mm. SODIMM Carrier Board mechanical dimension is shown below.
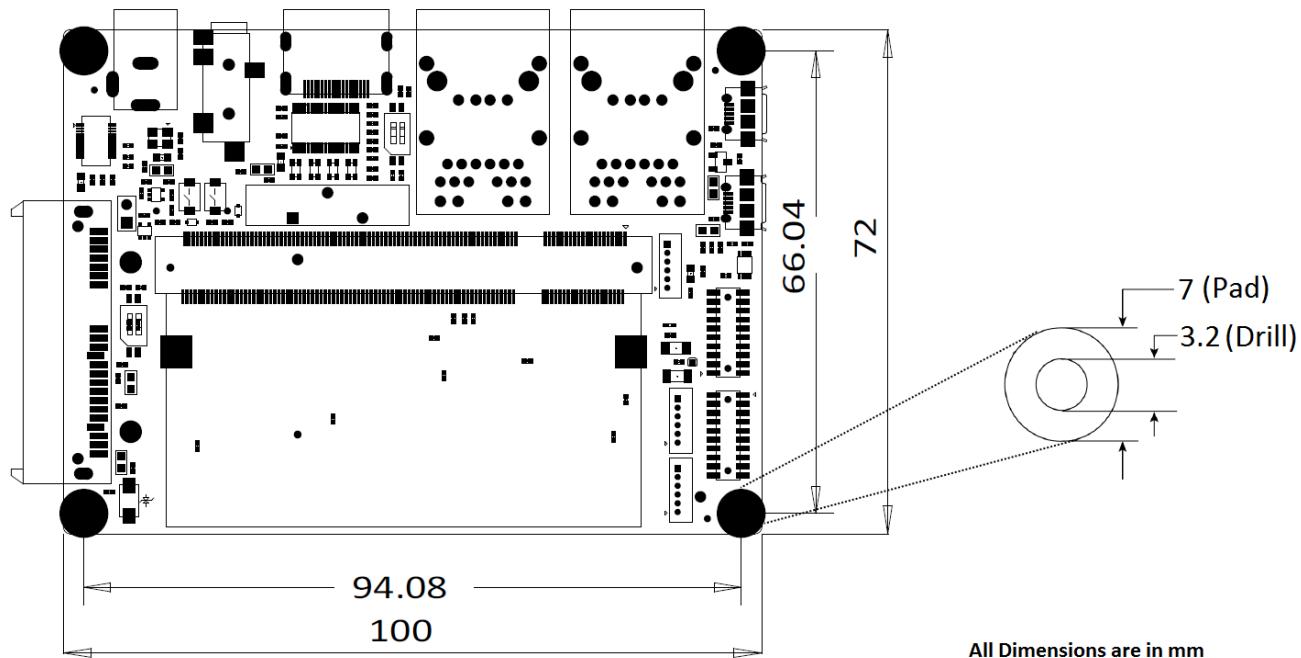

Figure 22: Mechanical dimension of i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board

i.MX 8M Mini or i.MX 8M Nano SODIMM carrier board PCB thickness is 1.6mm±0.1mm, top side maximum height component is Ethernet Jack 1 & 2 (23.24mm) followed by RTC Battery Holder (21.9mm) and bottom side maximum height component is JTAG Header (5mm). Please refer the below figure for height details of the i.MX 8M Mini or i.MX 8M Nano SODIMM Carrier Board.
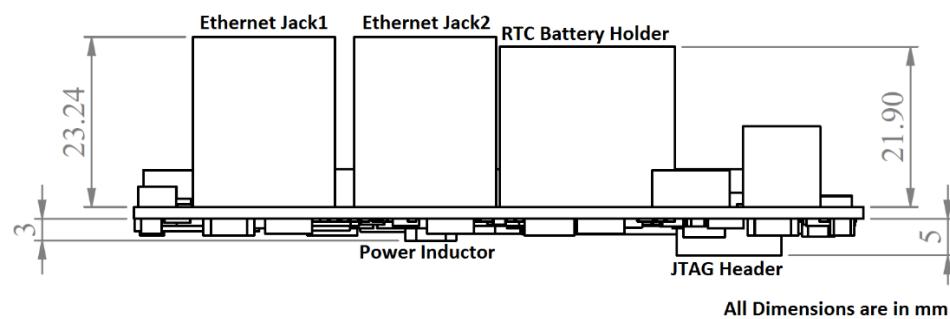

Figure 23: Mechanical dimension of i.MX 8M Mini or i.MX 8M Nano Carrier Board - Side View

4. ORDERING INFORMATION

The below table provides standard orderable part numbers for i.MX 8M Mini Development Platform which includes i.MX 8M Mini SODIMM SOM and SODIMM carrier board.

Table 19: i.MX 8M Mini Orderable Product Part Numbers

Product Part Number	Description	Temperature
i.MX8M Mini Quad SODIMM Development Platform		
iW-G34D-SM04-4L002G-E008G-LCD	i.MX8M Mini Quad, 2GB LPDDR4, 8GB eMMC flash, 2xEthernet, Linux without display.	Commercial
iW-G34D-SM04-4L001G-E008G-LCD	i.MX8M Mini Quad, 1GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit without display	Commercial
iW-G34D-SM02-4L001G-E008G-LCD	i.MX8M Mini Dual, 1GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit without display	Commercial
iW-G34D-SM01-4L001G-E008G-LCD	i.MX8M Mini Solo, 1GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit without display	Commercial

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.

The below table provides standard orderable part numbers for i.MX 8M Nano Development Platform which includes i.MX 8M Nano SODIMM SOM and SODIMM carrier board.

Table 20: i.MX 8M Nano Orderable Product Part Numbers

Product Part Number	Description	Temperature
i.MX8M Nano Quad SODIMM Development Platform		
iW-G37D-SM04-4L002G-E008G-LCB	i.MX8M Nano Quad, 2GB LPDDR4, 8GB eMMC flash, Linux Kit without display	Commercial
iW-G37D-SM04-4L001G-E008G-LCB	i.MX8M Nano Quad 1GB LPDDR4, 8GB eMMC flash, Linux Kit without display	Commercial
iW-G37D-SM02-4L001G-E008G-LCB	i.MX8M Nano Dual, 1GB LPDDR4, 8GB eMMC flash, Linux Kit without display	Commercial
iW-G37D-SM01-4L001G-E008G-LCB	i.MX8M Nano Solo, 1GB LPDDR4, 8GB eMMC flash, Linux Kit without display	Commercial

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.

5. APPENDIX

5.1   Guidelines to insert the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM into Carrier Board

- Make sure that power is not provided to the SODIMM carrier board.

- Insert the SOM module into the socket at a slight angle (approximately 25 degrees) as shown in the below illustration (A). Note that the socket and module are both keyed, which means the module can be installed one way only.

- To seat the module into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the SODIMM socket connector.

- With the module properly seated in the socket, rotate the module downward, as indicated in the illustration (B). Continue pressing the SOM module downward until the clips at each end of the socket lock into position.

- Once the SOM have been installed, Carrier board can be Powered ON with 5V power supply.
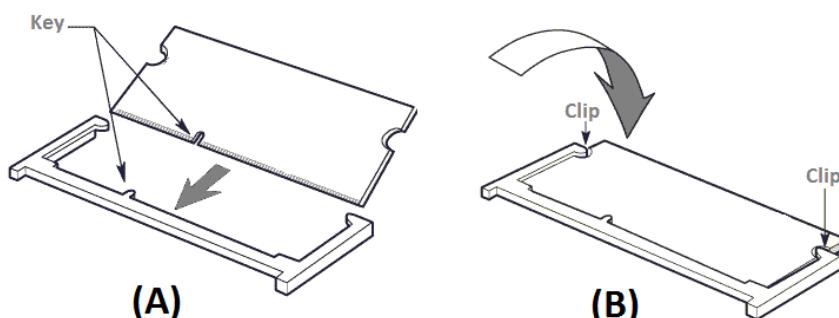

Figure 24: i.MX 8M Mini or i.MX 8M Nano SODIMM Module Insertion procedure

5.2   Guidelines to remove the i.MX 8M Mini or i.MX 8M Nano SODIMM SOM from Carrier board

- Make sure that power is not provided to the Carrier board.

- When you remove the SOM module, pull away the retention clips (A) on each side of the SOM module.

- The module pops up. Grasp the edge of the module (B), and gently pull the module out of the connector
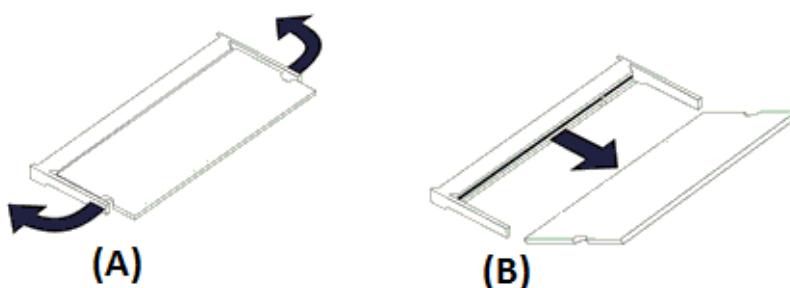

Figure 25: i.MX 8M Mini or i.MX 8M Nano SODIMM Module Removal procedure