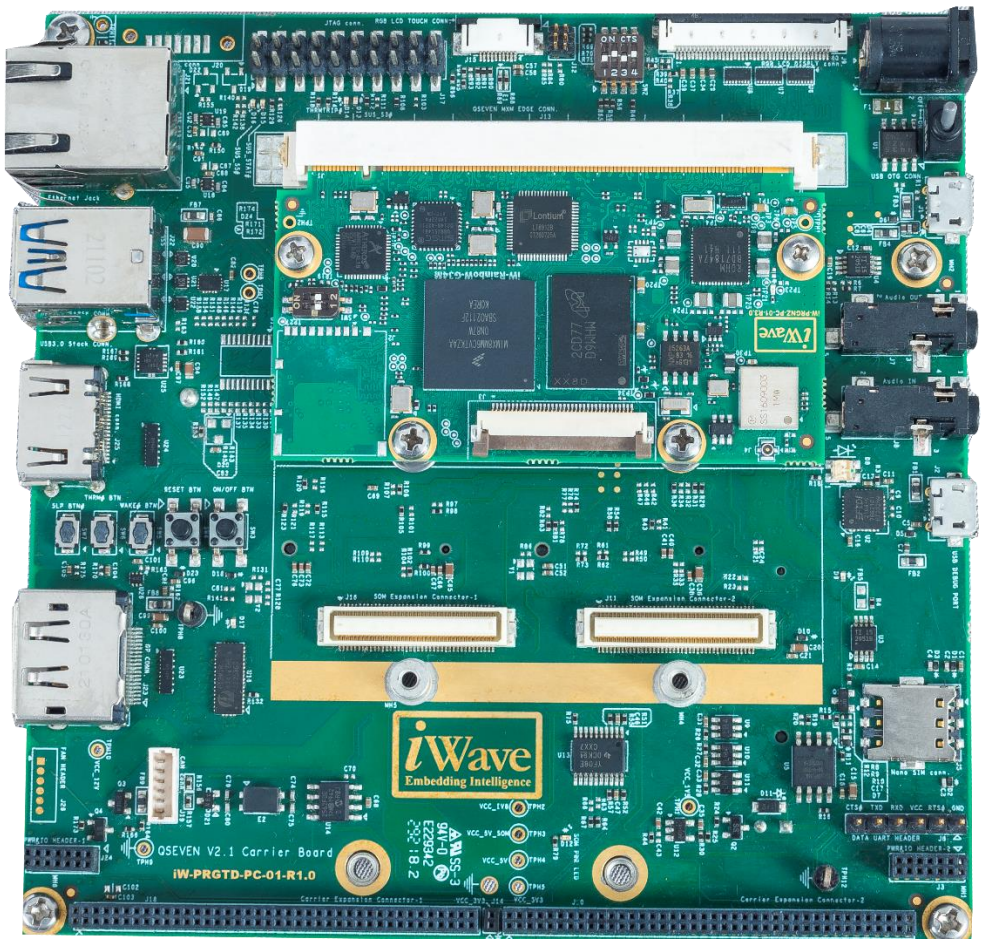
iW-RainboW-G34D/G37D
i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

The i.MX 8M Mini or i.MX 8M Nano µQseven development platform incorporates i.MX 8M Mini or i.MX 8M Nano applications processor based µQseven SOM and Qseven Carrier board for complete validation of i.MX 8M Mini or i.MX 8M Nano SoC functionality. This document is the hardware user guide for the i.MX 8M Mini or i.MX 8M Nano Qseven carrier board. This guide provides detailed information on the overall design and usage of the Qseven carrier board from a hardware system perspective. The details about the i.MX 8M Mini or i.MX 8M Nano µQseven SOM hardware is explained in i.MX 8M Mini or i.MX 8M Nano SOM User Manual document "iW-RainboW-G34M_G37M-i.MX_8M_Mini_Nano-uQseven-SOM-HardwareUserGuide-R3.0-REL1.x.pdf".

1.2 Overview

The µQseven is a versatile small form factor computer Module targeting applications that require low power, low cost and high performance.

iW-RainboW-G34D/G37D Development Platform comes with Qseven Carrier board, and i.MX 8M Mini or i.MX 8M Nano based µQseven SOM. The development board can be used for quick prototyping of various applications targeted by the i.MX 8M Mini or i.MX 8M Nano processor. With the 120mmx120mm Nano ITX size, Qseven carrier board is highly packed with all the necessary on-board connectors to validate the features of i.MX 8M Mini or i.MX 8M Nano µQseven SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BPP	Bits Per Pixel
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signal

Acronyms	Abbreviations
Mbps	Megabits per sec
MHz	Mega Hertz
MSIOF	Clock-Synchronized Serial Interface with FIFO
NC	No Connect
NPTH	Non-Plated Through hole
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PTH	Plated Through hole
PWM	Pulse Width Modulation
RTC	Real Time Clock
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SoC	System on Chip
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
TMDS	Transition-Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.5 References

- IMX8MMIEC_Rev_x.pdf
- IMX8MNIEC_Rev_x.pdf
- Qseven® Specification Version 2.1
- Qseven® Design Guide

2. ARCHITECTURE AND DESIGN – QSEVEN CARRIER BOARD

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform features with high level block diagram and detailed information about each block.

2.1 i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board Block Diagram

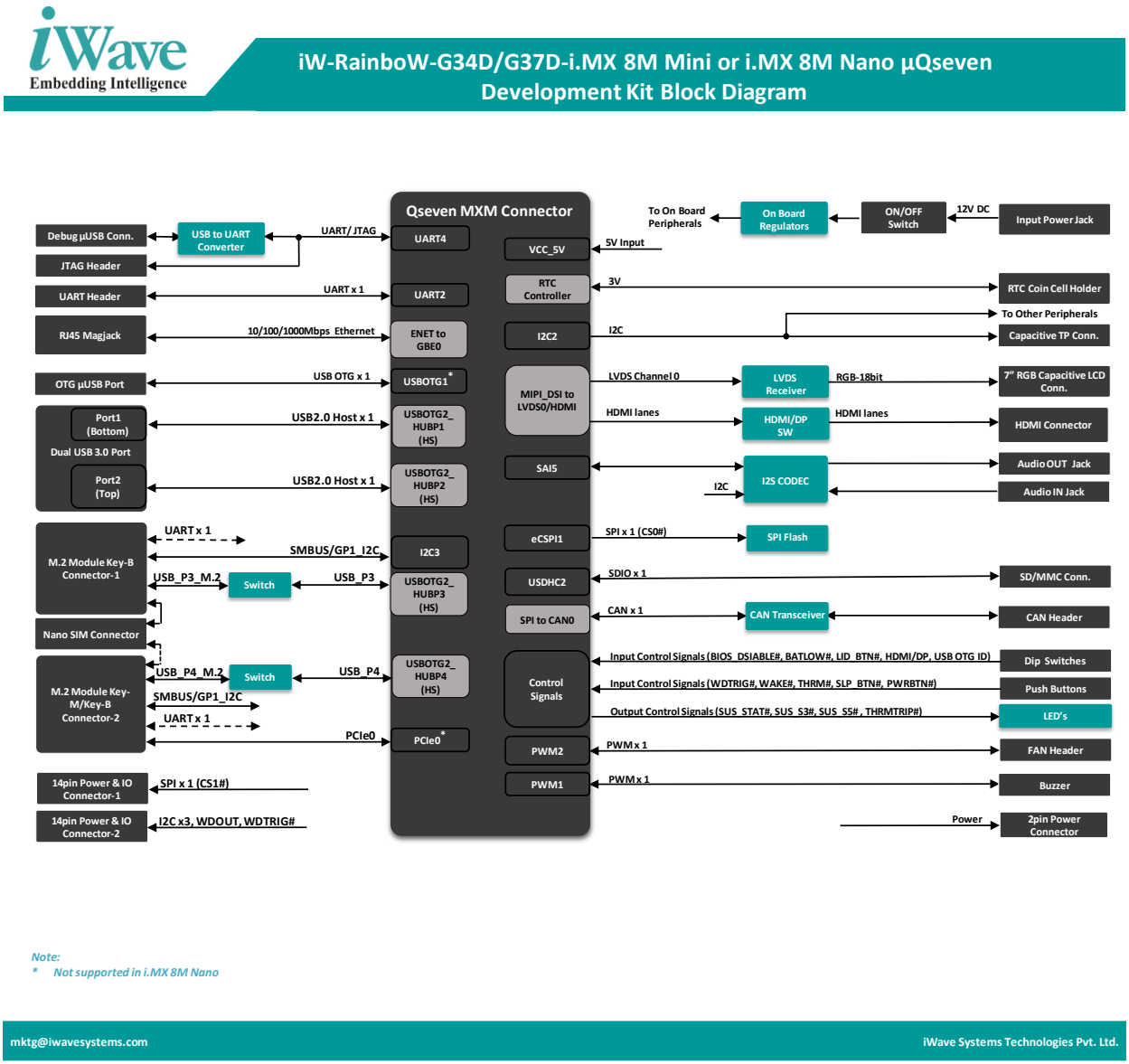


Figure 1: i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform Block Diagram

2.2 i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform Features

i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board supports the following features to support various interfaces from i.MX 8M Mini or i.MX 8M Nano µQseven SOM Edge connector

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header

High Speed Interface Features

- PCIe x 1 Port through M.2 Key-B/Key-M Connector-2[1]

Communication Features

- 10/100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 2 Port through Dual Stack Type A Connector
- USB 2.0 OTG x 1 Port through Micro AB Connector[2]
- SDHI (4bit) x 1 Port through Standard SD Connector
- CAN x 1 Port through Header

Audio/Video Features

- I2S Audio Codec with 3.5mm Audio IN and OUT jack
- 7" RGB LCD Connector through LVDS to RGB transmitter with Capacitive Touch[3]
- HDMI X 1 Port through Type A Connector[3]

Additional Features

- SPI Flash (MSIOF0 with SS#0)
- RTC Coin Cell holder
- Fan Header
- 20-Pin JTAG Header (Optional)[4]

Carrier board Power & IO Headers

- Power & IO Header-1
  - I2C x 2 Ports
  - GPIOs & Power
- Power & IO Header-2
  - SPI (MSIOF0 with SS1#) x 1 Port
  - WDOUT, WDTRIG# & Power

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Form Factor : 120mm X 120mm Nano ITX

[1]*PCIe is not supported in i.MX 8M Nano SoC.*

[2]*In i.MX 8M Nano µQseven SOM, USB2.0 OTG is only supported in Flash mode*

[3]*Either HDMI or LVDS can be supported at a time. By default, HDMI is supported.*

[4]*JTAG connector is supported always in Qseven carrier board hardware. If µQseven SOM supports JTAG interface on Qseven Edge connector, then JTAG can be tested in Qseven carrier board. In i.MX 8M Mini or i.MX 8M Nano SoC based µQseven SOM, JTAG is not supported in Qseven Edge connector by default.*

2.3 Qseven MXM Connector

i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports 230-pin Qseven MXM Edge mating connector for µQseven SOM attachment. This standard 230-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This Qseven MXM Edge mating connector (J13) is physically located at the top of the board as shown below.

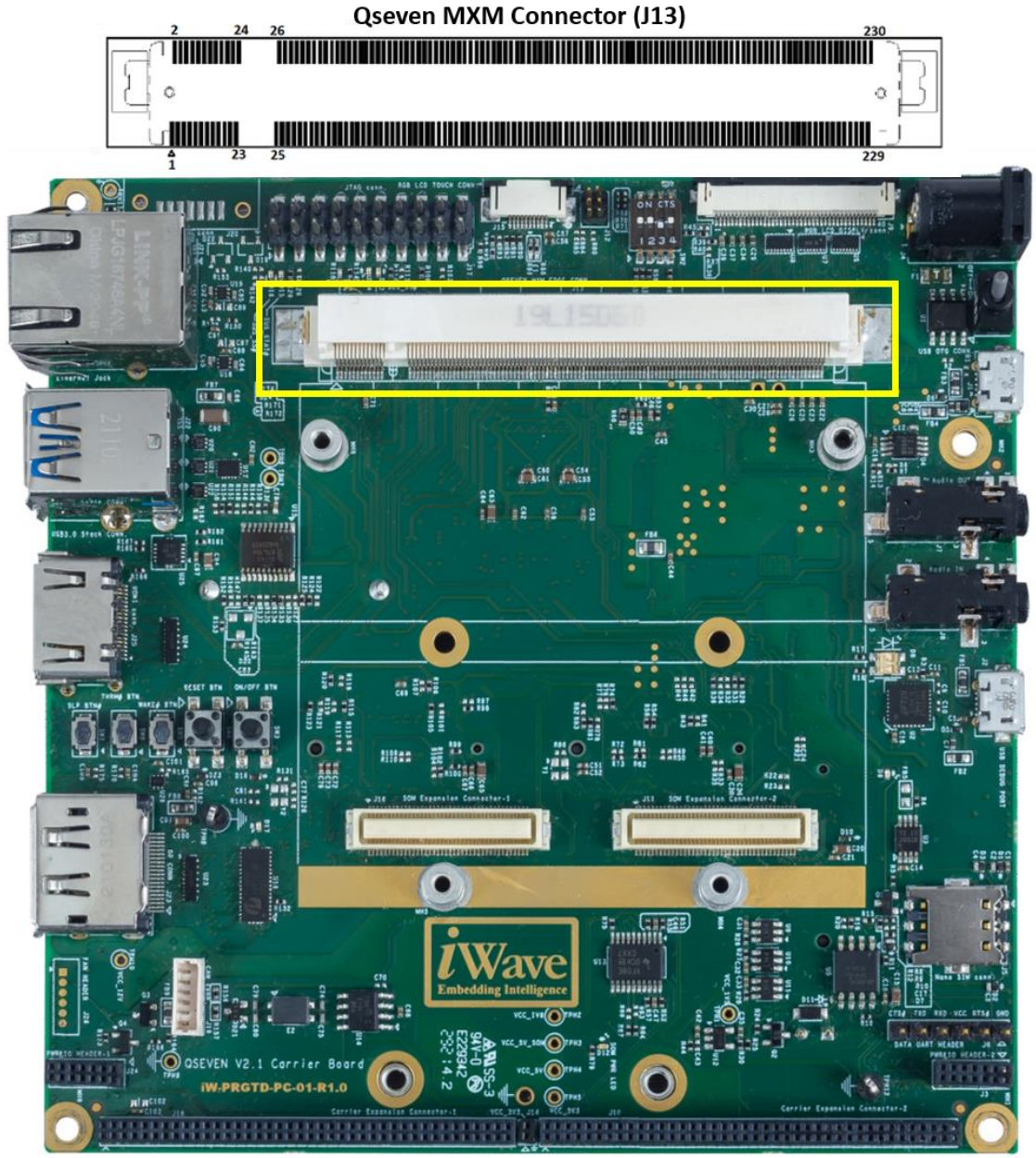


Figure 2: Qseven MXM Connector

Table 3: Qseven MXM Connector Pin Out

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	GND	NA	Power	Ground.
2	GND	GND	NA	Power	Ground.
3	GBE_MDI3-	GPHY_DTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative. This pin is connected to RJ45 Magjack J21.
4	GBE_MDI2-	GPHY_CTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative. This pin is connected to RJ45 Magjack J21.
5	GBE_MDI3+	GPHY_DTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive. This pin is connected to RJ45 Magjack J21.
6	GBE_MDI2+	GPHY_CTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive. This pin is connected to RJ45 Magjack J21.
7	GBE_LINK100#	GPHY_LINK10_100_LED	NA	I, 3.3V CMOS	100 Mbps Ethernet link status LED. This pin is connected to RJ45 Magjack J21.
8	GBE_LINK1000#	GPHY_LINK_1000_LED	NA	I, 3.3V CMOS	1000 Mbps Ethernet link status LED. This pin is connected to RJ45 Magjack J21.
9	GBE_MDI1-	GPHY_BTXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative. This pin is connected to RJ45 Magjack J21.
10	GBE_MDI0-	GPHY_ATXRXM	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative. This pin is connected to RJ45 Magjack J21.
11	GBE_MDI1+	GPHY_BTXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive. This pin is connected to RJ45 Magjack J21.
12	GBE_MDI0+	GPHY_ATXRXP	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to RJ45 Magjack J21.
13	GBE_LINK#	GPHY_LINK_1000_LED	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED. This pin is connected to indication LED D24.
14	GBE_ACT#	GPHY_ACT_LED	NA	I, 3.3V CMOS	Gigabit Ethernet Activity status LED. This pin is connected to RJ45 Magjack J21.
15	GBE_CTREF	VDVDH_GPHY1	NA	Power	This pin is connected to RJ45 Magjack J21 centre tap pins through resistor and default populated in carrier board.
16	SUS_S5#	SUS_S5_Q7	NA	I, 3.3V CMOS	S5 State. This pin is connected to indication LED D16.
17	WAKE#	NC	NA	NA	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. *Note:This pin is connected to Push button (SW5) in carrier board.*
18	SUS_S3#	SUS_S3_Q7	NA	I, 3.3V CMOS	S3 state. This pin is connected to indication LED D13 and to enable carrier board power.
19	SUS_STAT#	GPIO_SD1_LED(GPIO5_27)	UART3_TXD/ D18	I, 3.3V CMOS	Suspend Status. This pin is connected to indication LED D15.
20	PWRBTN#	PWRBTN#	ONOFF/A25	O, 3.3V CMOS	Power Button output. This pin is connected to Push button (SW3) in the carrier board used for SOM On/Off control.
21	GPII1	GPII_1	NA	O, 3.3V CMOS	This pin is connected to Push button (SW7) in carrier board. P5 Output of SOM I/O Expander

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
22	GPII0	GPII_0	NA	O, 3.3V CMOS	This pin is connected from 8bit DIP switch (SW2) 3rd position in carrier board. P4 Output of SOM I/O Expander
23	GND	GND	NA	Power	Ground.
24	GND	GND	NA	Power	Ground.
25	GND	GND	NA	Power	Ground.
26	PWGIN	PWRGIN	NA	O, 5V CMOS/ 10K PU	Power Good Output.
27	GPII2	GPII_2	NA	O, 3.3V CMOS	This pin is connected from 8bit DIP switch (SW2)2nd position in carrier board. P6 Output of SOM I/O Expander
28	RSTBTN#	RSTBN	NA	O, 3.3V CMOS	Active low Reset button Output. This pin is connected to Push button SW4 in carrier board for reset generation.
29	SATA0_TX+	NC	NA	-	NC.
30	SATA1_TX+	NC	NA	-	NC.
31	SATA0_TX-	NC	NA	-	NC.
32	SATA1_TX-	NC	NA	-	NC.
33	SATA_ACT#	NC	NA	-	NC.
34	GND	GND	NA	Power	Ground.
35	SATA0_RX+	NC	NA	-	NC.
36	SATA1_RX+	NC	NA	-	NC.
37	SATA0_RX-	NC	NA	-	NC.
38	SATA1_RX-	NC	NA	-	NC.
39	GND	GND	NA	Power	Ground.
40	GND	GND	NA	Power	Ground.
41	BIOS_DISABLE#/ BOOT_ALT#	NC	NA	-	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. This pin is connected from 8bit DIP switch (SW2)1st position in carrier board.
42	SDIO_CLK#	SD2_CLK	SD2_CLK/W23	I, 3.3V CMOS	SD2 Clock. This pin is connected to SD/MMC connector (J28).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
43	SDIO_CD#	SD2_CD	SD2_CD_B/AA26	O, 3.3V CMOS	SD2 Card Detect. This pin is connected from SD/MMC connector (J28).
44	RSVD1	NC	NA	I, 3.3V CMOS	Reserved. By default, NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM This pin is connected to Power & IO Header-2 (J3).
45	SDIO_CMD	SD2_CMD	SD2_CMD/W24	IO,3.3VCMOS	SD2command. This pin is connected to SD/MMC connector (J28).
46	SDIO_WP	GPIO_SD2_WP(GPIO5_26)	UART3_RXD/E18	O, 3.3V CMOS/ 10K PU	SD2 Write Protect. This pin is connected to SD/MMC connector (J28).
47	SDIO_PWR#	GPIO_SD1_PWR(GPIO1_01)	GPIO1_IO01/AF14	I, 3.3V CMOS/ 10K PD	SD/MMC Interface Power Enable. This pin is used control the power input to the SD/MMC connector (J28).
48	SDIO_DAT1	SD2_DATA1	SD2_DATA1/AB24	IO, 3.3V CMOS	SD2 Data1. This pin is connected to SD/MMC connector (J28).
49	SDIO_DAT0	SD2_DATA0	SD2_DATA0/AB23	IO, 3.3V CMOS	SD2 Data0. This pin is connected to SD/MMC connector (J28).
50	SDIO_DAT3	SD2_DATA3	SD2_DATA3/V23	IO, 3.3V CMOS	SD2 Data3. This pin is connected to SD/MMC connector (J28).
51	SDIO_DAT2	SD2_DATA2	SD2_DATA2/V24	IO, 3.3V CMOS	SD2 Data2. This pin is connected to SD/MMC connector (J28).
52	SDIO_DAT5	NC	NA	-	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
53	SDIO_DAT4	NC	NA	-	NC in i.MX 8M Mini ori.MX 8M Nano µQseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
54	SDIO_DAT7	NC	NA	-	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
55	SDIO_DAT6	NC	NA	-	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM. This pin is connected to SD/MMC connector (J28) in carrier board.
56	USB_DRIVE_VBUS	USB1_OTG_PWR(GPIO1_12)	USB1_OTG_PWR(GPIO1_IO12)/AB10	I, 3.3V CMOS	USB OTG Power enable.
57	GND	GND	NA	Power	Ground.
58	GND	GND	NA	Power	Ground.
59	HDA_SYNC/ I2S_WS	SAI5_TX_SYNC(SAI5_RXD1)	SAI5_TX_SYNC(SAI5_RXD1)/AC14	I, 3.3V CMOS	SAI Audio transmit frame synchronization. This pin is connected to I2S audio codec.
60	SMB_CLK/ GP1_I2C_CLK	I2C3_SCL	I2C3_SCL/E10	I, 3.3V OD	I2C3 clock. This pin is connected to M.2 Key-B Connector-1, M.2 Key-B/Key-M Connector-2 and Power & IO Header-1 (J24) 2ndPin.
61	HDA_RST#/ I2S_RST#	GPIO_RESET(GPIO5_2)	GPIO5_IO2(SAI3_MCLK)/AD6	I, 3.3V CMOS/ 10K PU	Audio Codec Reset. This pin is connected to Capacitive Touch Connector for touch reset.
62	SMB_DAT/ GP1_I2C_DAT	I2C3_SDA	I2C3_SDA/F10	IO, 3.3V OD	This pin is connected to M.2 Key-B Connector-1, M.2 Key-B/Key-M Connector-2 and Power & IO Header-1 (J24) 4thPin.
63	HDA_BCLK/ I2S_CLK	SAI5_TX_BCLK(SAI5_RXD2)	SAI5_TX_BCLK(SAI5_RXD2)/AD13	O, 3.3V CMOS	SAI Audio transmit clock. This pin is connected from I2S audio codec.
64	SMB_ALERT#	SMB_ALERT_B(GPIO1_15)	USB2_OTG_OC(GPIO1_IO15)/AB9	-	This pin is connected to M.2 Key-B Connector-1 (J33) & Optionally connected to M.2 Key-B/Key-M Connector-2(J31)

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
65	HDA_SDI/ I2S_SDI	SAI5_RX_DATA0(SAI5_RXD0)	SAI5_RX_DATA0(SAI5_RXD0)/AD18	I, 3.3V CMOS	SAI Audio Receive Data. This pin is connected to I2S audio codec.
66	GP0_I2C_CLK	I2C2_SCL	I2C2_SCL/D10	I, 3.3V OD	I2C2 clock. This pin is connected to I2S Audio Codec, Capacitive touch connector and IO Expander.
67	HDA_SDO/ I2S_SDO	SAI5_TX_DATA0(SAI5_RXD3)	SAI5_TX_DATA0(SAI5_RXD3)/AC13	O, 3.3V CMOS	SAI Audio Transmit Data. This pin is connected from I2S audio codec.
68	GP0_I2C_DAT	I2C2_SDA	I2C2_SDA/D9	IO, 3.3V OD	I2C2 Data. This pin is connected to I2S Audio Codec, Capacitive touch connector and IO Expander.
69	THRM#	THRM#	ONOFF / A25	O, 3.3V CMOS	This pin is connected from Push button (SW6) in carrier board.
70	WDTRIG#	Q7_WDTRIG_B	NA	-	This pin is connected to Expansion connector2 (J3) 11th pin in carrier board.
71	THRMTRIP#	GPIO_THRMTRIP_Q7(GPIO1_14)	USB2_OTG_PWR(GPIO1_IO14)/AC9	O, 3.3V CMOS	Thermal trip. This pin is connected to indication LED D14.
72	WDOUT	Q7_WDOG_B	NA	-	This pin is connected to Expansion connector2 (J3) 9th Pin in carrier board.
73	GND	GND	NA	Power	Ground.
74	GND	GND	NA	Power	Ground.
75	USB_P7-/ USB_SSTX0-	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
76	USB_P6-/ USB_SSRX0-	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
77	USB_P7+/ USB_SSTX0+	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
78	USB_P6+/ USB_SSRX0+	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
79	USB_6_7_OC#	NC	NA	-	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
80	USB_4_5_OC#	USB_HUB4_OC	NA	O, 3.3V CMOS	This pin is connected to USB3.0 Host Port1 Over

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					current indicator in carrier board.
81	USB_P5-/ USB_SSTX1-	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
82	USB_P4-/ USB_SSRX1-	USB_HUB4OUT_DM	NA	IO, DIFF	USB 2.0 Host Port4 Data negative. This pin is connected to Mini PCIe Connector through a USB switch.
83	USB_P5+/ USB_SSTX1+	NC	NA	IO, DIFF	NC in i.MX 8M Mini or i.MX 8M Nano µQseven SOM
84	USB_P4+/ USB_SSRX1+	USB_HUB4OUT_DP	NA	IO, DIFF	USB 2.0 Host Port4 Data positive. This pin is connected to Mini PCIe Connector through a USB switch.
85	USB_2_3_OC#	USB_HUB2_OC&USB_ HUB3_OC	NA	O, 3.3V CMOS	Over current sense signal for USB Host Port2 and Port3. This pin is connected from USB Host Port2 Over current indicator.
86	USB_0_1_OC#	USB1_OTG_OC(GPIO1 _13)&USB_HUB1_OC	USB1_OTG_ OC(GPIO1_I O13)/AD9	O, 3.3V CMOS/ 10K PU	Over current sense signal for USB Host Port0 and OTG Port1. This pin is connected from HostPort0 and USB OTG Port1Over current indicator.
87	USB_P3-	USB_HUB3OUT_DM	NA	IO, DIFF	USB 2.0 Host Port3 Data negative. This pin is connected to Dual stack USB3.0 TypeA connector (J22) top port in carrier board (from the USB HUB output port3 of the i.MX 8M Mini or i.MX 8M Nano SOM).
88	USB_P2-	USB_HUB2OUT_DM	NA	IO, DIFF	USB 2.0 Host Port2 Data negative. This pin is connected to Dual stack USB3.0 TypeA

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					connector (J22) bottom port.
89	USB_P3+	USB_HUB3OUT_DP	NA	IO, DIFF	USB 2.0 Host Port3 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J22) top port in carrier board (from the USB HUB output port3 of the i.MX 8M Mini or i.MX 8M Nano SOM).
90	USB_P2+	USB_HUB2OUT_DP	NA	IO, DIFF	USB 2.0 Host Port2 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J22) bottom port.
91	USB_VBUS	USB_OTG1_VBUS	USB1_VBUS/ F22	O, 5V Power	Reference voltage to USB controller.
92	USB_ID	USB_ID	USB1_ID/D2 2	O, 3.3V CMOS	USB OTG ID. This pin is connected from Micro USB OTG connector (J1).
93	USB_P1-	USB1_DN	USB1_DN/A2 2	IO, DIFF	USB 2.0 OTG Port1 Data negative. This pin is connected to Micro USB OTG connector (J1).
94	USB_P0-	USB_HUB1OUT_DM	NA	IO, DIFF	USB 2.0 Host Port0 Data negative. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1of the i.MX 8M Mini or i.MX 8M Nano SOM).
95	USB_P1+	USB1_DP	USB1_DP/B2 2	IO, DIFF	USB 2.0 OTG Port1 Data positive. This pin is connected to Micro USB OTG connector (J1).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
96	USB_P0+	USB_HUB1OUT_DP	NA	IO, DIFF	USB 2.0 Host Port0 Data positive. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1of the i.MX 8M Mini or i.MX 8M Nano SOM).
97	GND	GND	NA	Power	Ground.
98	GND	GND	NA	Power	Ground.
99	eDP0_TX0+/ LVDS_A0+	LVDS_CH0_P	NA	I, DIFF LVDS	LVDS primary channel differential pair0 positive. This pin is connected to LVDS Receiver.
100	eDP1_TX0+/ LVDS_B0+	NC	NA	I, DIFF LVDS	NC
101	eDP0_TX0-/ LVDS_A0-	LVDS_CH0_N	NA	I, DIFF LVDS	LVDS primary channel differential pair0 negative. This pin is connected to LVDS Receiver.
102	eDP1_TX0-/ LVDS_B0-	NC	NA	I, DIFF LVDS	NC.
103	eDP0_TX1+/ LVDS_A1+	LVDS_CH1_P	NA	I, DIFF LVDS	LVDS primary channel differential pair1 positive. This pin is connected to LVDS Receiver.
104	eDP1_TX1+/ LVDS_B1+	NC	NA	I, DIFF LVDS	NC.
105	eDP0_TX1-/ LVDS_A1-	LVDS_CH1_N	NA	I, DIFF LVDS	LVDS primary channel differential pair1 negative. This pin is connected to LVDS Receiver.
106	eDP1_TX1-/ LVDS_B1-	NC	NA	I, DIFF LVDS	NC.
107	eDP0_TX2+/ LVDS_A2+	LVDS_CH2_P	NA	I, DIFF LVDS	LVDS primary channel differential pair2 positive. This pin is connected to LVDS Receiver.
108	eDP1_TX2+/ LVDS_B2+	NC	NA	I, DIFF LVDS	NC.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
109	eDP0_TX2-/ LVDS_A2-	LVDS_CH2_N	NA	I, DIFF LVDS	LVDS primary channel differential pair2 negative. This pin is connected to LVDS Receiver.
110	eDP1_TX2-/ LVDS_B2-	NC	NA	I, DIFF LVDS	NC.
111	LVDS_PPEN	GPIO_LVDS_PPEN(GPIO5_04)	SPDIF_RX/ AG9	I, 3.3V CMOS/ 10K PU	LCD Panel Power Enable.
112	LVDS_BLEN	GPIO_LVDS_BLEN(GPIO5_05)	SPDIF_EXT_CLK/ AF8	I, 3.3V CMOS/ 10K PU	LCD Panel Backlight Enable Control.
113	eDP0_TX3+/ LVDS_A3+	LVDS_CH3_P	NA	I, DIFF LVDS	LVDS primary channel differential pair3 positive. This pin is connected to LVDS Receiver.
114	eDP1_TX3+/ LVDS_B3+	NC	NA	I, DIFF LVDS	NC.
115	eDP0_TX3-/ LVDS_A3-	LVDS_CH3_N	NA	I, DIFF LVDS	LVDS primary channel differential pair3 negative. This pin is connected to LVDS Receiver.
116	eDP1_TX3-/ LVDS_B3-	NC	NA	I, DIFF LVDS	NC.
117	GND	GND	NA	Power	Ground.
118	GND	GND	NA	Power	Ground.
119	eDP0_AUX+/ LVDS_A_CLK+	LVDS_CLK_P	NA	I, DIFF LVDS	LVDS primary channel differential Clock positive. This pin is connected to LVDS Receiver.
120	eDP1_AUX+/ LVDS_B_CLK+	NC	NA	I, DIFF LVDS	NC.
121	eDP0_AUX-/ LVDS_A_CLK-	LVDS_CLK_N	NA	I, DIFF LVDS	LVDS primary channel differential Clock negative. This pin is connected to LVDS Receiver.
122	eDP1_AUX-/ LVDS_B_CLK-	NC	NA	I, 1.8V LVDS	NC.
123	LVDS_BLT_CTRL /GP_PWM_OUT0	GPIO_LVDS_BLT_CTRL (GPIO5_03)	SPDIF_TX/AF9	I, 3.3V CMOS/ 10K PU	LCD Panel Backlight Control.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
124	GP_1-Wire_Bus	GP_1_WB	NA	IO, 3.3V CMOS	This pin is connected to CEC pin of HDMI connector (J25) in carrier board.
125	GP2_I2C_DAT/LVDS_DID_DAT	I2C2_SDA	I2C2_SDA/D9	IO, 3.3V OD	I2C2 Data. This pin is directly connected to Power & IO Header-1 (J24) 1st Pin in carrier board.
126	eDP0_HPD#/LVDS_BLC_DAT	NC	NA	-	NC
127	GP2_I2C_CLK/LVDS_DID_CLK	I2C2_SCL	I2C2_SCL/D10	I, 3.3V OD	I2C2 Clock. This pin is directly connected to Power & IO Header-1 (J24) 3rd Pin in carrier board.
128	eDP1_HPD#/LVDS_BLC_CLK	NC	NA	-	NC
129	CAN0_TX	CAN0_TX	NA	I,3.3V CMOS	Transmit input for CAN0 bus. This pin is connected to CAN0 Transceiver.
130	CAN0_RX	CAN0_RX	NA	O, 3.3V CMOS	Receive output for CAN0 bus. This pin is connected fromCAN0 Transceiver.
131	DP_LANE3+/TMDS_CLK+	HDMI_CLKP	NA	I, TMDS	HDMI differential data lane clock positive. This pin is connected to HDMI connector (J25) in carrier board.
132	USB_SSTX1-	NC	NA	-	NC
133	DP_LANE3-/TMDS_CLK-	HDMI_CLKM	NA	I, TMDS	HDMI differential data clock negative. This pin is connected to HDMI connector (J25) in carrier board.
134	USB_SSTX1+	NC	NA	-	NC
135	GND	GND	NA	Power	Ground.
136	GND	GND	NA	Power	Ground.
137	DP_LANE1+/TMDS_LANE1+	HDMI_D1P	NA	I, TMDS	HDMI differential data lane 1 positive.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to HDMI connector (J25) in carrier board.
138	DP_AUX+	NC	NA	-	NC
139	DP_LANE1-/ TMDS_LANE1-	HDMI_D1M	NA	I, TMDS	HDMI differential data lane 1 negative. This pin is connected to HDMI connector (J25) in carrier board.
140	DP_AUX-	NC	NA	-	NC
141	GND	GND	NA	Power	Ground.
142	GND	GND	NA	Power	Ground.
143	DP_LANE2+/ TMDS_LANE0+	HDMI_D0P	NA	I, TMDS	HDMI differential data lane 0 positive. This pin is connected to HDMI connector (J25) in carrier board.
144	RSVD	NC	NA	-	NC
145	DP_LANE2-/ TMDS_LANE0-	HDMI_D0M	NA	I, TMDS	HDMI differential data lane 0 negative. This pin is connected to HDMI connector (J25) in carrier board.
146	RSVD	NC	NA	-	NC
147	GND	GND	NA	Power	Ground.
148	GND	GND	NA	Power	Ground.
149	DP_LANE0+/ TMDS_LANE2+	HDMI_D2P	NA	I, TMDS	HDMI differential data lane 2 positive. This pin is connected to HDMI connector (J25) in carrier board.
150	HDMI_CTRL_DAT	I2C3_SDA	I2C3_SDA/F10	IO, 3.3V OD	HDMI I2C Data. This pin is connected to HDMI connector (J25) in carrier board.
151	DP_LANE0-/ TMDS_LANE2-	HDMI_D2M	NA	I, TMDS	HDMI differential data lane 2 negative. This pin is connected to HDMI connector (J25) in carrier board.
152	HDMI_CTRL_CLK	I2C3_SCL	I2C3_SCL/E10	I, 3.3V OD	HDMI I2C Clock.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to HDMI connector (J25) in carrier board.
153	DP_HDMI_HPD#	HDMI_HPD	NA	O, 3.3V CMOS	HDMI hot plug detect. This pin is connected to HDMI connector (J25) in carrier board.
154	RSVD	NC	NA	-	NC
155	PCIE_CLK_REF+	PCIE_REFCLK_DP[1]	NA	I, DIFF	PCIe differential reference clock positive. This pin is connected to M.2 Key-B/Key-M connector (J31).
156	PCIE_WAKE#	PCIe_WAKE_B(GPIO1_10)	GPIO1_IO10/ AD10	O, 3.3V CMOS/ 10K PU	PCIe wake event. This pin is connected to M.2 Key-B/Key-M connector (J31).
157	PCIE_CLK_REF-	PCIE_REFCLK_DM[1]	NA	I, DIFF	PCIe differential reference clock negative. This pin is connected to M.2 Key-B/Key-M connector (J31).
158	PCIE_RST#	PCIe_RST(GPIO1_11)	GPIO1_IO11/ AC10	I, 3.3V CMOS	PCIe reset. This pin is connected to M.2 Key-B/Key-M connector (J31).
159	GND	GND	NA	Power	Ground.
160	GND	GND	NA	Power	Ground.
161	PCIE3_TX+	NC	NA	-	NC
162	PCIE3_RX+	NC	NA	-	NC
163	PCIE3_TX-	NC	NA	-	NC
164	PCIE3_RX-	NC	NA	-	NC
165	GND	GND	NA	Power	Ground.
166	GND	GND	NA	Power	Ground.
167	PCIE2_TX+	NC	NA	-	NC
168	PCIE2_RX+	NC	NA	-	NC
169	PCIE2_TX-	NC	NA	-	NC
170	PCIE2_RX-	NC	NA	-	NC
171	UART0_TX	UART2_TX(SAI3_TXC)	UART2_TX(SAI3_TXC)/ AG6	I, 3.3V CMOS	UART2 interface serial data transmitter.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to Data UART Header (J6) 05th Pin.
172	UART0_RTS#	UART2_CTS_B(SAI3_RXC)	UART2_CTS_B(SAI3_RXC)/ AG7	I, 3.3V CMOS	UART2 interface ready to receive handshake signal. This pin is connected to Data UART Header (J6) 06th Pin.
173	PCIE1_TX+	NC	NA	-	NC
174	PCIE1_RX+	NC	NA	-	NC
175	PCIE1_TX-	NC	NA	-	NC
176	PCIE1_RX-	NC	NA	-	NC
177	UART0_RX	UART2_RX(SAI3_TXFS)	UART2_RX(SAI3_TXFS)/ AC6	O, 3.3V CMOS	UART2 interface serial data receiver. This pin is connected from Data UART Header (J6) 04th Pin.
178	UART0_CTS#	UART2_RTS_B(SAI3_RXD)	UART2_RTS_B(SAI3_RXD) / AF7	O, 3.3V CMOS	UART2 interface ready to send handshake signal. This pin is connected from Data UART Header (J6) 02nd Pin.
179	PCIE0_TX+	PCIE_TXP[1]	PCIE_TXN_P/ B20	I, DIFF	PCIe Channel0 Transmit data output positive. This pin is connected to M.2 Key-B/Key-M Connector(J31).
180	PCIE0_RX+	PCIE_RXP[1]	PCIE_RXN_P/ B19	O, DIFF	PCIe Channel0 Receive data input positive. This pin is connected to M.2 Key-B/Key-M Connector(J31).
181	PCIE0_TX-	PCIE_TXN[1]	PCIE_TXN_N / A20	I, DIFF	PCIe Channel0 Transmit data output negative. This pin is connected to M.2 Key-B/Key-M Connector(J31).
182	PCIE0_RX-	PCIE_RXN[1]	PCIE_RXN_N / A19	O, DIFF	PCIe Channel0 Receive data input negative. This pin is connected to M.2 Key-B/Key-M Connector(J31).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
183	GND	GND	NA	Power	Ground.
184	GND	GND	NA	Power	Ground.
185	LPC_AD0/ GPIO0	Q7_GPIO0(GPIO5_22)	ECSPI3_SCLK (UART1_RXD)/ E14	IO,3.3VCMOS/ 10K PU	General purpose Input/Output0. This GPIO is used for Touch Interrupt and connected from Capacitive Touch Connector or Resistive Touch Controller.
186	LPC_AD1/ GPIO1	Q7_GPIO1(GPIO1_05)	GPIO1_IO05/ AF12	IO,3.3VCMOS/ 10K PU	General purpose Input/Output1. This pin is connected to M.2 Key-B/Key M Connector (J31) and M.2 Key-B Connector (J33).
187	LPC_AD2 / GPIO2	Q7_GPIO2(GPIO5_23)	ECSPI3_MOS I(UART1_TXD)/ F13	IO,3.3VCMOS/ 10K PU	General purpose Input/Output2. This GPIO is used for Mic Input Detect and connected from Audio IN Jack.
188	LPC_AD3/ GPIO3	Q7_GPIO3(GPIO1_06)	GPIO1_IO06/ AG11	IO,3.3VCMOS/ 10K PU	General purpose Input/Output3. This GPIO is used for Headphone Detect and connected from Audio Out Jack.
189	LPC_CLK/ GPIO4	Q7_GPIO4(GPIO5_24)	ECSPI3_MIS O(UART2_RX D)/ F15	IO, 3.3V CMOS	General purpose Input/Output4. This GPIO is used for CAN0 Transceiver Power down control and connected to CAN transceiver.
190	LPC_FRAME#/ GPIO5	Q7_GPIO5(GPIO1_07)	GPIO1_IO07/ AF11	IO,3.3VCMOS/ 10K PU	General purpose Input/Output5. This pin is connected to M.2 Key-B Connector (J33) and optionally connected to M.2 Key-B/Key-M Connector(J31).

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
191	SERIRQ / GPIO6	Q7_GPIO6(GPIO5_25)	ECSPI3_SS0(UART2_TXD) / E15	IO,3.3VCMOS/ 10K PU	General purpose Input/Output6.
192	LPC_LDRQ#/ GPIO7	Q7_GPIO7(GPIO1_08)	GPIO1_IO08/ AG10	IO, 3.3V CMOS	General purpose Input/Output7. This pin is connected to M.2 Key-B Connector (J33) and optionally connected to M.2 Key-B/Key-M Connector(J31).
193	VCC_RTC	VRTC_3V0	NA	O, 3V Power	3V backup coin cell input for RTC.
194	SPKR/ GP_PWM_OUT2	PWM1_OUT(I2C4_SDA)	PWM1_OUT(I2C4_SDA)/ E13	I, 3.3V CMOS	Buzzer control PWM input. This pin is connected to buzzer in carrier board.
195	FAN_TACHOIN/ GP_TIMER_IN	NC		-	NC
196	FAN_PWMOUT/ GP_PWM_OUT1	PWM2_OUT(I2C4_SCL)	PWM2_OUT(I2C4_SCL)/ D13	I, 3.3V CMOS/10K PU	Fan Control PWM input. This pin is connected to Fan Header (J26) 2nd Pin.
197	GND	GND	NA	Power	Ground.
198	GND	GND	NA	Power	Ground.
199	SPI_MOSI	ECSPI1_MOSI	ECSPI1_MOS I/ B7	I, 3.3V CMOS	SPI Master Out Slave In. This Pin is connected to SPI Flash. *Note: This pin is also connected to Expansion connector3 (J14) 48th Pin.*
200	SPI_CS0#	ECSPI1_SS0	ECSPI1_SS0/ B6	I, 3.3V CMOS/ 10K PU	SPI Chip Select1. This Pin is connected to SPI Flash.
201	SPI_MISO	ECSPI1_MISO	ECSPI1_MIS O/ A7	O, 3.3V CMOS	SPI Master In Slave Out. This Pin is connected from SPI Flash. *Note: This pin is also connected to Power & IO Header-2 (J3) 1st Pin.*
202	SPI_CS1#	GPIO_ECSPI1_SS1	SAI5_MCLK/ AD15	I, 3.3V CMOS	SPI Chip Select2. This pin is also connected to Power & IO Header-2 (J3) 2nd Pin.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
203	SPI_SCK	ECSPI1_SCLK	ECSPI1_SCLK / D6	I, 3.3V CMOS	SPI Clock. This Pin is connected to SPI Flash. *Note: This pin is also connected to Power & IO Header-2 (J3) 6th Pin.*
204	MFG_NC4	MFG_NC4	NA	O, 3.3V CMOS/ 10K PD	Can be used for selecting between debug UART and JTAG This pin is connected from JTAG Header (J17) 03rd Pin through buffer.
205	VCC_5V_SB	NC	NA	-	NC
206	VCC_5V_SB	NC		-	NC
207	MFG_NC0	JTAG_TCK	JTAG_TCK/ F26	O, 3.3V CMOS/ 10K PD	JTAG Test Clock. This pin is connected from JTAG Header (J17) 09thPin through buffer.
208	MFG_NC2	JTDI_URX	UART4_RXD/ F19 Or JTAG_TDI/ E27	O, 3.3V CMOS	UART4 serial data receiver. This pin is connected from Serial to USB converter for Debug console. *Note: This pin is also connected to JTAG Header (J17) 05thPin (JTAG_TDI) through buffer.*
209	MFG_NC1	JTDO_UTX	UART4_TXD/ F18 Or JTAG_TDO/ E26	I, 3.3V CMOS	UART4 serial data transmitter. This pin is connected to Serial to USB converter for Debug console. *Note: This pin is also connected to JTAG Header (J17) 13thPin (JTAG_TDO) through buffer.*
210	MFG_NC3	JTAG_TMS	JTAG_TMS/ F27	O, 3.3V CMOS/ 10K PU	JTAG Test Mode Select. This pin is connected from JTAG Header (J17) 07thPin through buffer.
211	VCC/NC	NC	NA	-	NC
212	VCC/NC	NC	NA	-	NC
213	VCC/NC	NC	NA	-	NC

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
214	VCC/NC	NC	NA	-	NC
215	VCC/NC	NC	NA	-	NC
216	VCC/NC	NC	NA	-	NC
217	VCC/NC	NC	NA	-	NC
218	VCC/NC	NC	NA	-	NC
219	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
220	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
221	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
222	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
223	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
224	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
225	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
226	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
227	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
228	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
229	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
230	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.

Note:

1. PCIe is not supported in i.MX 8M Nano SoC

2.4 On Board Switches

2.4.1 Power ON/OFF Switch

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board has power ON/OFF switch (SW1) to control the Main Power Input On/Off functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

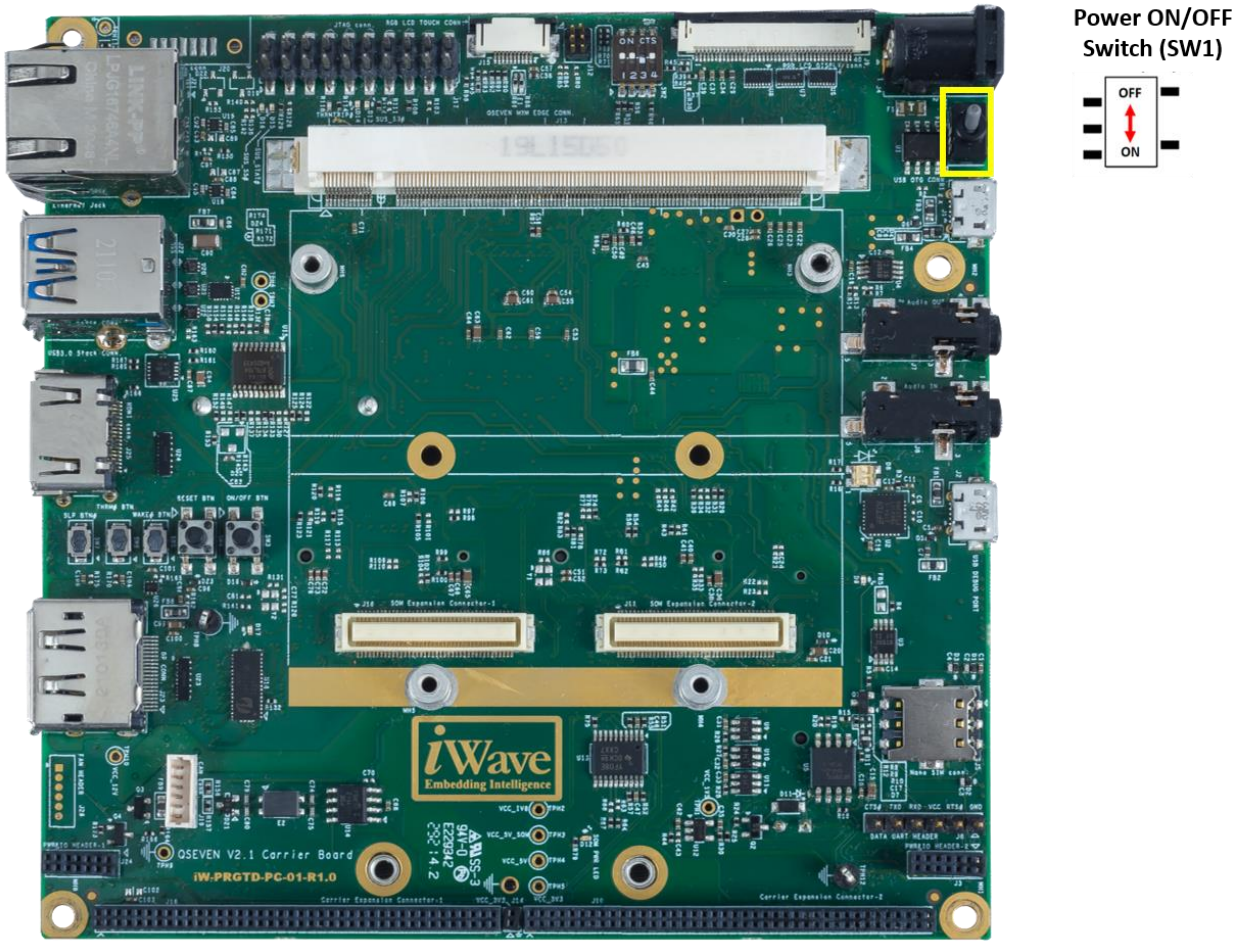


Figure 3: Power ON/OFF Switch

2.4.2 Board Configuration Switch

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform has one 4bit Board configuration switch (SW2) to configure board specific feature setting. Each bit of this switch is used to select the different features or modes. This Board configuration switch is physically located at the top of the board as shown below.

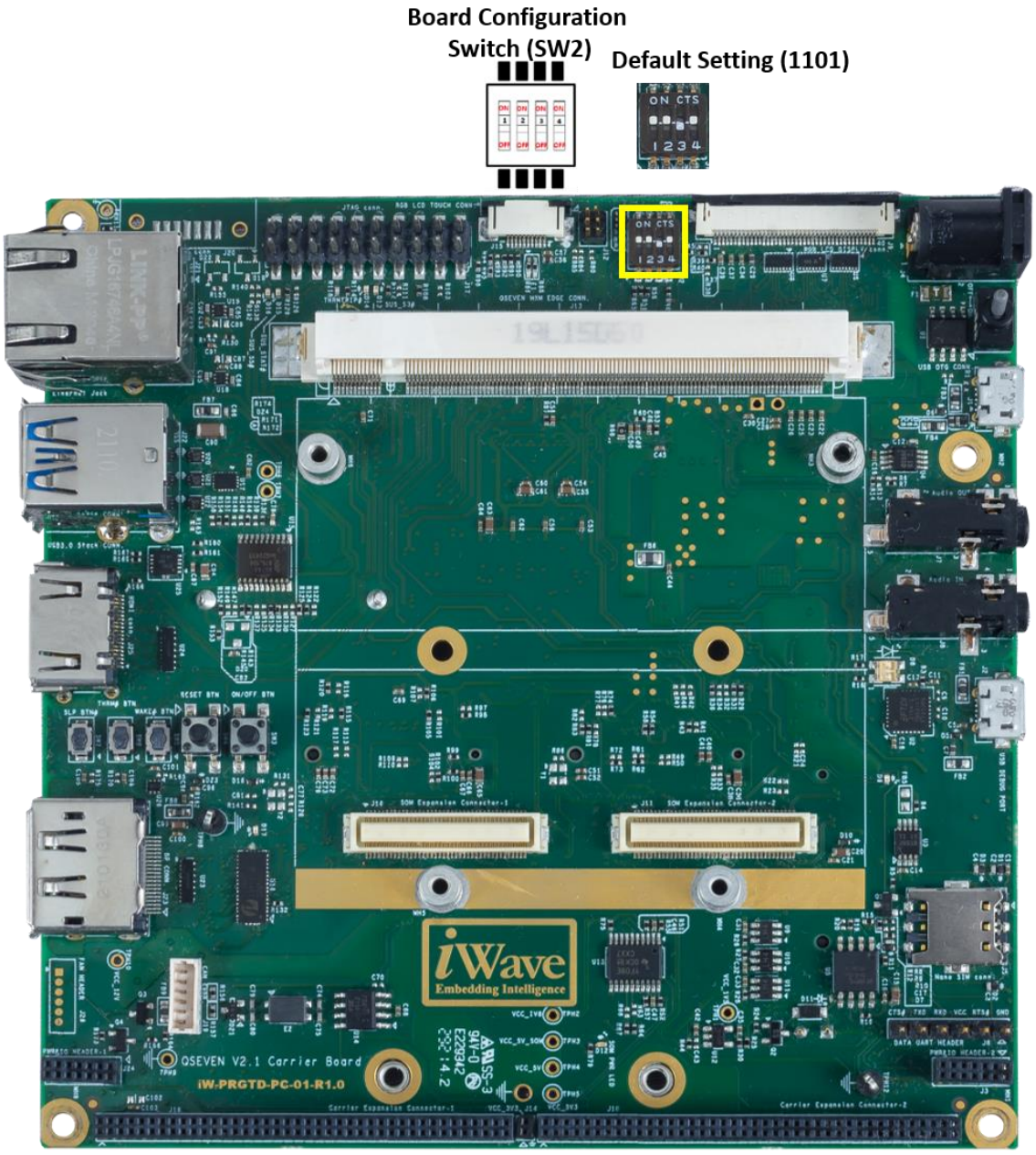


Figure 4: Board Configuration Switch

The functionality of Board configuration switch (SW2) of the carrier board is explained in the following table. All the bits of Board configuration switch are not used in i.MX 8M Mini or i.MX 8M Nano Development platform and so only the required bits are explained with default setting highlighted.

Table 4: Board Configuration Switch

SW2 Bits	SW2 Bit Name	Description	
		OFF	ON
1	M.2/LCS_SEL	M.2 Key B USB	-
2	USB_SELECT	-	M.2 KeyB/KeyM USB
3	GPU_SELECT	HDMI is selected	-
4	DEBUG_SELECT	-	Debug Port is selected as UART.

2.4.3 General Purpose Berg-stick

i.MX 8M Mini or i.MX 8M Nano µQseven SOM supports BIOS_DISABLE#/BOOT_ALT# functionality as per Qseven specification. By pulling low on this pin puts i.MX 8M Mini or i.MX 8M Nano SoC in serial download mode where the CPU boot media can be programmed through its USB OTG interface.

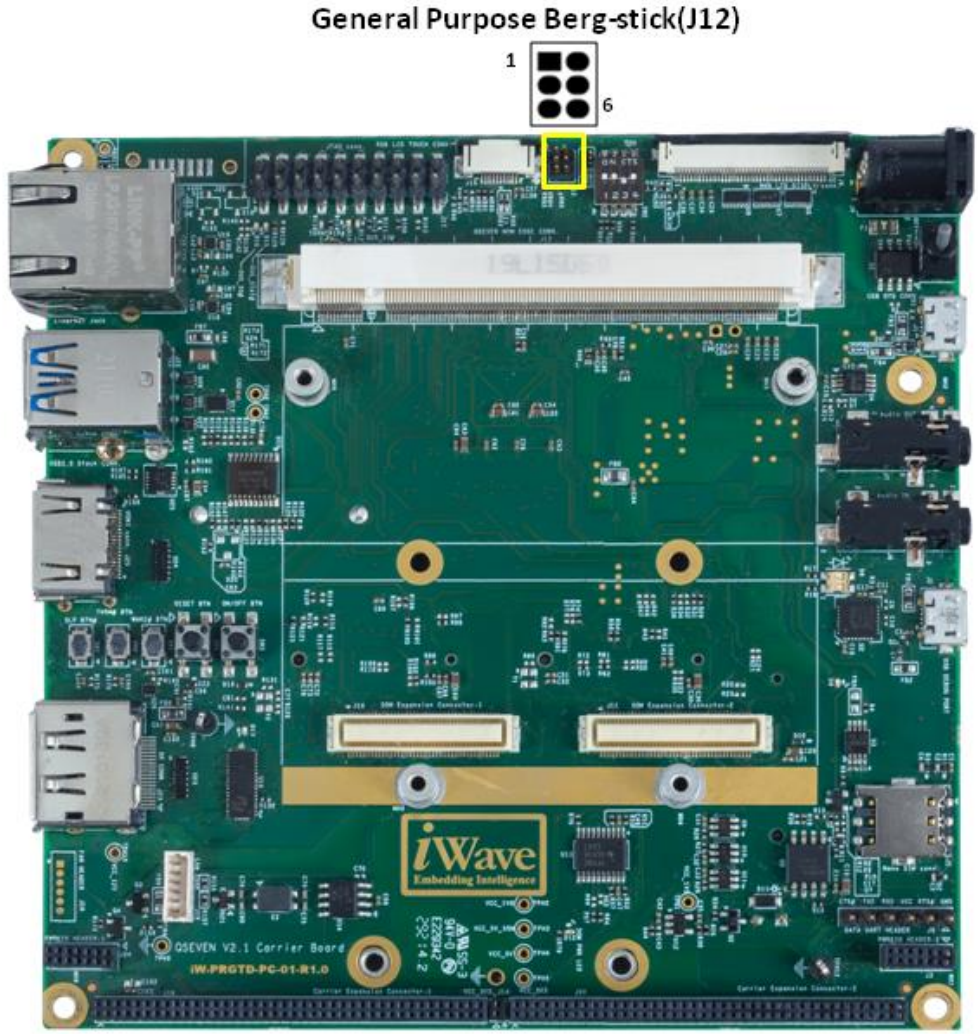


Figure 5: General Purpose Berg-Stick

Table 5: General Purpose 6 pin berg-stick

SW2 Bits	SW2 Bit Name	Description		Remark
		OFF	ON	
1	LID_BTN#/ GPII0	-	-	GPII0 is connected
2	BIOS_DSIABLE#	SoC in serial download mode where the CPU boot media can be programmed through its USB OTG interface.	Boot Mode	
3	BATLOW#/ GPII2	-	-	GPII2 is connected

2.4.4 Reset Switch

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports Push button switch (SW4) to reset the i.MX 8M Mini or i.MX 8M Nano SoC. “RSTBTN#” signal of Qseven MXM connector is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the top of the board as shown below.

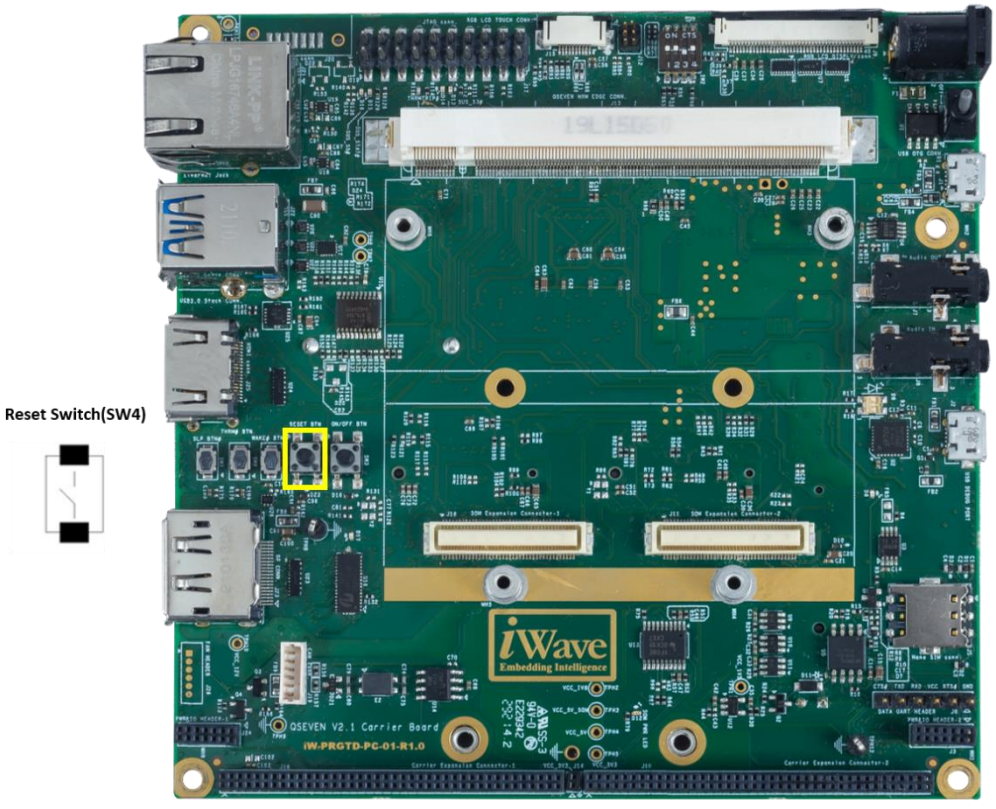


Figure 6: Reset Switch

2.5 Serial Interface Features

2.5.1 Debug UART Port

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports debug interface through CPU's UART4 interface. This UART4 signals from Qseven MXM connector is connected to UART to USB Convertor "FT232RQ" and to USB Micro AB Connector (J2). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

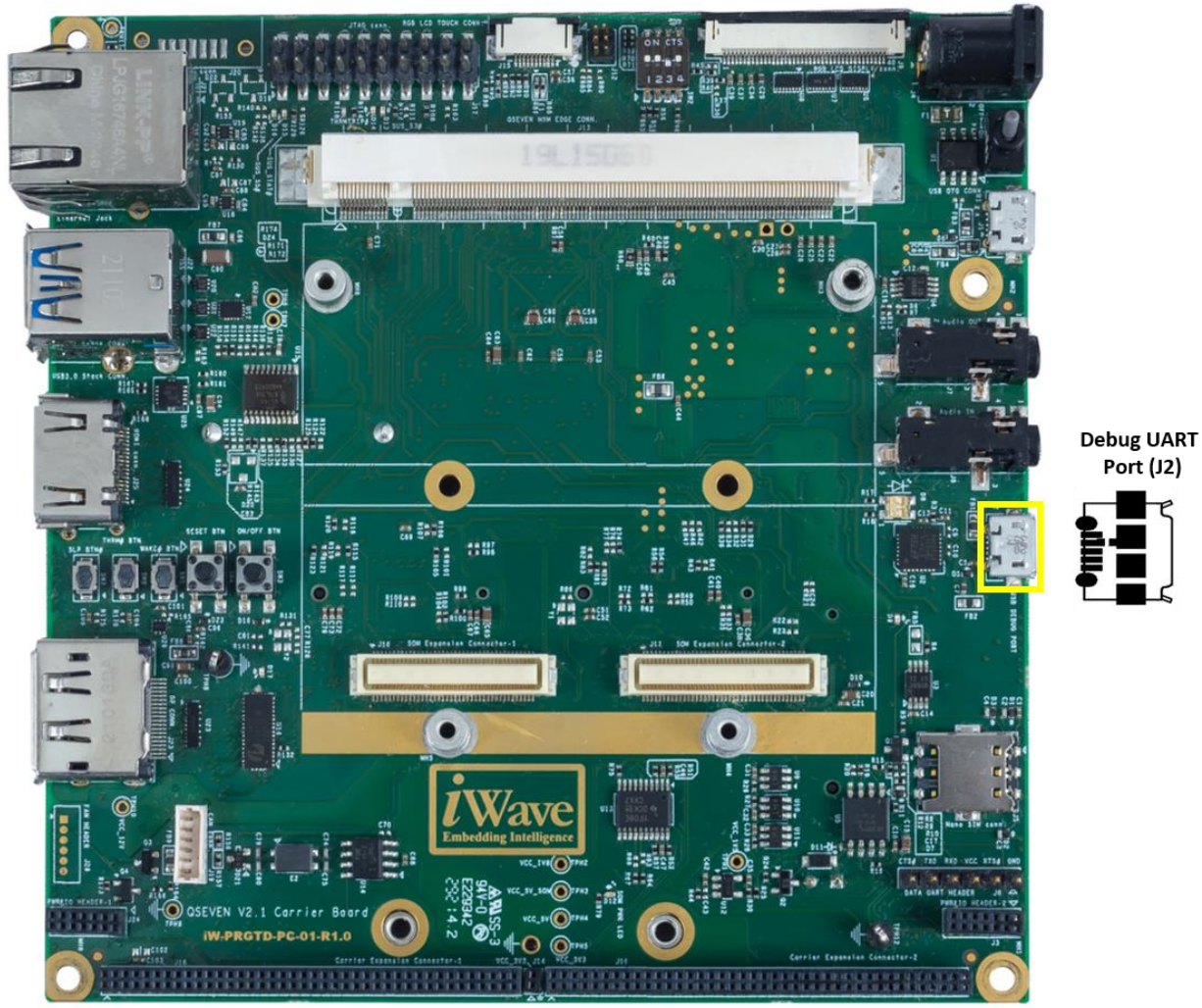


Figure 7: Debug UART

As per Qseven specification version 2.1, Debug UART interface and JTAG interface share the same pins in Qseven Edge connector and so either one interface only can be used at a time. The required debug interface can be selected by setting the 4thbit of Board configuration switch (SW2) to Debug UART Mode.

2.5.2 Data UART Header

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports full functional Data UART interface through CPU's UART2 interface. This UART2 signals from Qseven MXM connector is connected directly to 6pin Header (J6) for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

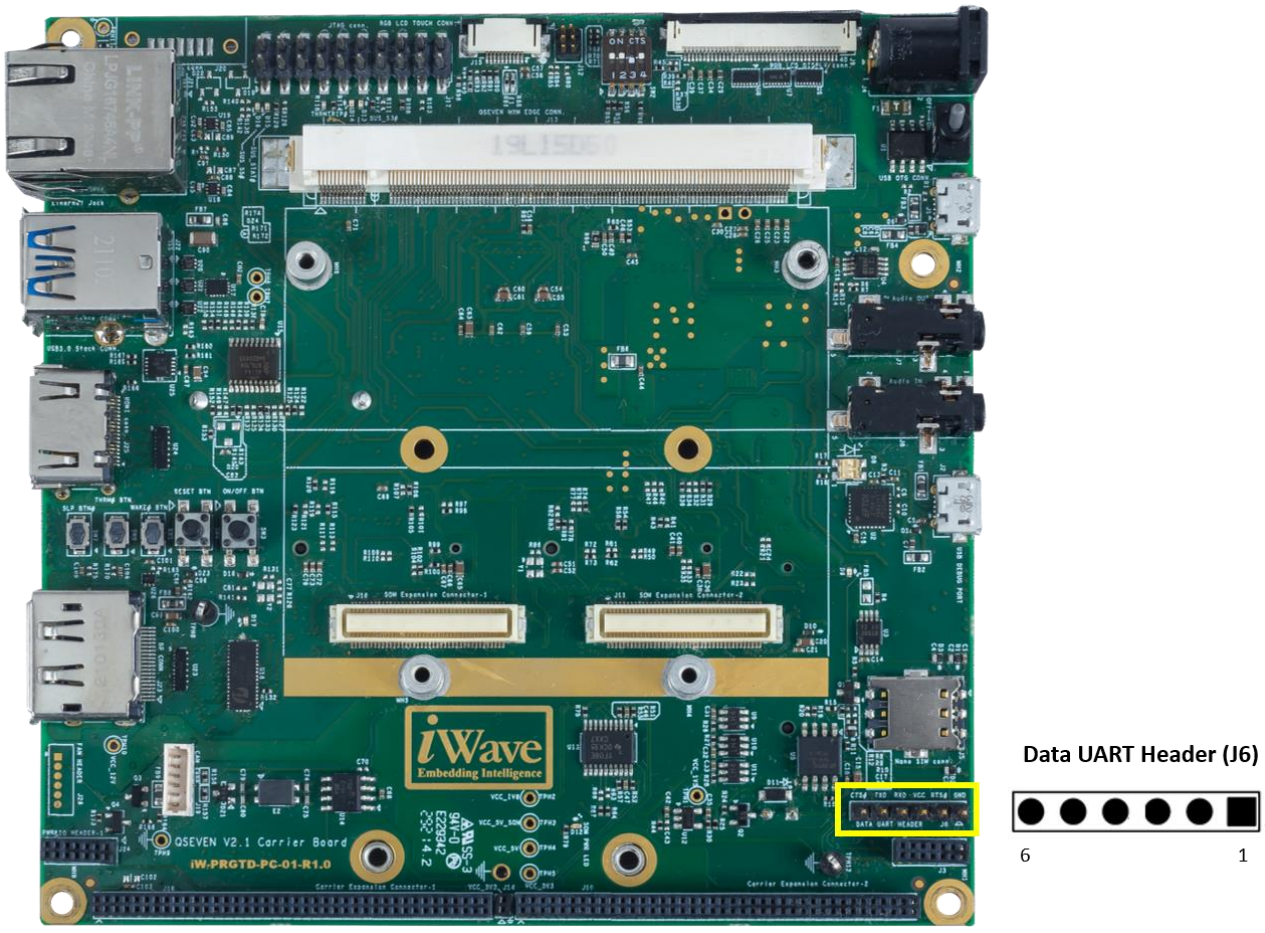


Figure 8: Data UART Header

Table 6: Data UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	CTS#	UART2_CTS_B(SAI3_RXC)	O, 3.3V CMOS	UART2 interface Clear to Send signal.
3	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	TXD	UART2_TX(SAI3_TXC)	I, 3.3V CMOS	UART2 interface Receive signal.
5	RXD	UART2_RX(SAI3_TXFS)	O, 3.3V CMOS	UART2 interface Transmit signal.
6	RTS#	UART2_RTS_B(SAI3_RXD)	I, 3.3V CMOS	UART2 interface Ready To Send signal.

2.6 High Speed Interface Features

2.6.1 M.2 Key-B Connector-1

The i.MX 8M Mini or i.MX 8M Nano Pico ITX SBC supports M.2 B key socket. M.2 B key socket is the Next Generation Form Factor (NGFF) which is designed to support multiple modules and make the M.2 more suitable in application like solid-state storage, WWAN. The M.2 Key-B supports USB 2.0, UIM and SMBus.

The M.2 Key-B Connector(J33) is physically located on the bottom side of the board as shown below.

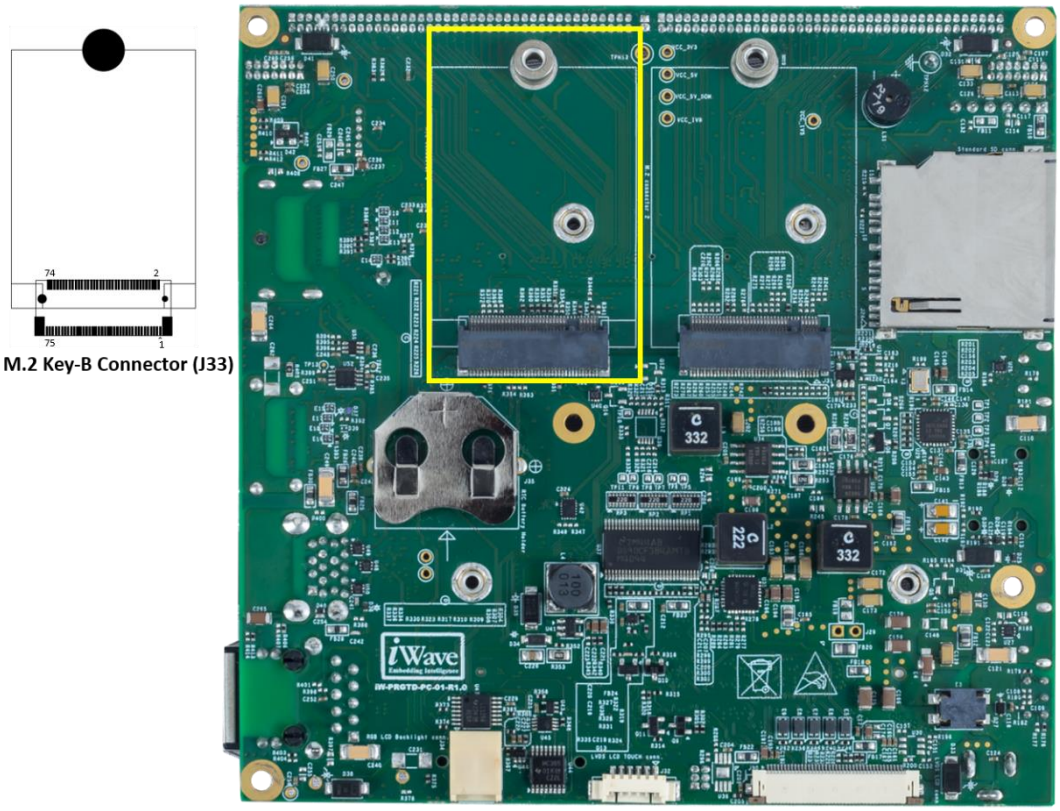


Figure 9: M.2 Key-B Connector-1

Table 7: M.2 Key-B Connector-1 Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_1_CONFIG_3	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 3.
2	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND	GND	Power	Ground.
4	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	GND	GND	Power	Ground.
6	FULL_CARD_POWER_OFF# (O)(0/1.8V_3.3V)	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal.
7	USB_D+	USB_HUB3OUT_DP	IO, USB	USB2.0 Host Port3 Data Plus.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
8	W_DISABLE1# (O)(0/3.3V)	Q7_GPIO1(GPIO1_05)	O, 3.3V CMOS	M.2 Wireless Disable Signal *Note: 10K PU is provided for W_DISABLE*
9	USB_D-	USB_HUB3OUT_DM	IO, USB	USB2.0 Host Port3 Data Minus.
10	GPIO9(LED1#/DAS_DSS#) (I/0)(0/3.3V)	NC	O, 3.3V CMOS	Provide status indicators via LED. Note: M.2_LED_1 is connected to LED
11	GND	GND	Power	Ground.
12	B1	NC	NC	NC.
13	B2	NC	NC	NC.
14	B3	NC	NC	NC.
15	B4	NC	NC	NC.
16	B5	NC	NC	NC.
17	B6	NC	NC	NC.
18	B7	NC	NC	NC.
19	B8	NC	NC	NC.
20	GPIO5(AUDIO0/I2S_CLK(I/O)(0/1.8V)	NC	NC	NC.
21	CONFIG_0	M.2_1_CONFIG_0	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 0.
22	GPIO6_(AUDIO1/I2S_RX) (I/O)(0/1.8V)	NC	NC	NC.
23	GPIO11(WOWWAN#/HSIC_DATA(1.2V))(I/O) (0/1.8V)	Q7_GPIO7(GPIO1_08)	IO, 1.8V CMOS	M.2 Host Wake.
24	GPIO7(AUDIO2/I2S_TX) (I/O)(0/1.8V)	NC	NC	NC.
25	DPR (O) (0/1.8V)	DPR	O, 1.8V CMOS 10K PU	M.2 Dynamic Power Reduction Signal.
26	GPIO10_(W_DISABLE_2#/HSIC_STROBE(1.2V)) (I/O)(0/1.8V)	NC	NA 10K PU	NC.
27	GND	GND	Power	Ground.
28	GPIO8(AUDIO3/I2S_WS)(I/O)(0/1.8V)	NC	NC	NC.
29	PERN1/USB30_RX-/SSIC_RX-	NC	NC	NC.
30	UIM-RESET (I)	SIM_RST	O, SIM	SIM Card Reset Signal.
31	PERP1/USB30_RX+/SSIC_RX+	NC	NC	NC.

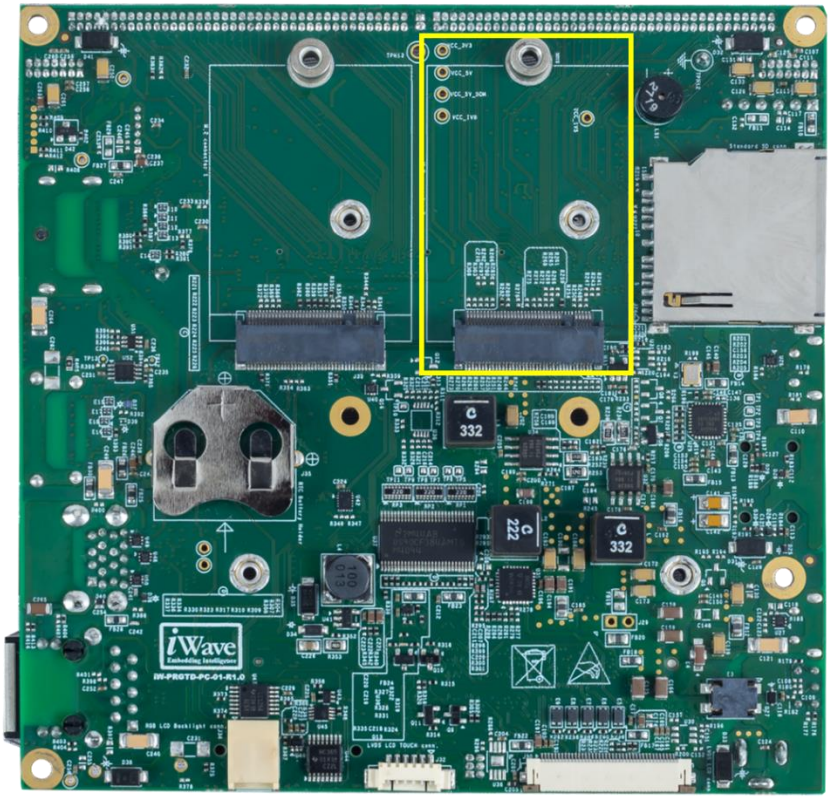
Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
32	UIM-CLK (I)	SIM_CLK	I, SIM	SIM Card Clock Signal.
33	GND	GND	Power	Ground.
34	UIM-DATA (I/O)	SIM_DAT	IO, SIM	SIM Card Data IO Signal.
35	PETN1/USB3.1-TX-/SSIC-TXN	NC	NC	NC.
36	UIM-PWR (I)	M2_UIM_PWR	O, SIM Power	SIM Card Power.
37	PETP1/USB3.1-TX+/SSIC-TXP	NC	NC	NC.
38	DEVSLP (O)	NC	NC	NC.
39	GND	GND	Power	Ground.
40	GPIO0(SMB_CLK/GNSS_SCL/SIM_DET2)(I/O)(0/1.8V)	I2C3_SCL	O, 1.8V CMOS	I2C CLK. *Note: I2C3_SCL is given to voltage translator*
41	PERN0/SATA_B+	NC	NC	NC.
42	GPIO1(SMB_DATA/GNSS_SDA/UIM_DAT2)(I/O)/(0/1.8V)	I2C3_SDA	IO, 1.8V CMOS	I2C Data. *Note: I2C3_SCA is given to voltage translator*
43	PERP0/SATA_B-	NC	NC	NC.
44	GPIO2_(ALERT# /GNSS_IRQ/UIM_CLK2)(I)/(0/1.8V)	SMB_ALERT_B(GPIO1_15)	IO, 1.8V CMOS	General Purpose Input Output.
45	GND	GND	Power	Ground.
46	GPIO3(SYSCLK/GNSS_0/ UIM_RST2) (I/O)(0/1.8V)	NC	NC	NC.
47	PETN0/SATA_A-	NC	NC	NC.
48	GPIO4(TX_BLK/GNSS_1/ UIM_PWR2)(I/O)(0/1.8V)	NC	NC	NC.
49	PETP0/SATA_A+	NC	NC	NC.
50	PERST# (O)(0/3.3V)	NC	-	NC
51	GND	GND	Power	Ground.
52	CLKREQ# (I/O)(0/3.3V)	NC	-	NC
53	REFCLKN	NC	NC	NC
54	PEWAKE# (I/O)(0/3.3V)	NC	NC	NC
55	REFCLKP	NC	NC	NC.
56	MFG_DATA	NC	NC	NC.
57	GND	GND	Power	Ground.
58	MFG_CLOCK	NC	NC	NC.
59	ANTCTL0 (I)(0/1.8 V)	NC	NC	NC.
60	COEX3 (I/O)(0/1.8V)	NC	NC	NC.

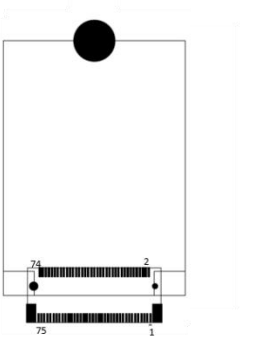
Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
61	ANTCTL1 (I)(0/1.8 V)	NC	NC	NC.
62	COEX_TXD (O)(0/1.8V)	NC	NC	NC.
63	ANTCTL2 (I)(0/1.8 V)	NC	NC	NC.
64	COEX_RXD (I)(0/1.8V)	NC	NC	NC.
65	ANTCTL3 (I)(0/1.8 V)	NC	NC	NC.
66	SIM_DETECT (I)	M.2_SIM_DETECT_1	NC	NC
67	RESET# (O)(0/1.8V)	Q7_GPIO5(GPIO1_07)	I, 1.8V	M.2 Reset Signal
68	SUSCLK(32KHZ) (O)(0/3.3V)	M.2_SUSCLK	I, 32.768kHz Clock Supply	*Note: Optionally connected 32.768kHz Clock output*
69	CONFIG_1	M.2_1_CONFIG_1	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 1.
70	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND	GND	Power	Ground.
72	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND	GND	Power	Ground.
74	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_1_CONFIG_2	I, 3.3V CMOS 10K PU	M.2 Configuration Pin 2.

2.6.2 M.2 Key-B/Key-M Connector-2

The i.MX 8M Mini Qseven Development platform supports one PCI Express Gen2.0 lane through CPU's PCIe0 interface. PCIe reference clock from Qseven MXM connector is connected to M.2 Key-B/Key-M Connector for clock reference.

The M.2 Key-B/Key-M Connector(J31) is physically located on the bottom side of the board as shown below.





M.2 Key-B/Key-M Connector (J31)

Figure 10: M.2 Key-B/Key-M Connector

Table 8: M.2 key-B/Key-M Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	M.2_2_CONFIG_3	I, 3.3V CMOS 10K PU	M.2 Conn-2 Configuration Pin 3.
2	3.3 V1	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	GND1	GND	Power	Ground.
4	3.3 V2	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	PERn3	USB_HUB4OUT_DM	IO, USB	USB2.0 Host Port3 Data Positive. *Note: NC, PCIe Port 3 Receive pair negative if M.2 Key-M is used.*
6	N/A1	M.2_PWR_OFF#	O, 3.3V CMOS 10K PU	M.2 Full card Power off Signal. *This pin is NC if M.2 Key-M is used*
7	PERp3	NC	IO, USB	USB2.0 Host Port3 Data Positive. *Note:NC, PCIe Port 3 Receive pair positive if M.2 Key-M is used.*
8	N/A2	M.2_W_DISABLE1#	O, 3.3V CMOS	M.2 Wireless Disable Signal *Note:This pin is NC if M.2 Key-M is used*
9	GND2	USB_HUB4OUT_DM	IO, USB	USB2.0 Host Port3 Data Minus. *Note:This pin is NC if M.2 Key-M is used*
10	DAS/DSS	M.2_LED_2	O, 3.3V CMOS	Provide status indicators via LED.
11	PETn3	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Note:NC, PCIe Port 3 Receive pair negative if M.2 Key-M is used.
12	3.3 V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
13	PETp3	NC	-	NC, PCIe Port 3 Transmit pair positive.
14	3.3 V4	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
15	GND3	GND	Power	Ground.
16	3.3V5	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
17	PERn2	NC	-	NC, PCIe Port 2 Receive pair negative.
18	3.3 V6	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
19	PERp2	NC	-	NC, PCIe Port 2 Receive pair positive.
20	N/A3	NC	-	NC
21	CONFIG_0	M.2_2_CONFIG_0	I, 3.3V CMOS 10K PU	M.2 Conn-2 Configuration Pin 0.
22	N/A4	NC	-	NC
23	PETn2	NC	-	NC, PCIe Port 2 Transmit pair negative.
24	N/A5	NC	-	NC
25	PETp2	NC	-	NC, PCIe Port 2 Transmit pair positive.
26	N/A6	NC	NA 10K PU	NC
27	GND4	GND	Power	Ground.
28	N/A7	NC	-	NC
29	PERn1	NC	-	NC, PCIe Port 1 Receive pair negative.
30	N/A8	NC	-	SIM Card Reset Signal. *Note:This pin is NC if M.2 Key-M is used*
31	PERp1	NC	-	NC, PCIe Port 1 Receive pair positive.
32	N/A9	NC	-	SIM Card Clock Signal. *Note:This pin is NC if M.2 Key-M is used*
33	GND5	GND	Power	Ground.
34	N/A10	NC	-	SIM Card Data IO Signal. *Note:This pin is NC if M.2 Key-M is used*
35	PETn1	NC	-	NC, PCIe Port 1 Transmit pair negative.
36	N/A11	NC	-	SIM Card Power. *Note:This pin is NC if M.2 Key-M is used*
37	PETp1	NC	-	NC, PCIe Port 1 Transmit pair positive.
38	DEVSLP	NC	NC	NC.
39	GND6	GND	Power	Ground.
40	SMB_CLK	I2C3_SCL	O, 1.8V CMOS	I2C CLK. *Note: I2C3_SCL is given to voltage translator*
41	SATA-B+/PERn0	PCIE_RXN	I, DIFF	PCIe Port 0 Receive pair negative.
42	SMB_DATA	I2C3_SDA	IO, 1.8V CMOS	I2C Data.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Note: I2C3_SCD is given to voltage translator
43	SATA-B-/PERp0	PCIE_RXP	I, DIFF	PCIe Port 0 Receive pair positive.
44	ALERT#	SMB_ALERT_B(GPIO1_15)	IO, 1.8V CMOS	General Purpose Input Output. *Note: This pin is optionally connected*
45	GND7	GND	Power	Ground.
46	N/A15	NC	-	NC
47	SATA-A-/PETn0	PCIE_TXN	O, DIFF	PCIe Port 0 Transmit pair negative.
48	N/A16	NC	-	NC
49	SATA-A+/PETp0	PCIE_TXP	O, DIFF	PCIe Port 0 Transmit pair positive.
50	PERST#	PCIe_RST(GPIO1_11)	O, 3.3V CMOS/ 10K PU	PCIe PERST#.
51	GND8	GND	Power	Ground.
52	CLKREQ#	CLKREQ#	IO, 3.3V CMOS 10K PU	M.2 Clock Request Pin
53	REFCLKN	PCIE_REFCLK_DN	O, DIFF	PCIe Reference Clock negative.
54	PEWAKE#	PCIE_WAKE_B(GPIO1_10)	O, 3.3V CMOS	PCIe Wake Signal
55	REFCLKP	PCIE_REFCLK_DP	O, DIFF	PCIe Reference Clock positive.
56	MFG1(DATA)	NC	-	NC
57	GND9	GND	Power	Ground.
58	MFG2(CLOCK)	NC	-	NC
59	M1	NC	-	NC
60	M2	Q7_GPIO5(GPIO1_07)	-	NC *Note: GPIO1_07 Optionally connected*
61	M3	NC	-	NC
62	M4	UART2_TX(SAI3_TXC)	-	NC *Note:UART2_TX(SAI3_TXC) optionally connected*
63	M5	NC	-	NC
64	M6	UART2_RX(SAI3_TXFS)		NC *Note: UART2_RX(SAI3_TXFS) optionally connected*
65	M7	NC	-	NC
66	M8	NC	NA	NC.
67	N/A17	Q7_GPIO5(GPIO1_07)	-	NC *Note: GPIO1_07 Optionally connected*
68	SUSCLK	M.2_2_SUSCLK	I, 3.3V CMOS 33E Series	M.2 Clock *Note: Optionally connected 32.768kHz Clock Oscillator.*
69	CONFIG_1	M.2_2_CONFIG_1	I, 3.3V CMOS 10K PU	M.2 Conn-2 Configuration Pin 1.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
70	3.3 V7	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
71	GND10	GND	Power	Ground.
72	3.3 V8	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	GND11	GND	Power	Ground.
74	3.3 V9	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	CONFIG_2	M.2_2_CONFIG_2	I, 3.3V CMOS 10K PU	M.2 Conn-2 Configuration Pin 2.

Note: PCIe is not supported in i.MX 8M Nano SoC.

2.7 Communication Interface Features

2.7.1 Gigabit Ethernet Port

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports Ethernet interface through CPU's ENET interface which supports 100/1000Mbps Ethernet. The Ethernet PHY output signals from Qseven MXM connector is directly connected to RJ45 Magjack (J21). Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

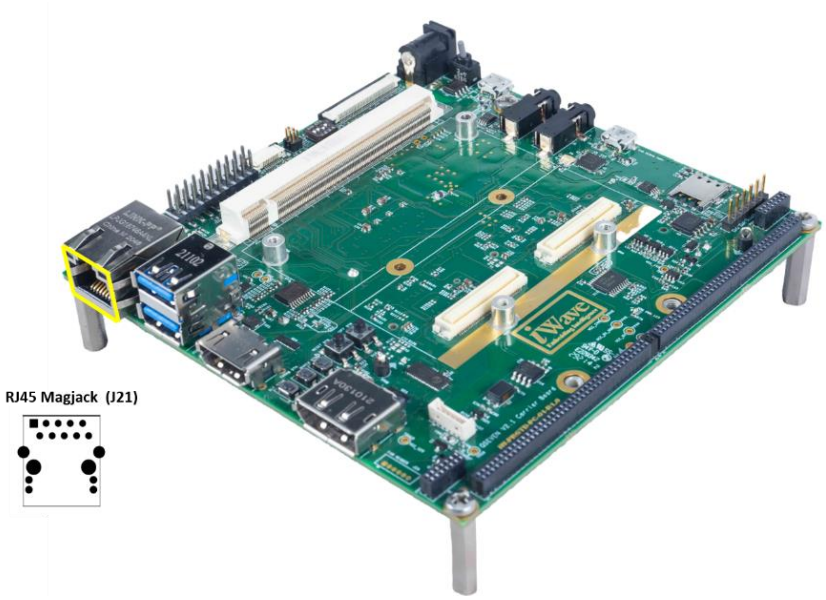


Figure 11: RJ45 Magjack

2.7.2 USB2.0 Ports (Host)

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports two USB2.0 High Speed Host Type-A connector. The CPU's USB2 channel is to edge connector connected from interface is expanded to dual USB host ports through USB HUB on i.MX 8M Mini or i.MX 8M Nano µQseven SOM and available in USB2.0 Port0 and Port2 signals of Qseven MXM connector. These two USB2.0 Port0 and Port2 host ports from the Qseven MXM connector is directly connected to Bottom and Top port of dual stack USB3.0 TypeA connector (J22) respectively.

The VBUS power of USB2.0 Port0 connector is connected through current limit power switches which limits the current above 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1 (86th Pin).

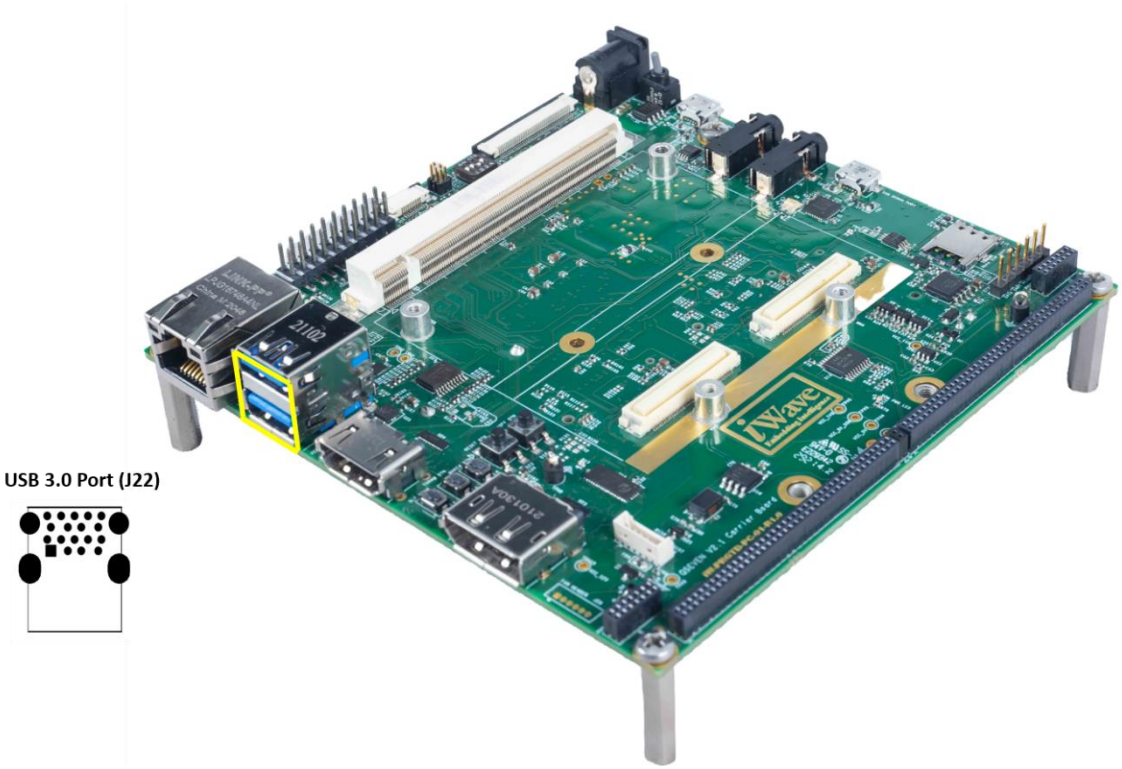


Figure 12: USB2.0 Port (Host)

2.7.3 USB2.0 Port1 (OTG)

The i.MX 8M Mini or i.MX 8M Nano Qseven Development support USB2.0 High Speed OTG interface through i.MX 8M Mini or i.MX 8M Nano SOM SoC's USB0 interface. This USB2.0 Port1 signals of Qseven MXM connector is directly connected to USB2.0 MicroAB connector (J1). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected µQseven SOM detects the USB functionality through USB ID pin and controls the power using the USB_DRIVE_VBUS pin (56th pin) of Qseven MXM connector. In Host mode, USB_DRIVE_VBUS should drive high to enable the power to the connector and in device mode, USB_DRIVE_VBUS should drive low to disable the power to the connector.

If connected USB2.0 device takes more than 500mA current, current limit power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1. This USB2.0 OTG connector is physically located at the top of the board as shown below.

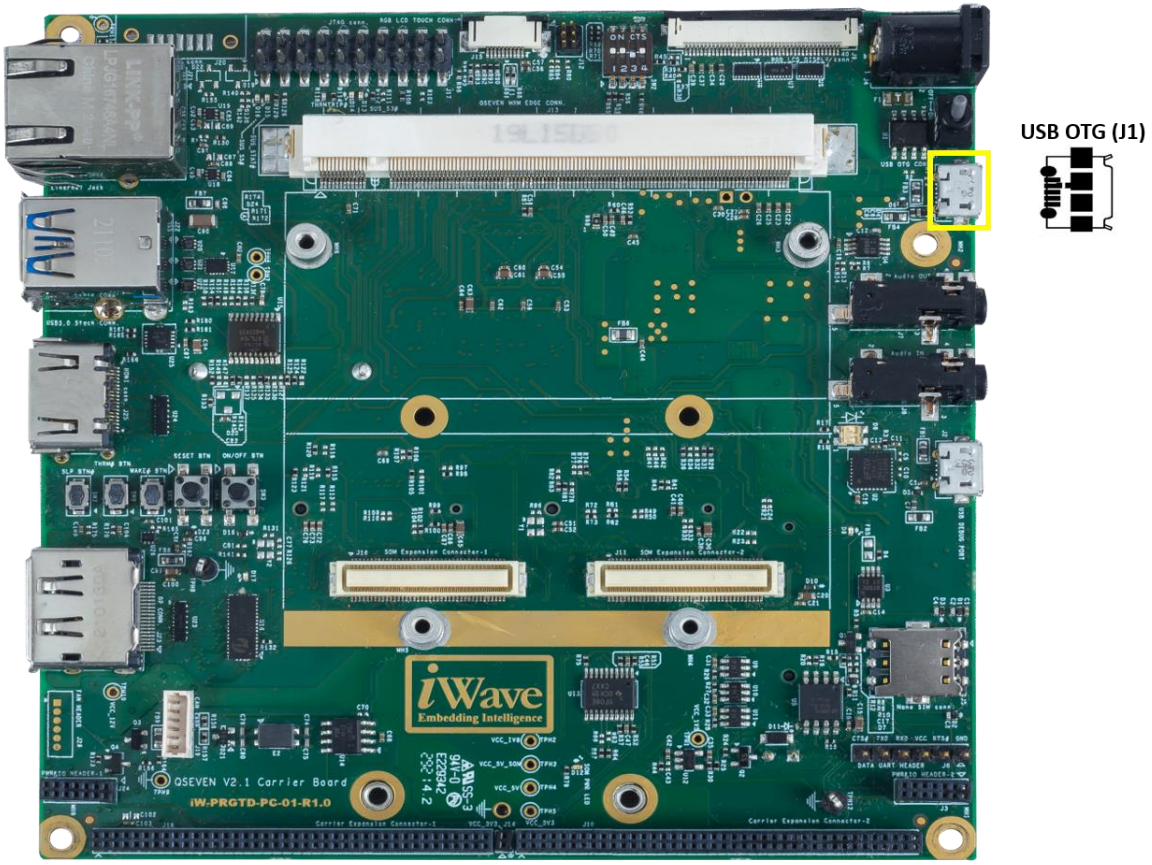


Figure 13: USB2.0 Port (OTG)

Note: In i.MX 8M Nano SOC USB2.0 OTG is available only in flash mode

2.7.4 SDIO Port

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports SDIO interface through CPU's USDHC2 interface. This USDHC2 signals from Qseven MXM connector is connected to SD/MMC connector (J28) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR# pin of Qseven MXM connector. This SD/MMC connector (J28) is physically located at the bottom of the board as shown below.

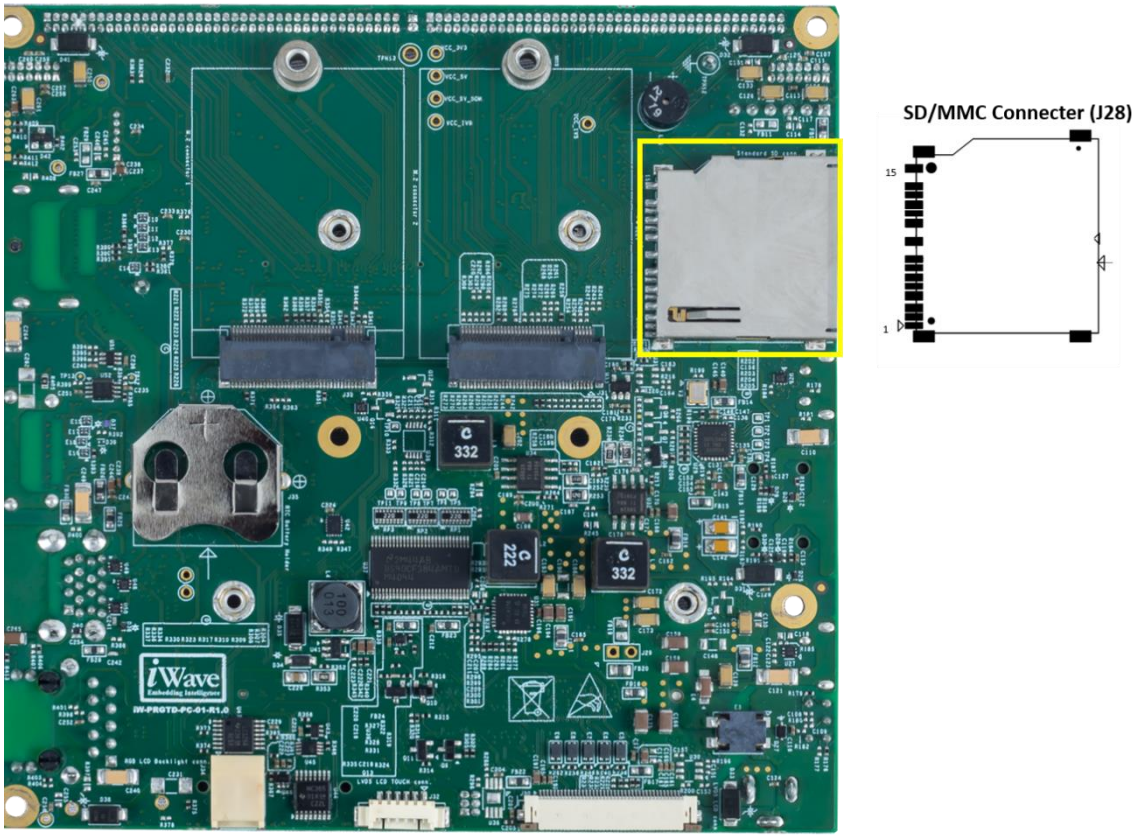


Figure 144: SD/MMC Connector

2.7.5 CAN Header

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports CAN interface by using on SOM SPI to CAN controller. CPU's ECSPI2 interface is connected to MCP2518FD to support CAN over Qseven Edge connector. This CAN interface signals from Qseven MXM connector (pins 129th& 130th) is connected to CAN Bus transceiver "MCP2562FD-E/SN" and to 6pin custom CAN header (J19). Mode select pin (Rs) of the CAN Bus transceiver is connected to GPIO4 (189th Pin) of the Qseven MXM connector. This CAN header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 530470610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

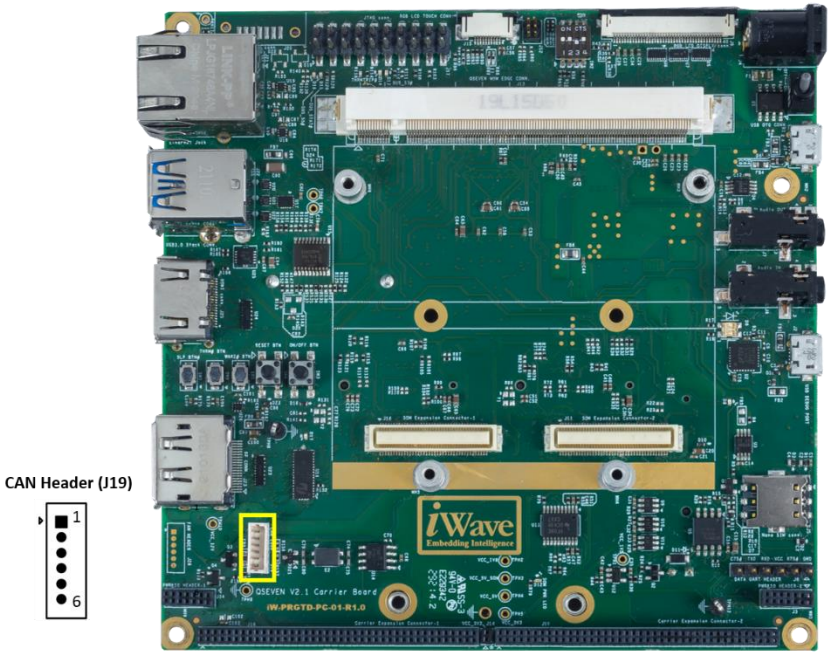


Figure 155: CAN Header

Table 9: CAN Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type /Termination	Description
1	VCC_5V	VCC_5V_CAN	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	-	NC. *Note: Optionally connected to on board 12V through resistor and not populated.*
3	CANL	CANL	IO, DIFF	CAN Differential negative.
4	GND	GND	Power	Ground.
5	CANH	CANH	IO, DIFF	CAN Differential positive.
6	GND	GND	Power	Ground.

2.8 Audio/Video Features

2.8.1 Audio IN&OUT

The i.MX 8M Mini or i.MX 8M Nano Qseven Development platform supports Audio In and Out through CPU's SAI5 interface which can support I2S format. This four wire I2S signals from Qseven MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input which is supported through 3.5mm Jack J7 and J8 correspondingly. Also, Headphone detect and Mic detect is supported through Qseven MXM connector pin 188th& 187th Pin correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

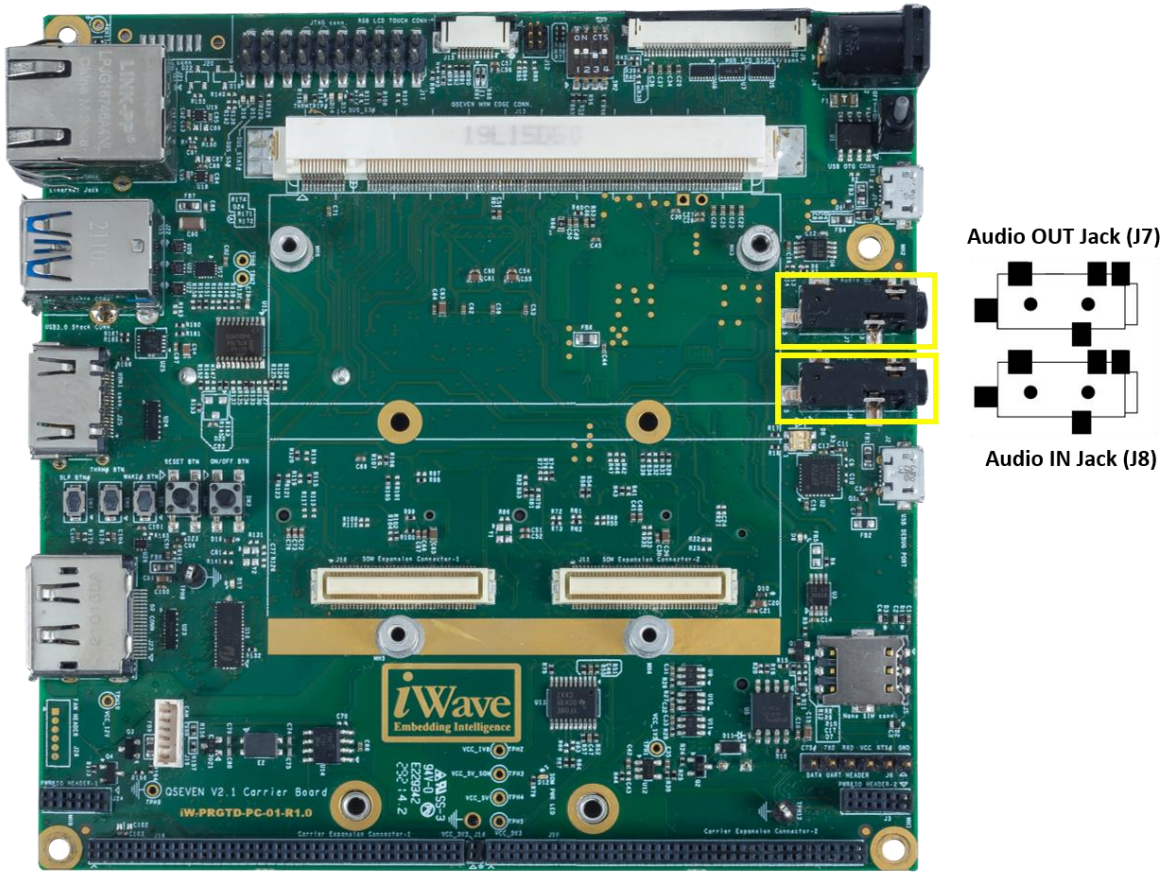


Figure 166: Audio IN/OUTJack

2.8.2 7” LCD with Capacitive Touch

i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports 7inch, 18bpp RGB LCD “ETM070001ADH6” from Emerging Display Technologies Corporation (EDT) with capacitive touch panel from MIPI_DSI to LVDS/HDMI Bridge “LT8912B” from Lontium Semiconductor and is available on the LVDS0(Primary channel) port of the Qseven MXM connector. LVDS transmitter (DS90CF384A) in carrier board which converts LVDS Interface signals to RGB and connects to RGB LCD connector (J9). This RGB LCD connector (J9) is physically located at the top of board as shown below.

This RGB LCD’s power enable and backlight enable is connected from LVDS_PPEN (111th pin) & LVDS_BLEN (112th pin) of Qseven MXM connector which is i.MX 8M Mini or i.MX 8M Nano SOC’s GPIO pins “AG9” and “AF8” respectively. Also, RGB LCD’s brightness is controlled from LVDS_BLT_CTRL (123rd pin) of Qseven MXM connector which is i.MX 8M Mini or i.MX 8M Nano SOC’s (AF9).

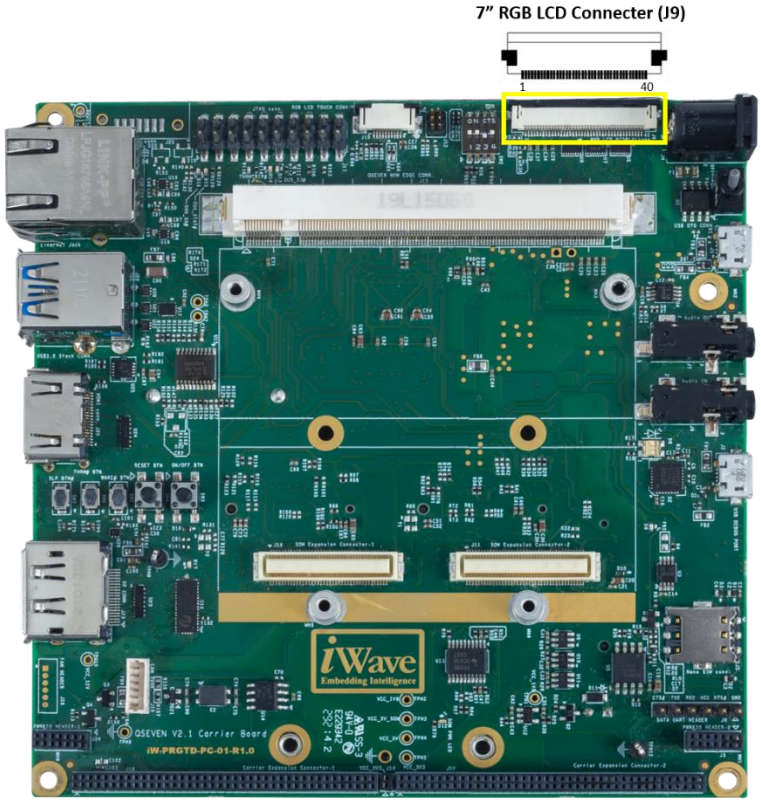


Figure 177: RGB LCD Connector

Table 10: 7” RGB LCD Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	U/D	U/D	O,3.3V CMOS/ 10K PD	Up or Down Scanning Direction.
2	R/L	R/L	O,3.3V CMOS/ 10K PU	Left or Right Scanning Direction.
3	NC	NC	-	-

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
4	VCC1	VCC_3V3_TFT1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VCC2	VCC_3V3_TFT1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VCC3	VCC_3V3_TFT1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VCC4	VCC_3V3_TFT1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	NC	NC	-	-
9	DE	DIS_DE	O,3.3V CMOS	Data Enable Output.
10	VSS1	GND	Power	Ground.
11	VSS2	GND	Power	Ground.
12	VSS3	GND	Power	Ground.
13	B5	DIS_B7	O,3.3V CMOS	Display Blue Data 7(MSB).
14	B4	DIS_B6	O,3.3V CMOS	Display Blue Data 6.
15	B3	DIS_B5	O,3.3V CMOS	Display Blue Data 5.
16	VSS4	GND	Power	Ground.
17	B2	DIS_B4	O,3.3V CMOS	Display Blue Data 4.
18	B1	DIS_B3	O,3.3V CMOS	Display Blue Data 3.
19	B0	DIS_B2	O,3.3V CMOS	Display Blue Data 2(LSB).
20	VSS5	GND	Power	Ground.
21	G5	DIS_G7	O,3.3V CMOS	Display Green Data 7(MSB).
22	G4	DIS_G6	O,3.3V CMOS	Display Green Data 6.
23	G3	DIS_G5	O,3.3V CMOS	Display Green Data 5.
24	VSS6	GND	Power	Ground.
25	G2	DIS_G4	O,3.3V CMOS	Display Green Data 4.
26	G1	DIS_G3	O,3.3V CMOS	Display Green Data 3.
27	G0	DIS_G2	O,3.3V CMOS	Display Green Data 2(LSB).
28	VSS7	GND	Power	Ground.
29	R5	DIS_R7	O,3.3V CMOS	Display Red Data 7(MSB).
30	R4	DIS_R6	O,3.3V CMOS	Display Red Data 6.
31	R3	DIS_R5	O,3.3V CMOS	Display Red Data 5.
32	VSS8	GND	Power	Ground.
33	R2	DIS_R4	O,3.3V CMOS	Display Red Data 4.
34	R1	DIS_R3	O,3.3V CMOS	Display Red Data 3.
35	R0	DIS_R2	O,3.3V CMOS	Display Red Data 2(LSB).
36	VSS9	GND	Power	Ground.
37	NC	NC	-	-
38	CLK	DIS_CLK	O,3.3V CMOS	DOT Data Clock.
39	HSYNC	DIS_HSYNC	O,3.3V CMOS	Horizontal SYNC Output.
40	VSYNC	DIS_VSYNC	O,3.3V CMOS	Vertical SYNC Output.

This RGB LCD also supports capacitive touch panel. The touch interrupt from capacitive touch controller is connected to GPIO0 (185th pin) of Qseven MXM connector which is i.MX 8M Mini or i.MX 8M Nano SOC's GPIO pin "E14". This Capacitive Touch Connector (J15) is physically located at the top of board as shown below.

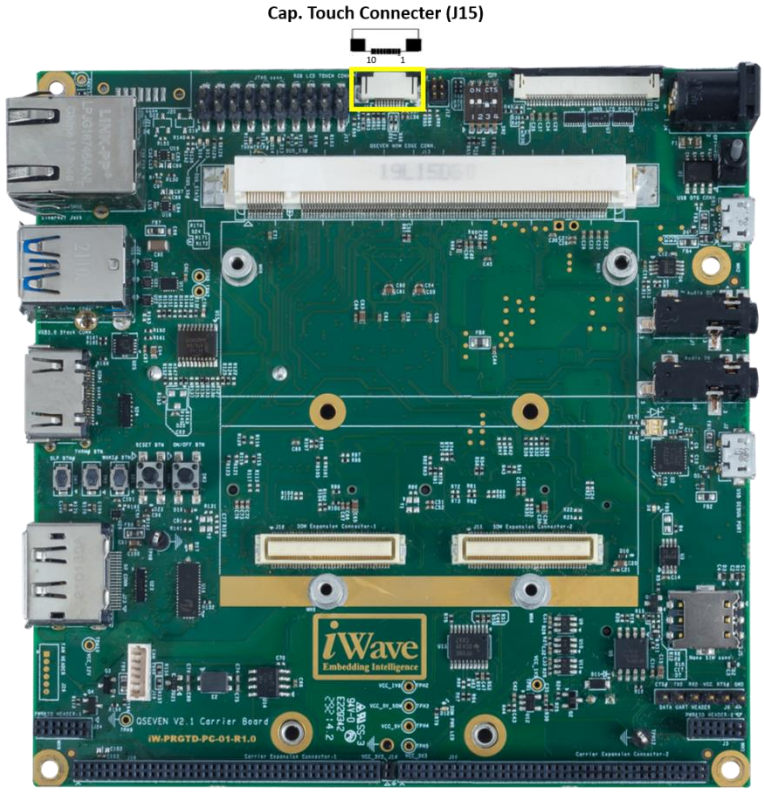


Figure 18: Capacitive Touch Connector

Table 11: Capacitive Touch Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VSS1	GND	Power	Ground.
2	VDD	VDD	O, 3.3V Power	3.3V Supply voltage.
3	SCL	I2C2_SCL	O, 3.3V OD	I2C2 Clock Signal
4	NC	NC	-	-
5	SDA	I2C2_SDA	IO, 3.3V OD	I2C2 Data Signal
6	NC	NC	-	-
7	RST#	GPIO_RESET(GPIO5_2)	O,3.3V CMOS/ 10K PU	Touch Controller Reset.
8	WAKE#	CAP_WAKE#	O,3.3V CMOS/ 10K PU	Wake Interrupt.
9	INT#	Q7_GPIO0(GPIO5_22)	I,3.3V CMOS/ 10K PU	Touch Controller Interrupt.
10	VSS1	GND	Power	Ground.

2.8.3 HDMI Port

i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports HDMI display output through On-SOM MIPI_DSI to LVDS/HDMI Bridge “LT8912B” from Lontium semiconductor and is available on the TMDS port of the Qseven MXM

connector. This TMDS signals from Qseven MXM connector is connected to HDMI connector with ESD protection circuit in the i.MX 8M Mini or i.MX 8M Nano Qseven carrier board.

HDMI connector (J25) is physically located on top of the board as shown below.

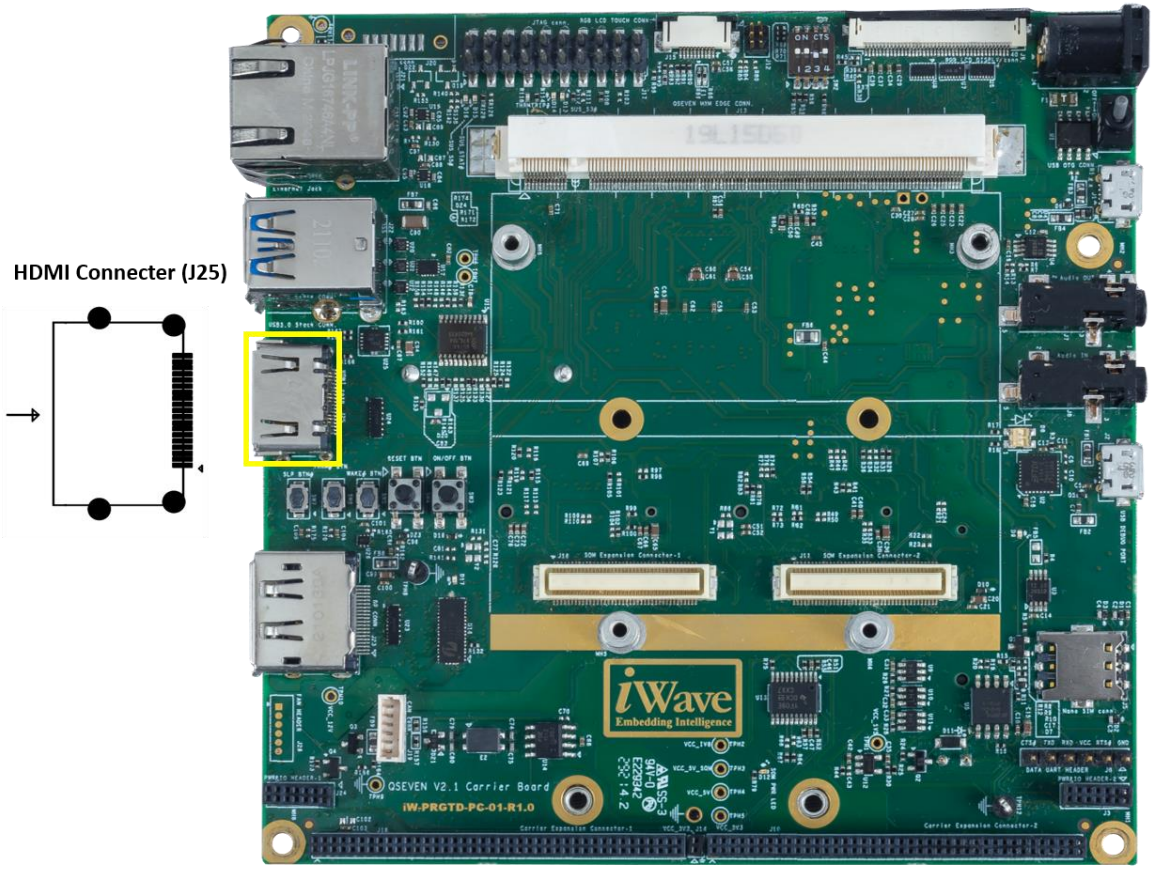


Figure 19: HDMI Connector

2.9 Additional Features

2.9.1 SPI Flash

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports SPI Flash through i.MX 8M Mini or i.MX 8M Nano Qseven SOC's ESCPI1 interface. This SPI interface signals from Qseven MXM connector is connected to SPI Flash "SST25VF016B-50" in the Qseven carrier board and operating at 3.3V Level.

2.9.2 RTC Coin Cell Holder

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to µQseven SOM for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J35) is physically located at the bottom of the board as shown below.

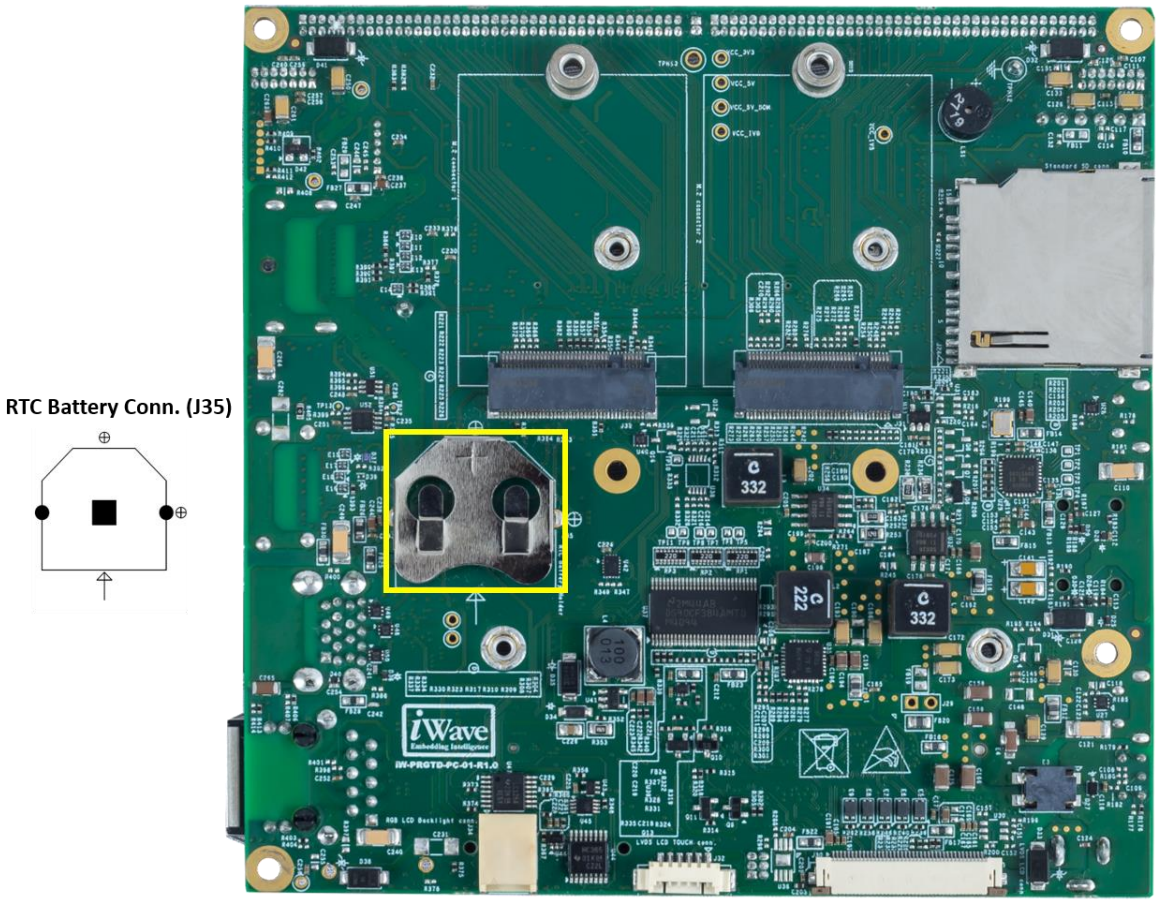


Figure 20: Coin Cell Holder

2.9.3 Fan Header

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board supports 6pin Fan Header (J26) to connect the Fan if required. The "FAN_PWMOUT" signal of Qseven MXM connector is connected to Fan header to control the speed of the Fan. This Fan Header (J26) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 530470610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

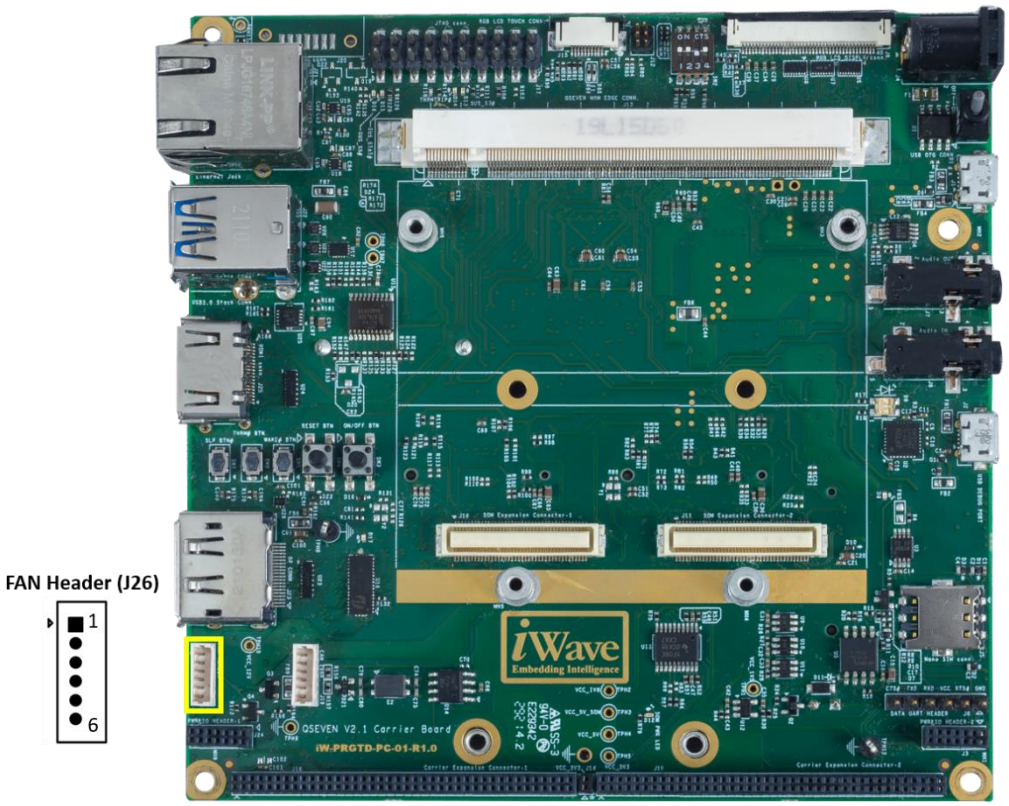


Figure 21: Fan Header

Table 12: Fan Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type /Termination	Description
1	VCC	VCC_12V	O, 12V Power	12V Supply Voltage.
2	PWM	PWM2_OUT(I2C4_SCL)	O, 3.3 CMOS	Fan Speed control.
3	GND	GND	Power	Ground.
4	TACHO	NC	-	-
5	FAN_PWR	VCC_FAN	O, Power	Controlled Power for Fan.
6	GND	GND	Power	Ground.

2.9.4 JTAG Header (Optional)

A Standard 20-pin ARM JTAG Header is available in i.MX 8M Mini or i.MX 8M Nano Qseven carrier board for debug purpose. JTAG signals from Qseven MXM connector is connected to JTAG Header (J17) through 3.3V level Buffer. This JTAG Header (J17) is physically located at the top of the board as shown below.

As per Qseven specification version 2.1, Debug UART and JTAG interfaces share the same pins in Qseven Edge connector. Hence either debug UART or JTAG interface can be used at a time. By default, Debug UART is supported in the i.MX 8M Mini or i.MX 8M Nano µQseven SOM and hence JTAG connector on i.MX 8M Mini or i.MX 8M Nano Qseven carrier board cannot be used for debugging.

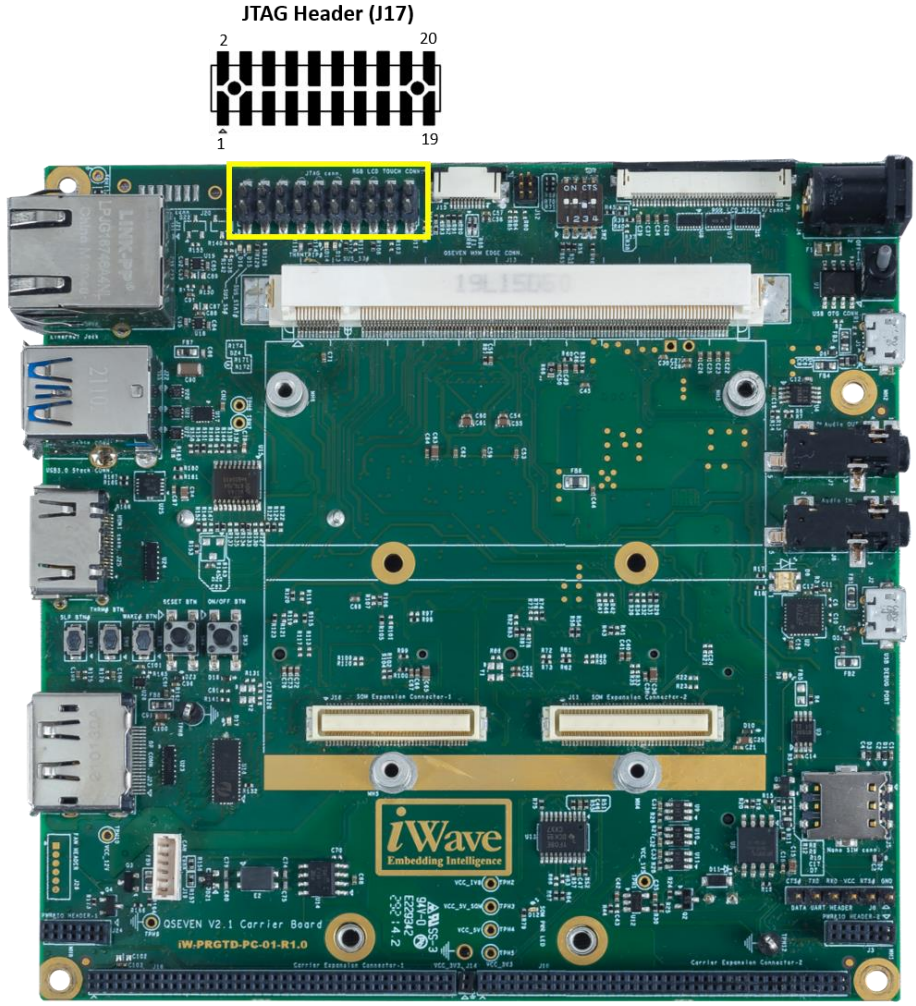


Figure 22: JTAG Header

Table 13: JTAG Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type /Termination	Description
1	VCC	VCC_3V3	O, 3.3V Power	VREF reference Voltage.
2	VCC	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	JTAG_TRSTB	JTAG_TDO	I, 3.3V CMOS	JTAG test reset signal.
4	GND	GND	Power	Ground.
5	JTAG_TDI	JTAG_TDI	I, 3.3V CMOS	JTAG test data Input.
6	GND	GND	Power	Ground.
7	JTAG_TMS	JTAG_TMS	I, 3.3V CMOS/ 10K PU	JTAG test mode select.
8	GND	GND	Power	Ground.
9	JTAG_TCK	JTAG_TCK	I, 3.3V CMOS/ 10K PD	JTAG test clock.
10	GND	GND	Power	Ground.
11	-	-	10K PD	-
12	GND	GND	Power	Ground.
13	JTAG_TDO	JTAG_TDO	O, 3.3V CMOS	JTAG test data Output.
14	GND	GND	Power	Ground.
15	RSTBN	RSTBN	I,3.3V CMOS/ 10K PU	Reset Signal.
16	GND	GND	Power	Ground.
17	NC	NC	-	NC.
18	GND	GND	Power	Ground.
19	-	-	10K PD	-
20	GND	GND	Power	Ground.

2.10 Carrier Board Expansion Connectors

Since SOM Expansion Connectors are not present, Carrier Board Expansion Connectors-1 and 2 are NC.

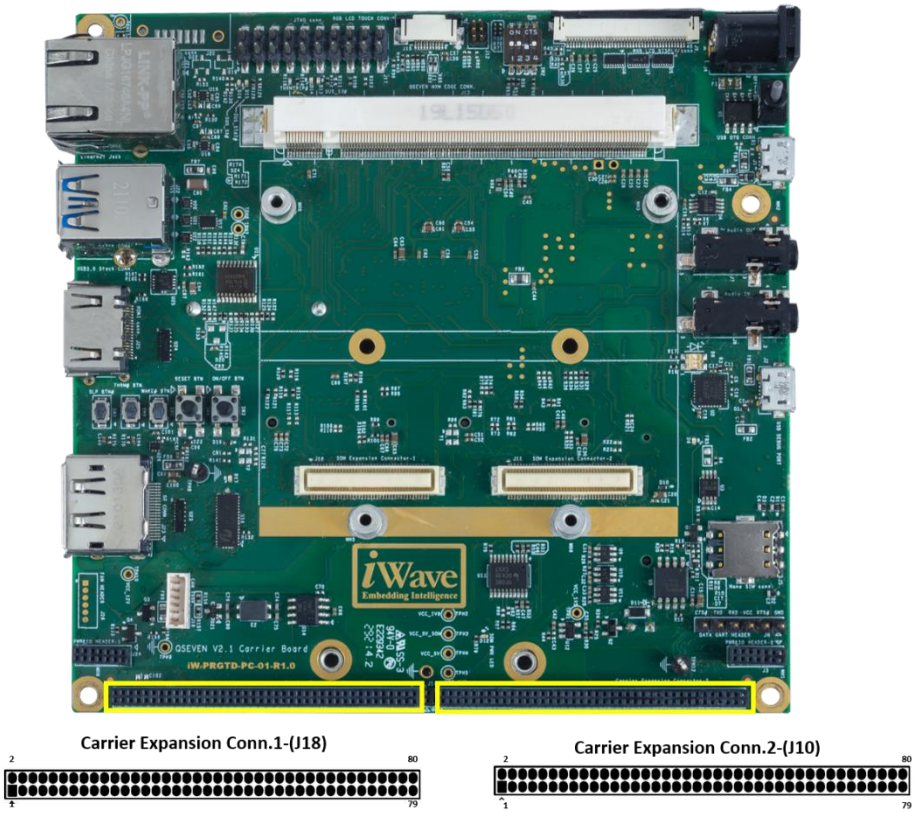


Figure 23: Carrier Board Expansion Connectors

2.11 Carrier Board Power & IO Headers

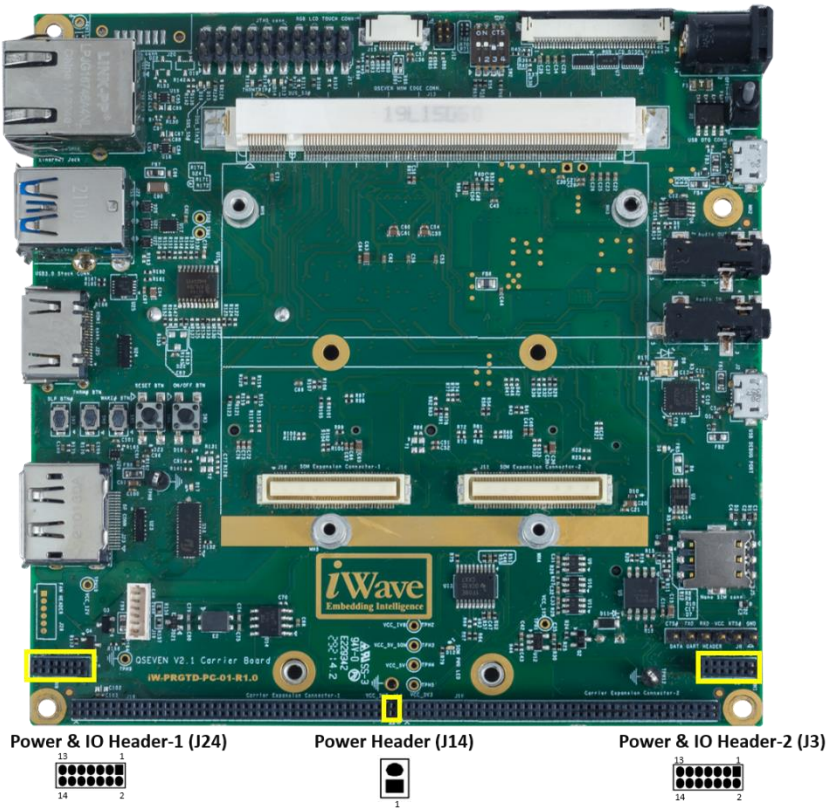


Figure 24: Carrier Board Power & IO Headers

Table 14: Carrier Board Power & IO Header-1

Pin No	Signal Name	Signal Type / Termination	Description
1	I2C2_SDA	O, 3.3V OD	I2C2 Data Signal
2	I2C3_SCL	O, 3.3V OD	I2C3 Clock Signal
3	I2C2_SCL	O, 3.3V OD	I2C2 Clock Signal
4	I2C3_SDA	O, 3.3V OD	I2C3 Data Signal
5	VCC_12V	Power	Supply Voltage 12V.
6	VCC_5V	Power	Supply Voltage 5V.
7	VCC_12V	Power	Supply Voltage 12V.
8	VCC_5V	Power	Supply Voltage 5V.
9	NC	-	NC.
10	VCC_3V3	Power	Supply Voltage 3.3V.
11	NC	-	NC.
12	VCC_3V3	Power	Supply Voltage 3.3V.
13	GND	Power	Ground.
14	GND	Power	Ground.

Table 15: Carrier Board Power & IO Header-2

Pin No	Signal Name	Signal Type / Termination	Description
1	ECSPI1_MISO	I, 3.3V CMOS	SPI Master In Slave Out. This Pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8M Mini or i.MX 8M Nano SoC's ECSPI1_MISO line through Qseven MXM connector 201st pin.*
2	GPIO_ECSPI1_SS1	I, 3.3V CMOS	SPI Chip Select2. *Note: This pin is connected to i.MX 8M Mini or i.MX 8M Nano SoC's GPIO_ECSPI1_SS1 line through Qseven MXM connector 202nd pin.*
3	ECSPI1_MOSI	O, 3.3V CMOS	SPI Master Out Slave In. This pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8M Mini or i.MX 8M Nano SoC'sECSPI1_MOSI line through Qseven MXM connector 199thpin.*
4	GND	Power	Ground.
5	VCC_3V3	Power	Supply Voltage 3.3V.
6	ECSPI1_SCLK	I, 3.3V CMOS	SPI Clock. This Pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8M Mini or i.MX 8M Nano SoC's ECSP1_SCLK line through Qseven MXM connector 203rdpin.*
7	VCC_3V3	Power	Supply Voltage 3.3V.
8	VCC_1V8	Power	Supply Voltage 1.8V.
9	WDOUT	-	Not used in i.MX 8M Mini or i.MX 8M Nano Qseven carrier board. *Note: This pin is connected to Qseven MXM connector 72nd pin.*
10	RSVD1	-	Not used in i.MX 8M Mini or i.MX 8M Nano Qseven carrier board. *Note: This pin is connected to Qseven MXM connector 44th pin.*
11	WDTRIG#	-	Not used in i.MX 8M Mini or i.MX 8M Nano Qseven carrier board. *Note: This pin is connected to Qseven MXM connector 70th pin.*
12	VCC_1V5	Power	Supply Voltage 1.5V.
13	GND	Power	Ground.
14	GND	Power	Ground.

Table 16: Carrier Board Power Header

Pin No	Signal Name	Signal Type / Termination	Description
1	GND	Power	Ground.
2	VCC_3V3	Power	Supply Voltage 3.3V.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Qseven Carrier Board through Power Jack (J4). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm (DC Plug Centre Pin is Positive). This connector is physically placed at the top of the board as shown below.

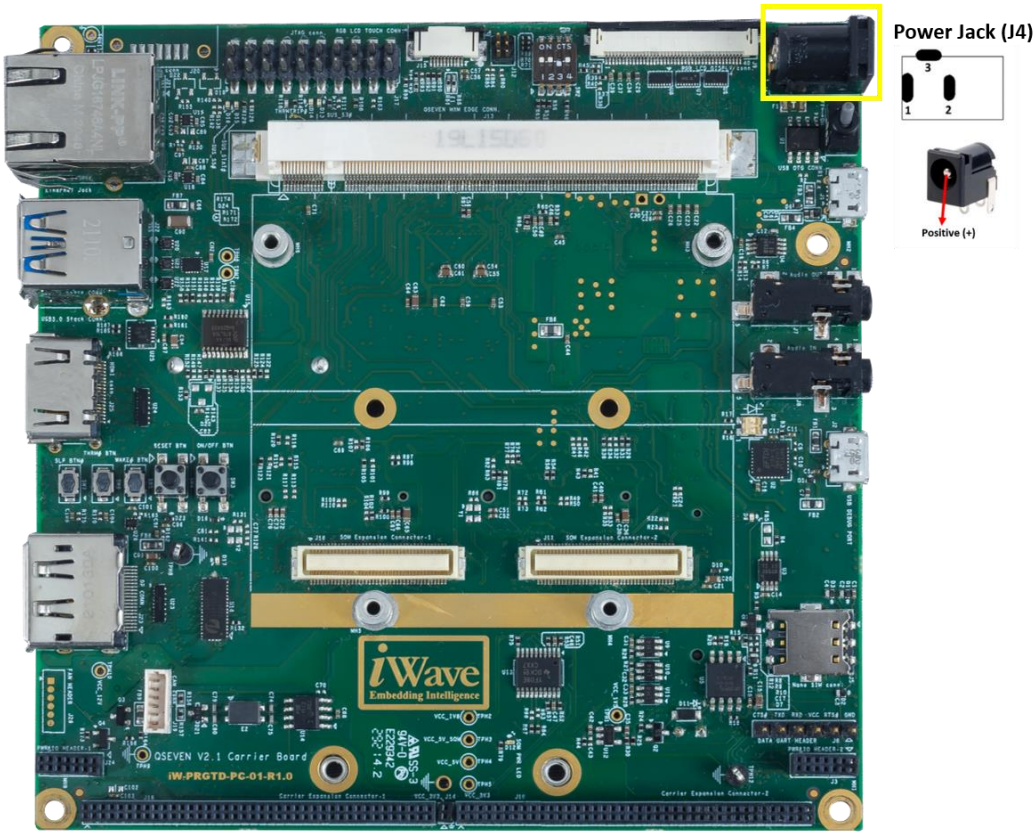


Figure 25: Power Jack

Table 17: Power Jack Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_12V	12V, Power	Input Supply Voltage.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.

The below table provides the Power Input Requirement of i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board.

Table 18: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX 8M Mini or i.MX 8M Nano µQseven SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

Important Note: All carrier board power supplies should be powered ON only after the i.MX 8M Mini or i.MX 8M Nano SoC is powered ON completely in the i.MX 8M Mini or i.MX 8M Nano µQseven SOM. This is to ensure that there is no back voltage (leakage) from any supply on the board towards the i.MX 8M Mini or i.MX 8M Nano SoC IO pins.

3.1.2 Power Output Specification

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board has dedicated power regulator to provide +5V power to µQseven SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided to µQseven SOM for Real time clock support.

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board also shares on board +5V, +3.3V and +1.5V power to Expansion connector3 for Add-On Module power.

Table 19: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to µQseven SOM (through Qseven MXM connector)					
1	VCC_5V_SOM	4.85V	5V	5.15V	4000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion connector3)					
2	VCC_5V	4.85V	5V	5.15V	1500mA
3	VCC_3V3	3.15	3.3	3.45	1000mA
3	VCC_1V5	1.35	1.5	1.65	500mA

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform.

Table 20: Environmental Specification

Parameters	Min	Max
Operating temperature range (Commercial)[1]	0°C	60°C
Storage temperature range	0°C	60°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.2.2 RoHS Compliance

iWave's i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's i.MX 8M Mini or i.MX 8M Nano Qseven Development Platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board Mechanical Dimensions

The i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board PCB form factor is Nano ITX with 120mm x 120mm. Qseven Carrier Board mechanical dimension is shown below. (All dimensions are shown in mm)

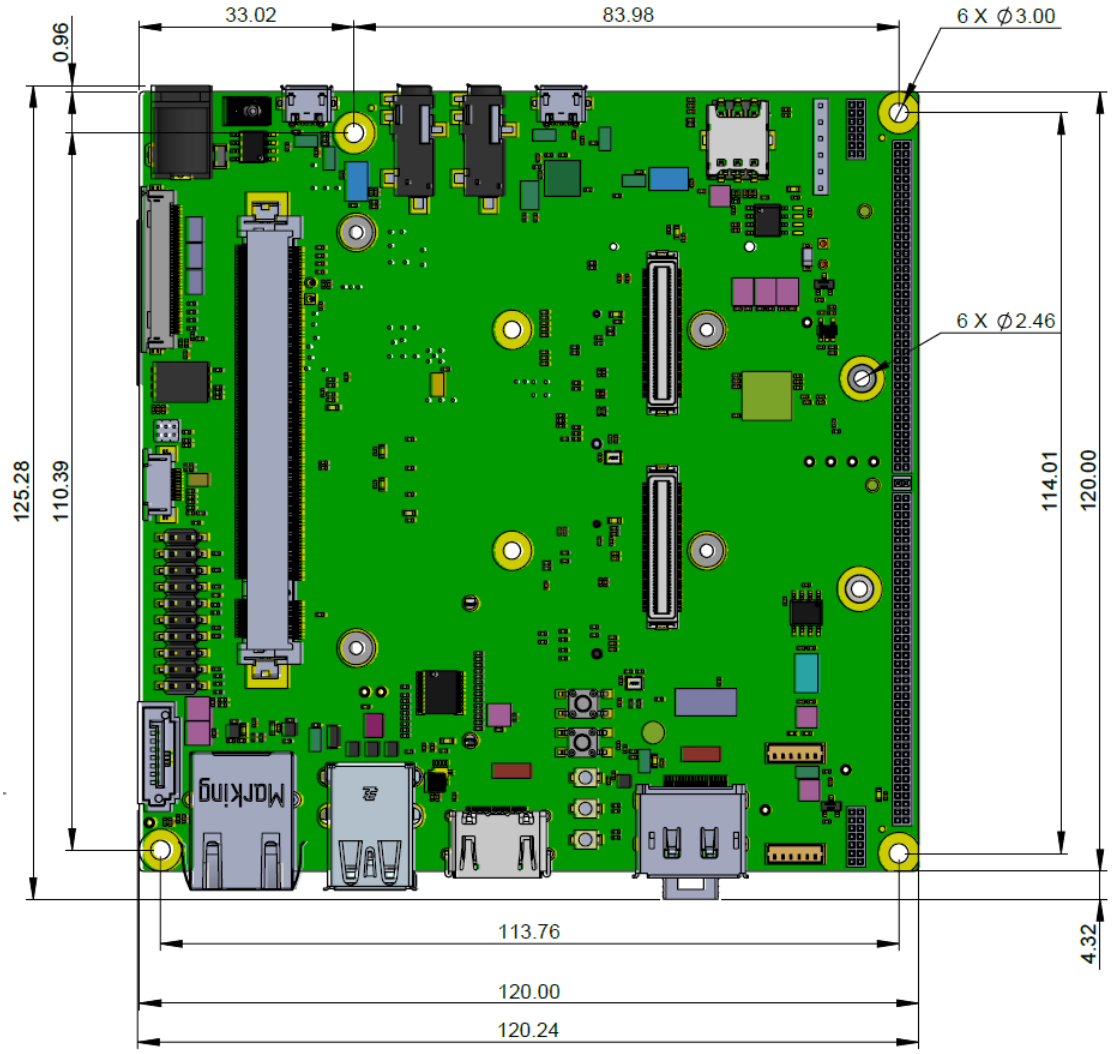


Figure 26: i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board Mechanical dimension – Top View

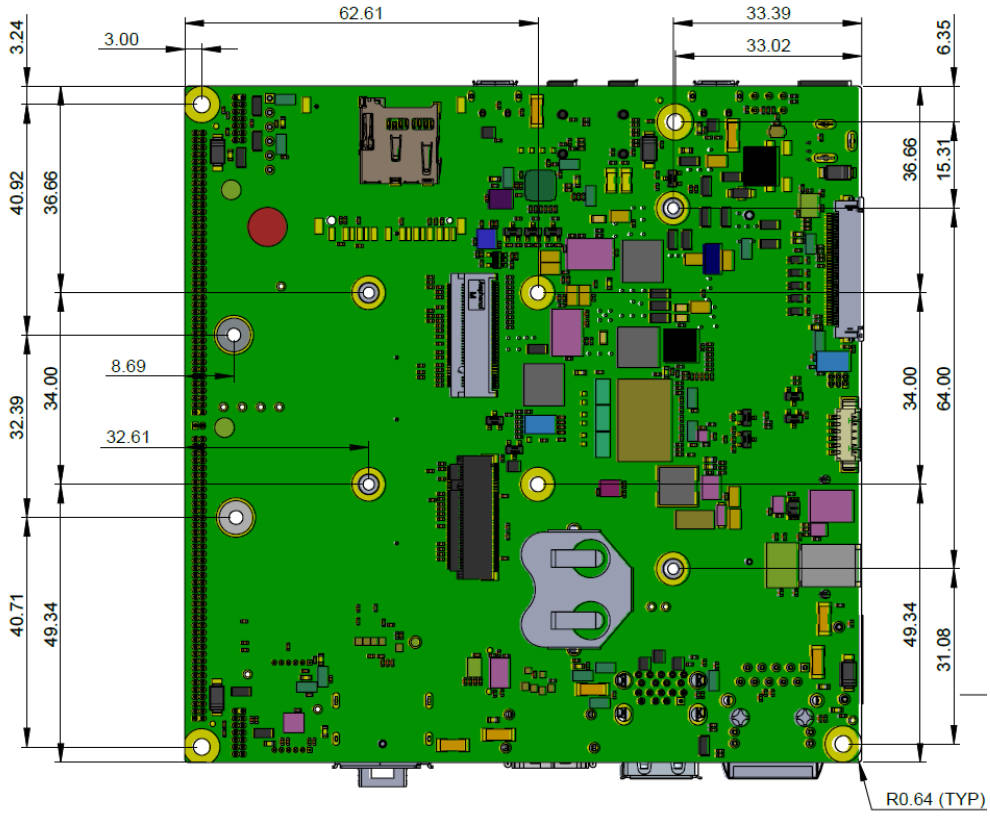


Figure 27: i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board Mechanical dimension – Bottom View

The i.MX 8M Mini or i.MX 8M Nano Qseven carrier board PCB thickness is 1.6mm±0.1mm, top side maximum height component is USB Dual Stack (16.11mm) and bottom side maximum height component is Power Header (8.93mm), which is optional in default configuration. Hence Inductors-L1, L2(7mm) will be the maximum height on bottom side in default configuration. Please refer the below figures for height details of the i.MX 8M Mini or i.MX 8M Nano Qseven Carrier Board.

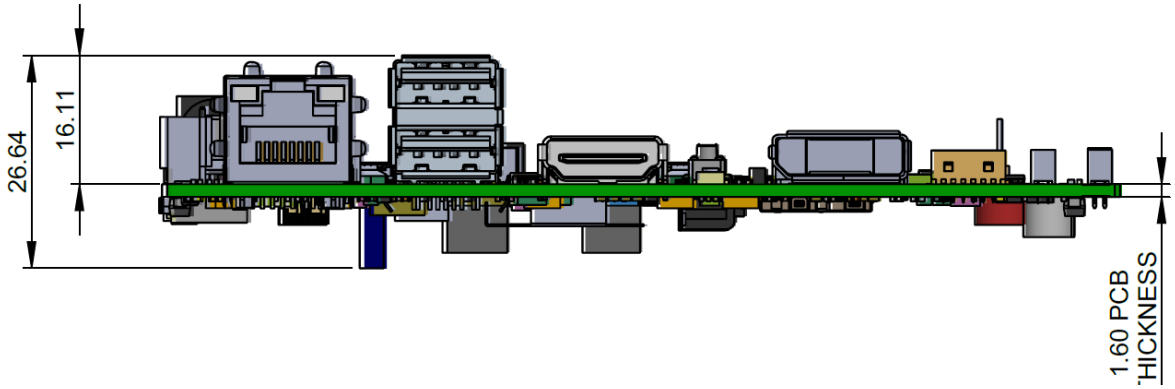


Figure 28: i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board Mechanical dimension – Top Max Heighted Components

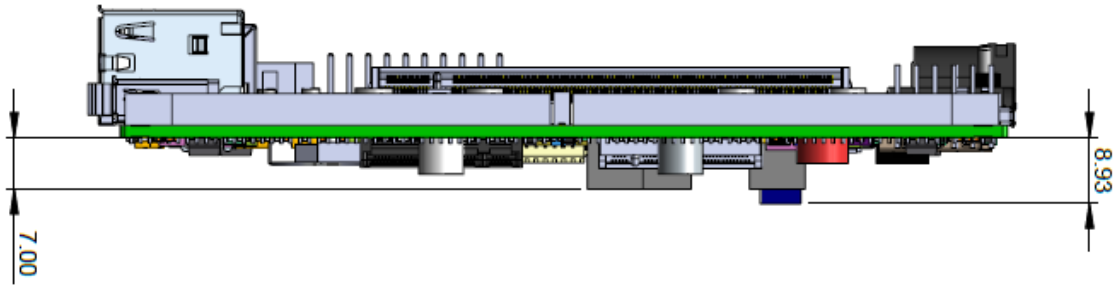


Figure 29: i.MX 8M Mini or i.MX 8M Nano Qseven Carrier board Mechanical dimension – Bottom Max Heighted Components

3.3.2 Guidelines to insert the µQseven SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the µQseven module in to the MXM connector as shown below in the below images.
- Make sure that the Notch position of µQseven module is proper while inserting.

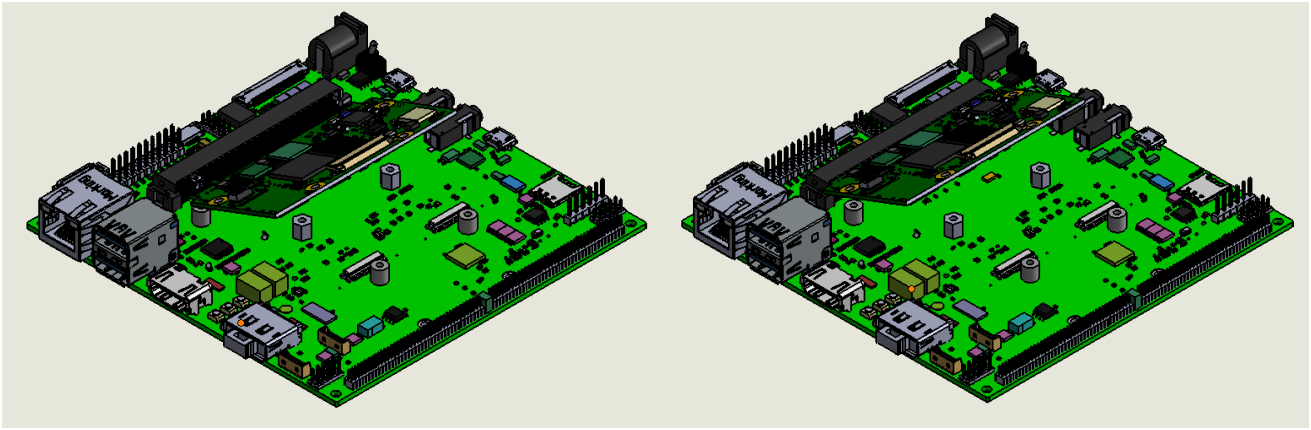


Figure 30: µQseven SOM Insertion Step -1

- Insert M2.5x12mm pan head screw from i.MX 8M Mini or i.MX 8M Nano Qseven carrier board bottom side as shown below.

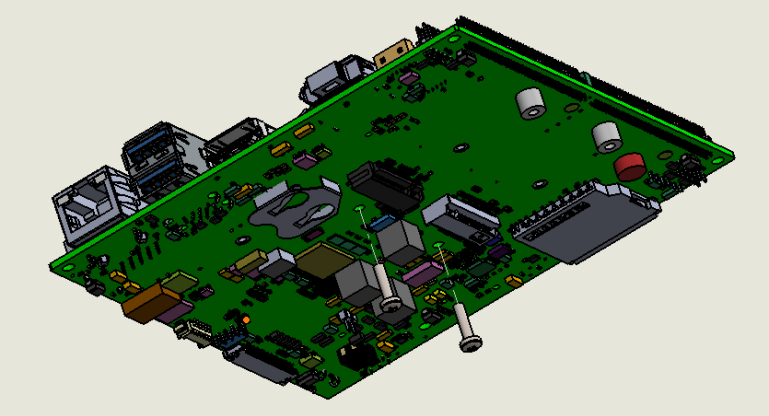


Figure 31: µQseven SOM Insertion Step -2

- Tighten the M2.5 x 5mm threaded metallic hex spacer into the inserted screw from Carrier board top side and insert the i.MX 8M Mini or i.MX 8M Nano µQseven SOM into the carrier board through the M2.5mm screw as shown below.

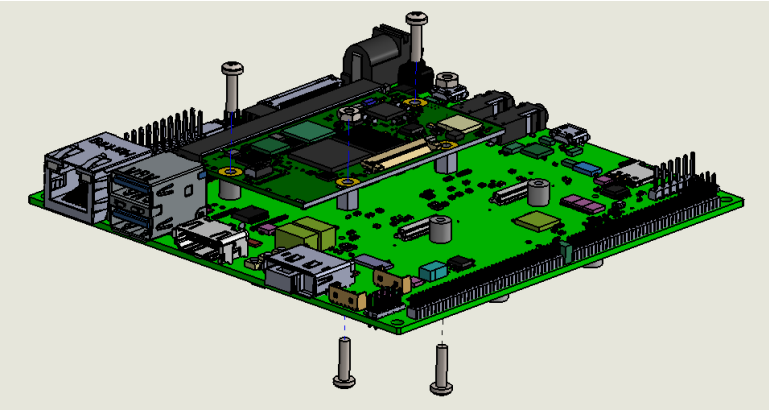


Figure 32: µQseven SOM Insertion Step -3

- Finally, tighten the M2.5mm nut into screw as shown below.

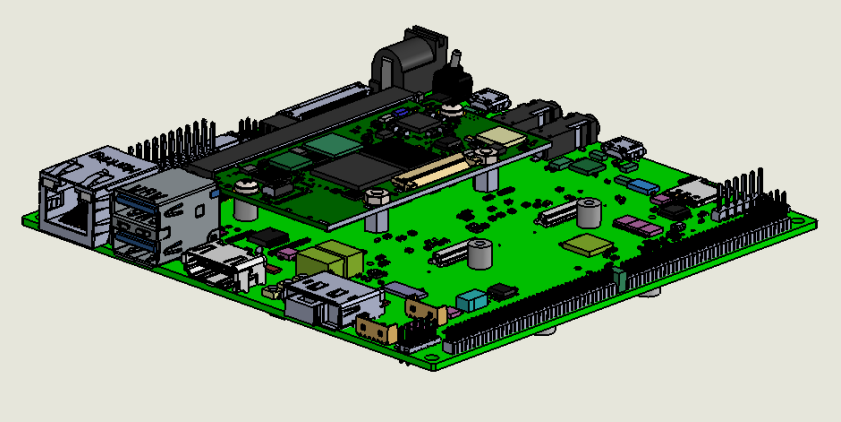


Figure 33: µQseven SOM Insertion Step -4

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Qseven Development Platform which includes i.MX 8M Mini or i.MX 8M Nano µQseven SOM and Qseven carrier board.

Table 21: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G34D – i.MX 8M Mini µQseven Development Kit		
iW-G34D-Q704-4L002G-E008G-LCC	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit with display	Commercial
iW-G34D-Q704-4L002G-E008G-LCD	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit without display	Commercial
iW-G34D-Q704-4L001G-E008G-LCC	i.MX 8M Mini Quad, 1GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit with display	Commercial
iW-G34D-Q704-4L001G-E008G-LCD	i.MX 8M Mini Quad, 1GB LPDDR4, 8GB eMMC flash, 1xEthernet, Linux Kit without display	Commercial
iW-G34D-Q704-4L002G-E008G-ACC	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC flash, 1xEthernet, Android Kit with display	Commercial
iW-G34D-Q704-4L002G-E008G-ACD	i.MX 8M Mini Quad, 2GB LPDDR4, 8GB eMMC flash, 1xEthernet, Android Kit without display	Commercial
Rainbow G37D – i.MX 8M Nano µQseven Development Kit		
iW-G37D-Q704-4L001G-E008G-LCC	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC flash, Linux Kit with display	Commercial
iW-G37D-Q704-4L001G-E008G-LCD	i.MX8M Nano Quad, 1GB LPDDR4, 8GB eMMC flash, Linux Kit without display	Commercial

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.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