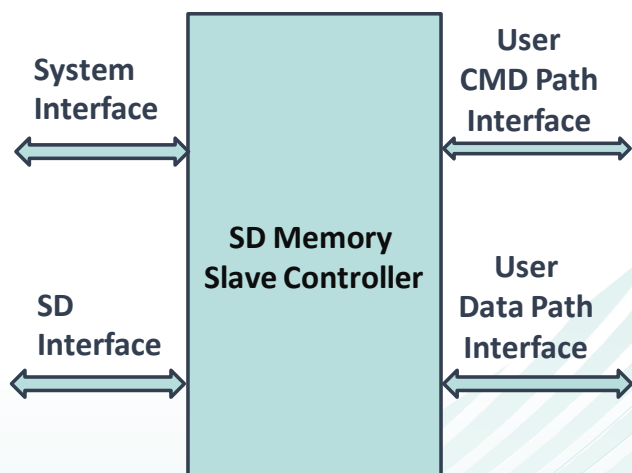


## iW SD Memory Slave 2.0 Controller IP



Memory Slave Controller IP forms a bridge between the SD host and user interface, enabling the data transfer between each other. This IP will send the response to the SD host depending on the command issued and also communicates with the user through a register interface for control and status. The Controller has two different variants depending on the availability of the processor towards user side. One being the AXI4 -lite or AHB complaint interface for accessing through processor and other is simple general-purpose interface which can be used without the processor.

### Highlights

- Core handles SD bus protocol on the card interface and provides simplified interface to user logic
- Core handle all the housekeeping tasks by itself without user logic intervention
- Supports both processor and non-processor environments with two different variants
- Supports both the standard and High capacity operation

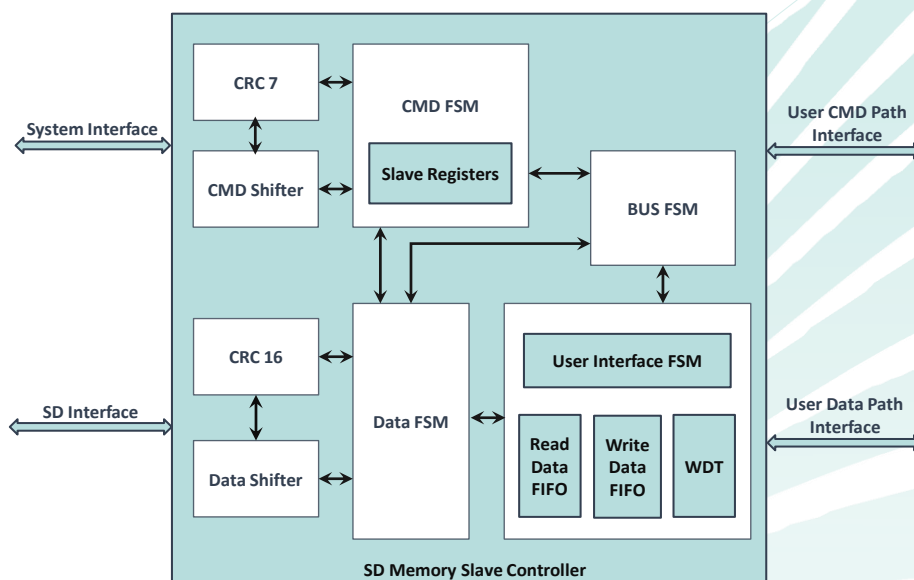
### Applications

- SOC design integration with SD memory card
- Used in all kind of consumer electronics devices such as digital cameras, mobile phones etc

### Features

- Compliant with SD Physical Specification Version 2.00
- Supports 1-bit and 4-bit SD Mode
- Supports Standard and High Capacity operations
- Supports Default and High Speed Modes of operation
- Supports all mandatory slave registers set
- CID Register fields are configured
- Supports only Standard command set
- Supports all mandatory SD Command Classes
- CRC7 checking/generation for Command/Response
- CRC16 checking/generation for Data transfer
- Support Maximum block length of 512 bytes
- Supports Single and Multiple block read and write data transfer
- Supports Partial and Misalign Block length option
- SD Memory only implementation
- IP provides simple and general-purpose interface or AXI4-lite or AHB interface to user application

## iW SD Memory Slave Controller Block Diagram



### Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual
- Simulation Environment
- BareMetal driver reference

### Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License – Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License – Single Site or Multi Site

### Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave Systems, a leading FPGA design house enhances your design productivity by providing an extensive suite of proven, optimized and easy-to-use FPGA IP Cores along with reference designs to complement and quicken your applications development. Our extensive suite of IP Cores covers all key markets and applications. Along with the rich set of FPGA IP cores, iWave offers custom FPGA designs tailored to meet the client specifications which includes RTL Design, Integration of iWave's or 3rd Party IP Cores on our FPGA SOMs with Carrier Card/ Custom Hardware/ Off-the-Shelf Evaluation Kits to provide end-to-end solutions targeting Low-Power, High-Performance and Optimized Designs

### iW – SD Memory Slave Controller 2.0 FPGA IP

The IP can be ordered online from the iWave Website <http://www.iwavesystems.com/product/sd-memory-slave-controller>  
Or from our Local Partners in your region <http://www.iwavesystems.com/about-us/business-partner.html>

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