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FPGA IP CORE

iW- 80188XL Processor IP

The 80188XL is a powerful 16-bit microprocessor core, executes instruction list compatible with 80188XL microprocessor. The 80188XL core has a broad set of integrated peripherals, which helps reduce system development time and cost and is compatible with wide range of compilers and debuggers. The design along with multiple peripherals can be fit into single FPGA.

Highlights

- Quick migration of 80188XL based designs to an FPGA platform
- Replacement for 80188XL processor and ASICs

Features

- **80188XL CPU Core**
  - Multiplexed 20-bit address and 8-bit data bus
  - 1M-byte memory space divided into 4 segments
  - 64K-byte IO space
  - Non Maskable Interrupt support
  - Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16 x 16-bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)

- **CPU On-Chip Peripherals**
  - Programmable Timer / Counter Unit
    - Three programmable independent 16-bit timers
    - TOUT0 to TOUT1 pin outputs
    - TIN0 & TIN1 used either as clock or control signals
    - Timer-2 can be used to clock other two timers
    - Internal / external input clock selectable
  - Direct Memory Access Unit
    - Two independent high-speed DMA channels.
    - Data can be transferred between any combination of memory & IO space.
    - DMA transfer can be initiated by external, internal request or by direct programming.
    - 20-bit length address register.
    - 16-bit length transfer count register.
    - Transfer address can be incrementing, decrementing or remained constant.
    - Two kinds of channel priority order
    - Fixed priority
    - Rotating priority
    - DMAU can be programmed to produce interrupt request when its transfer count reaches zero.
    - Both byte & word transfer is possible in case of 80186XL; word transfer is illegal in case of 80188XL processor.
  - Interrupt Control Unit
    - Four external interrupt request inputs (INT0 to INT3).
    - Timer0, Timer1, Timer2 and DMA0, DMA1 Interrupts (Internal Interrupts)
    - Edge or level triggered interrupt request inputs.
    - Individually Mask-able interrupts request
    - Programmable interrupt request priority orders.
    - Polling operation capability.
    - Cascade with external 8259A interrupts (only on INT0 and INT1) operates in either Master mode or Slave mode.
    - Special fully nested mode support
  - Chip Select Unit
    - Thirteen programmable chip-select outputs
    - Six of the chip-selects map only into memory address space, while the remaining seven can map into either memory or I/O address space
    - Programmable block size and start / end address
    - Memory or I/O bus cycle decoder
    - Programmable wait-state generator
    - Provision to disable a chip-select
    - Provision to override bus ready
  - Clock Generator

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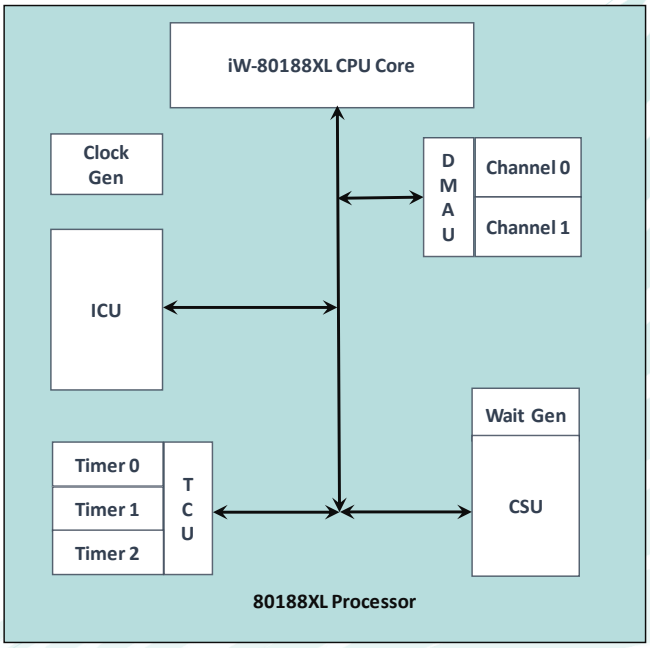
iW 80188XL Processor IP block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual

Licensing Options

- Non-Transferable: Single Project/Product Netlist License – Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License – Single Site or Multi Site
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Technical Support

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- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
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iW- 80188XL Processor FPGA IP
The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/80188xl-processor/
Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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