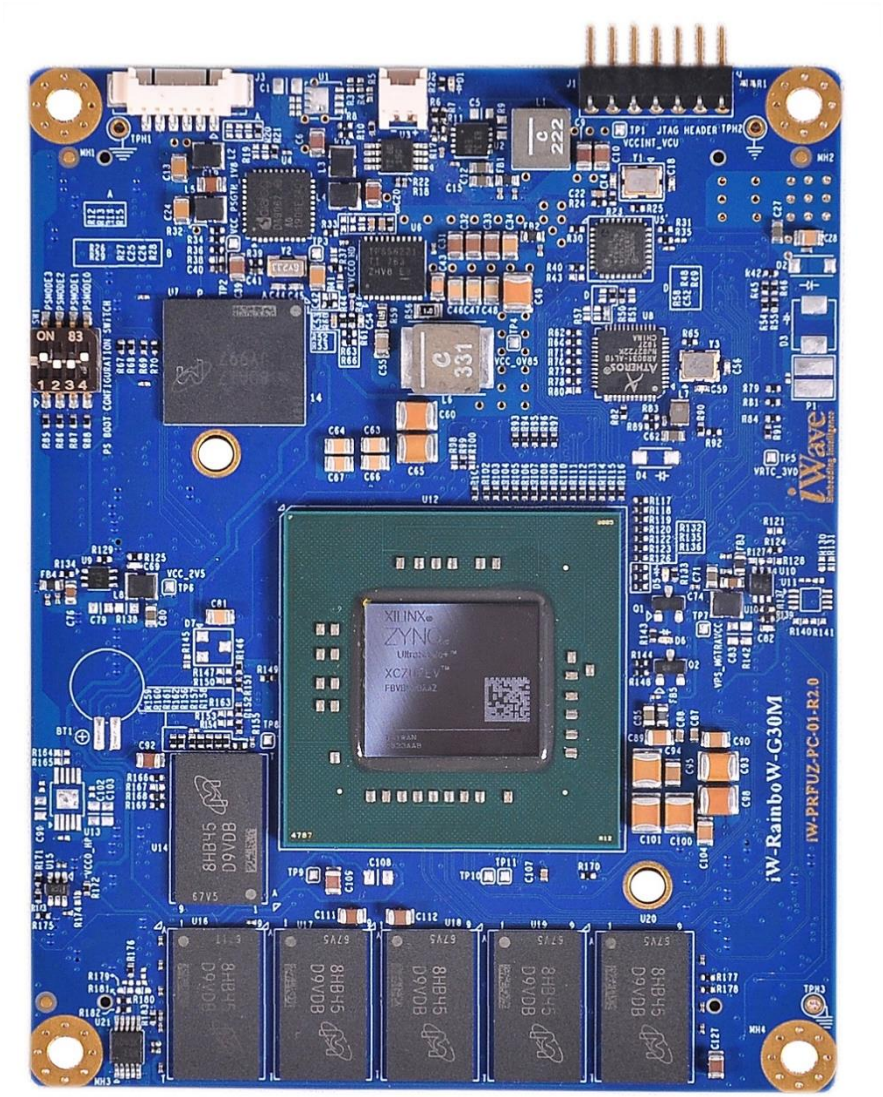
iW-RainboW-G30M
Zynq Ultrascale+ MPSoC SOM
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Zynq Ultrascale+ MPSoC System on Module based on the Xilinx Zynq Ultrascale+ MPSoC. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the Zynq Ultrascale+ MPSoC System on Module from a Hardware Systems perspective.

1.2 SOM Overview

The Zynq Ultrascale+ MPSoC SOM is an extension of Zynq Ultrascale+ MPSoC. Zynq Ultrascale+ MPSoC SOM has a form factor of 95mm x 75mm and provides the functional requirements for an embedded application. Two high speed ruggedized terminal strip connectors provide the carrier board interface to carry all the I/O signals to and from the Ultrascale+ MPSoC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ADC	Analog to Digital Converter
ARM	Advanced RISC Machine
BSP	Board Support Package
CAN	Controller Area Network
CPU	Central Processing Unit
DDR4 SDRAM	Double Data Rate fourth-generation Synchronous Dynamic Random Access Memory
FPGA	Field Programmable Gate Array
eMMC	Embedded Multimedia Card
GB	Giga Byte
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GHz	Giga Hertz
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group
Kbps	Kilobits per second
LVDS	Low Voltage Differential Signalling
MAC	Media Access Controller
MB	Mega Byte
Mbps	Megabits per sec

Acronyms	Abbreviations
MHz	Mega Hertz
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PMIC	Power Management Integrated IC
PTH	Plated Through hole
PL	Programmable Logic
PS	Processing System
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SGMII	Serial Gigabit Media Independent Interface
SoC	System On Chip
SOM	System On Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus
USB OTG	USB On The Go
UTMI	USB2.0 Transceiver Macrocell Interface

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB	Universal Serial Bus differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SOM.

1.5 References

- Zynq Ultrascale+ MPSoC Technical Reference Manual
- Zynq Ultrascale+ MPSoC Device Overview

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq Ultrascale+ MPSoC SOM features and Hardware architecture with high level block diagram. Also, this section provides detailed information about two Board to Board connector pin assignment and usage.

2.1 Zynq Ultrascale+ MPSoC SOM Block Diagram

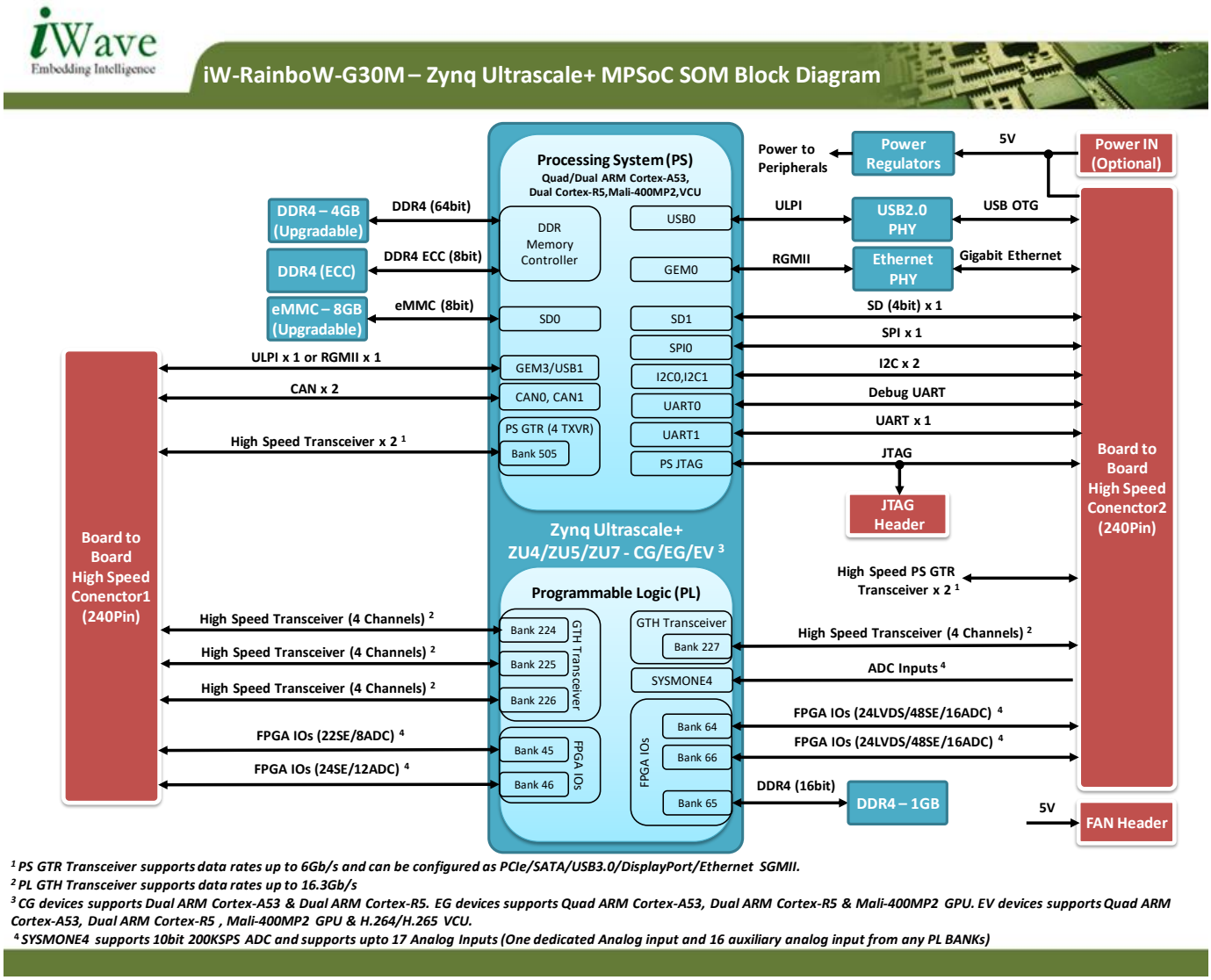


Figure 1: Zynq Ultrascale+ MPSoC SOM Block Diagram

2.2 Zynq Ultrascale+ MPSoC SOM Features

The Zynq Ultrascale+ MPSoC SOM supports the following features.

SoC

- Xilinx Zynq Ultrascale+ MPSoC
  - Compatible Zynq Ultrascale+ MPSoC Family (FBVB900) – ZU7EV, ZU5EV, ZU4EV
    Programming Logic with up to 504K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz), Mali™-400 MP2 Graphics Processor and H.264/H.265 Video Codec.
  - Compatible Zynq Ultrascale+ MPSoC Family (FBVB900) – ZU7EG, ZU5EG, ZU4EG
    Programming Logic with up to 504K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.5GHz), Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 600MHz) and Mali™-400 MP2 Graphics Processor.
  - Compatible Zynq Ultrascale+ MPSoC Family (FBVB900) – ZU7CG, ZU5CG, ZU4CG
    Programming Logic with up to 504K Logic cells and Processing System with integrated Quad-core ARM Cortex-A53 MPCore Application processor (up to 1.3GHz) and Dual-core ARM Cortex-R5 MPCore Real Time Processor (up to 533MHz).

PMIC

- Dialog's DA9062 PMIC with RTC

Memory

- 4GB DDR4 SDRAM (64bit) with ECC for PS (Expandable)
- 1GB DDR4 SDRAM (16bit) for PL (Expandable)
- 8GB eMMC Flash (Expandable)

Other On-SOM Features

- Gigabit Ethernet PHY Transceiver
- USB2.0 Transceiver
- JTAG Header
- Fan Header

Board to Board Connector1 Interfaces

From PS Block

- PS-GTR High Speed Transceivers (upto 6Gbps) x 2[3]
- RGMII Interface or ULPI Interface x 1 Port
- CAN x 2 Ports

From PL Block

- PL-GTH High Speed Transceivers (upto 16.3Gbps) x 12[3]
- PL IOs - HD Bank45[2, 3]
  - Upto 11 DIFF IOs/22 Single ended (SE) IOs
    - Upto 3 HDGC Global Clock Input pins (LVDS/SE)
    - Upto 8 ADC Input pins (Differential/Single Ended)
- PL IOs - HD Bank46[2, 3]
  - Upto 12 DIFF IOs/24 Single Ended (SE) IOs
    - Upto 4 HDGC Global Clock Input pins (LVDS/SE)
    - Upto 12 ADC Input pins (Differential/Single Ended)

Board to Board Connector2 Interfaces

From PS Block

- PS-GTR High Speed Transceivers (upto 6Gbps) x 2
- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- USB2.0 OTG x 1 Port (through On-SOM USB2.0 transceiver)
- SD (4bit) x 1 Port
- SPI x 1 Port
- Debug UART x 1 Port
- Data UART x 1 Port
- I2C x 2 Ports
- PS JTAG

From PL Block

- PL-GTH High Speed Transceivers (upto 16.3Gbps) x4[3]
- PL IOs - HP Bank64[2, 3]
  - Upto 24 LVDS IOs/48 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 16 ADC Input pins (Differential/Single Ended)
- PL IOs - HP Bank66[2, 3]
  - Upto 24 LVDS IOs/48 Single ended (SE) IOs
    - Upto 4 GC Global Clock Input pins (LVDS/SE)
    - Upto 16 ADC Input pins (Differential/Single Ended)

General Specification

- Power Supply : 5V (from Board to Board Connector2)
- Form Factor : 95mm x 75mm

[1] *In Zynq Ultrascale+ MPSoC PS, GEM3 RGMII interface & USB1 ULPI interface signals are multiplexed in same pins and so either GEM3 or USB1 only can be supported.*

[2] *In Zynq Ultrascale+ MPSoC SOM, PL BANK45 & BANK46 supports variable IO voltage setting and configurable through software.*

[3] *In Zynq Ultrascale+ MPSoC SOM, All the differential signals, PS-GTR Transceivers and GTH Transceivers are routed in 100 Ohm.*

Important Note: Zynq Ultrascale+ MPSoC SOM, All the GTH, GTR transceivers and PL Bank pair's P & N(Intra pair) are length matched within 1ps with internal 7EV MPSoC package delay . Inter Pair length match is not done. To add delay tuning in carrier board wherever required.

2.3 Zynq Ultrascale+ MPSoC

Xilinx's SoC portfolio integrates the software programmability of a processor with the hardware programmability of an FPGA, providing unrivalled levels of system performance, flexibility, and scalability. Unlike traditional SoC processing solutions, the flexible programmable logic provides optimization and differentiation, allowing to add the peripherals and accelerators for a broad base of applications.

The Zynq Ultrascale+ MPSoC SOM is based on Xilinx Zynq Ultrascale+ MPSoC with FBVB900 package. Zynq Ultrascale+ MPSoC family integrates Processing system (PS) and Xilinx programmable logic (PL) in a single device. MPSoC's Processing system includes feature-rich Quad-core ARM Cortex-A53 MPCore up to 1.5 GHz of Application processor, Dual-core ARM Cortex-R5 MPCore up to 600MHz, Mali™-400 MP2 of Graphics Processor and H.264/H.265 of Video Codec. The Block Diagram of Zynq Ultrascale+ MPSoC from Xilinx website is shown below for reference.

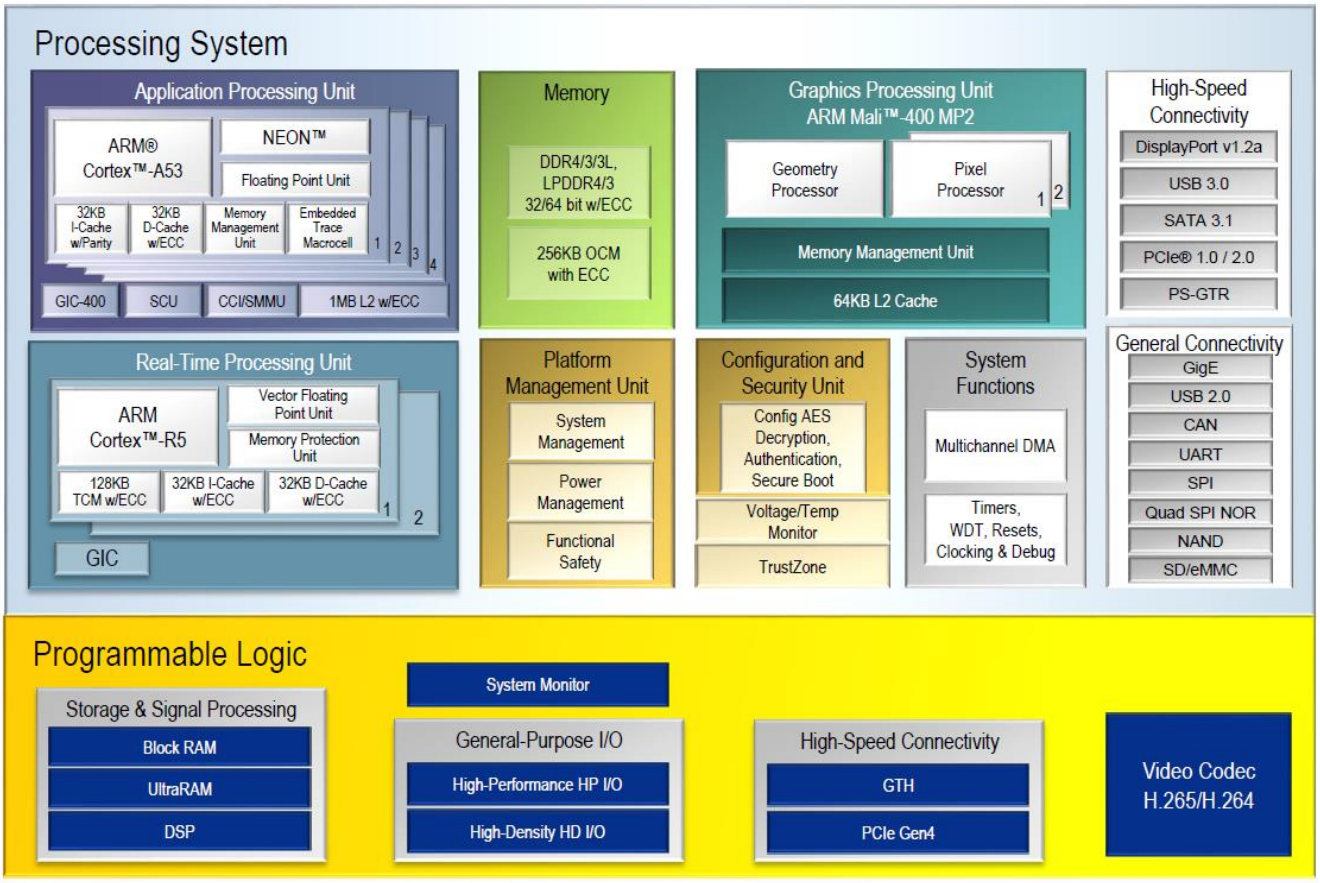


Figure 2: Zynq Ultrascale+ MPSoC CPU Simplified Block Diagram

Note: Please refer the latest Zynq Ultrascale+ MPSoC Datasheet & Technical Reference Manual for more details which may be revised from time to time.

The Zynq Ultrascale+ MPSoC SOM is compatible to ZU7EV, ZU5EV, ZU4EV, ZU7EG, ZU5EG, ZU4EG, ZU7CG, ZU5CG and ZU4CG MPSoC devices and feature comparison between these devices are shown below.

	ZU4CG	ZU5CG	ZU7CG	ZU4EG	ZU5EG	ZU7EG	ZU4EV	ZU5EV	ZU7EV
Application Processing Unit	Dual-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point;32KB/32KB L1 Cache, 1MB L2 Cache			Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point; 32KB/32KB L1 Cache, 1MB L2 Cache			Quad-core Arm Cortex-A53 MPCore with CoreSight; NEON & Single/Double Precision Floating Point;32KB/32KB L1 Cache, 1MB L2 Cache		
Real-Time Processing Unit	Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM			Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1 Cache, and TCM			Dual-core Arm Cortex-R5 with CoreSight; Single/Double Precision Floating Point; 32KB/32KB L1, Cache, and TCM		
Embedded and External Memory	256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3;External Quad-SPI; NAND; eMMC			256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3;External Quad-SPI; NAND; eMMC			256KB On-Chip Memory w/ECC; External DDR4; DDR3; DDR3L; LPDDR4; LPDDR3;External Quad-SPI; NAND; eMMC		
General Connectivity	214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple,Timer Counters			214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters			214 PS I/O; UART; CAN; USB 2.0; I2C; SPI; 32b GPIO; Real Time Clock; WatchDog Timers; Triple Timer Counters		
High-Speed Connectivity	4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII			4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII			4 PS-GTR; PCIe Gen1/2; Serial ATA 3.1; DisplayPort 1.2a; USB 3.0; SGMII		
Graphic Processing Unit	NA			Arm Mali™-400 MP2; 64KB L2 Cache			Arm Mali™-400 MP2; 64KB L2 Cache		
Video Codec	NA			NA			1	1	1
System Logic Cells	1,92,150	2,56,200	5,04,000	1,92,150	2,56,200	5,04,000	1,92,150	2,56,200	5,04,000
CLB Flip-Flops	1,75,680	2,34,240	4,60,800	1,75,680	2,34,240	4,60,800	1,75,680	2,34,240	4,60,800
CLB LUTs	87,840	1,17,120	2,30,400	87,840	1,17,120	2,30,400	87,840	1,17,120	2,30,400
Distributed RAM (Mb)	2.6	3.5	6.2	2.6	3.5	6.2	2.6	3.5	6.2
Block RAM Blocks	128	144	312	128	144	312	128	144	312
Block RAM (Mb)	4.5	5.1	11	4.5	5.1	11	4.5	5.1	11
UltraRAM Blocks	48	64	96	48	64	96	48	64	96
UltraRAM (Mb)	13.5	18	27	13.5	18	27	13.5	18	27
DSP Slices	728	1,248	1,728	728	1,248	1,728	728	1,248	1,728
CMTs	4	4	4	4	4	4	4	4	4
Max. HP I/O	156	156	156	156	156	156	156	156	156
Max. HD I/O	48	48	48	48	48	48	48	48	48
System Monitor	2	2	2	2	2	2	2	2	2
GTH Transceiver 16.3Gb/s	16	16	16	16	16	16	16	16	16
Transceiver Fractional PLLs	8	8	8	8	8	8	8	8	8
PCIe Gen3 x16	2	2	2	2	2	2	2	2	2

Changes from left side.

Figure 3: Zynq Ultrascale+ MPSoC Devices Comparison

The Zynq Ultrascale+ MPSoC's PS has 78 dedicated I/O pins referred as MIO (Multiplexed I/O) for the PS peripheral interfaces. These 78 MIO pins are divided into three banks (PS BANK500, 501 & 502) and each bank includes 26 device pins. Since 78 MIO pins are not enough to support simultaneous use of all the peripherals supported by PS, there is option in MPSoC to route most of the IO peripheral interfaces to PL Bank I/O pins referred as EMIO (Extended MIO). Zynq Ultrascale+ MPSoC's PS Peripheral Pin mapping options between MIO & EMIO is shown below.

Peripheral Interface	MIO	EMIO
Quad-SPI NAND	Yes	No
USB2.0: 0,1	Yes: External PHY	No
SDIO 0,1	Yes	Yes
SPI: 0,1 I2C: 0,1 CAN: 0,1 GPIO	Yes CAN: External PHY GPIO: Up to 78 bits	Yes CAN: External PHY GPIO: Up to 96 bits
GigE: 0,1,2,3	RGMII v2.0: External PHY	Supports GMII, RGMII v2.0 (HSTL), RGMII v1.3, MII, SGMII, and 1000BASE-X in Programmable Logic
UART: 0,1	Simple UART: Only two pins (TX and RX)	Full UART (TX, RX, DTR, DCD, DSR, RI, RTS, and CTS) requires either: • Two Processing System (PS) pins (RX and TX) through MIO and six additional Programmable Logic (PL) pins, or • Eight Programmable Logic (PL) pins
Debug Trace Ports	Yes: Up to 16 trace bits	Yes: Up to 32 trace bits
Processor JTAG	Yes	Yes

The Zynq Ultrascale+ MPSoC's PL Banks are classified as high-performance (HP) banks or high-density (HD) banks. The HP Bank I/Os are optimized for highest performance operation organized in banks of 52pins. The HD Bank I/Os are reduced-feature I/Os organized in banks of 24pins.

In Zynq Ultrascale+ MPSoC PL, each bank supports four global clock (GC or HDGC) input pin pairs. GC pins have direct access to the global clock buffers, MMCMs and PLLs of the same Bank. HDGC pins are from HD I/O banks and have direct access only to the global clock buffers.

Also Zynq Ultrascale+ MPSoC supports two types of high speed transceivers namely GTH and PS-GTR. These transceivers are arranged in groups of four known as a transceiver Quad. GTH transceivers are from PL and PS-GTR transceivers are from PS.

2.3.1 MPSoC Power

The Zynq Ultrascale+ MPSoC SOM uses discrete power regulators along with DA9062 PMIC from Dialog Semiconductor for MPSoC power management. In SOM, PS low-power domain, PS full-power domain & PL power domain supply voltage (VCC_PSINTLP, VCC_PSINTFP, VCCINT) is fixed to 0.85V or 0.9V based on the speed grade of the MPSoC. Also all PS Bank (VCCO_PSIO) I/O voltage is fixed to 1.8V.

The I/O voltage of PL HP Banks (PL Bank 64 & 66) which are connected to Board to Board Connectors is fixed to 1.8V. The I/O voltage of PL HD Banks (PL Bank 45 & 46) which are connected to Board to Board Connectors are generated from PMIC LDO3 and by default set to 1.8V. I/O voltage is configurable through software after bootup.

2.3.2 MPSoC Reset

The Zynq Ultrascale+ MPSoC SOM uses PMIC's Reset output (nRESET) for PS Power On Reset and connected to PS_POR_B pin of MPSoC. Also it supports warm reset input from Board to Board Connector2 pin35 and connected to PS_SRST_B pin of MPSoC.

2.3.3 MPSoC Reference Clock

The Zynq Ultrascale+ MPSoC SOM supports on board clock oscillators for reference clock to different blocks of Zynq Ultrascale+ MPSoC. These reference clock details are mentioned in the below table.

Table 3: Zynq Ultrascale+ MPSoC SOM Reference Clock.

Sl. No	On-SOM Oscillator Frequency	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description	Stability
1	33.33MHz	PS_REF_CLK	503	P19	1.8V, LVCMOS	33.33Mhz single ended reference clock for PS.	±50ppm
2	100MHz[1]	IO_L5P_HDGC_45	45	G16	1.8V, LVCMOS	100Mhz single ended reference clock for PL.	±25ppm
3	300MHz	IO_L11P_T1U_N8_GC_65	65	AG8	1.8V, LVDS	LVDS reference clock for PL DDR4. This is connected to Bank65 General Purpose Clock Input pin through 0.1uf AC Caps.	±100ppm
		IO_L11N_T1U_N9_GC_65		AH8			

[1] Important Note: I/O voltage of PL Bank45 is software configurable. Since this oscillator supports 1.8V to 3.3V VCC only, this reference clock can be used only if the I/O voltage of PL Bank45 is set between 1.8V to 3.3V.

[2] Mentioned voltage level is based on default I/O voltage set to PL Bank45.

2.3.4 MPSoC Configuration & Status

The Zynq Ultrascale+ MPSoC uses multi-stage boot process that supports both a non-secure and a secure boot. The PS is the master of the boot and configuration process. Upon reset, device executes code out of on-chip ROM and copies the first stage boot loader (FSBL) from the boot device to the on-chip RAM. The FSBL initiates the boot of the PS and can load and configure the PL or configuration of the PL can be deferred to a later stage.

The Zynq Ultrascale+ MPSoC SOM supports two LEDs (D6 & D5) for the MPSoC error status indication namely PS_ERROR_OUT and PS_ERROR_STATUS. LED D6 is for PS_ERROR_OUT and it is asserted for accidental loss of power, a hardware error, or an exception in the PMU. LED D5 is for PS_ERROR_STATUS and it indicates a secure lockdown state. Alternatively, it can be used by the PMU firmware to indicate system status.

The Zynq Ultrascale+ MPSoC SOM supports three dedicated input and output configuration pins. By default, Weak pre-reconfiguration I/O pull-up resistors disabled for PUDC_B pin, Standard PL power-on delay time for POR_OVERRIDE pin and PS-Done pin is connected to VCC_1V8 through 4.7K.

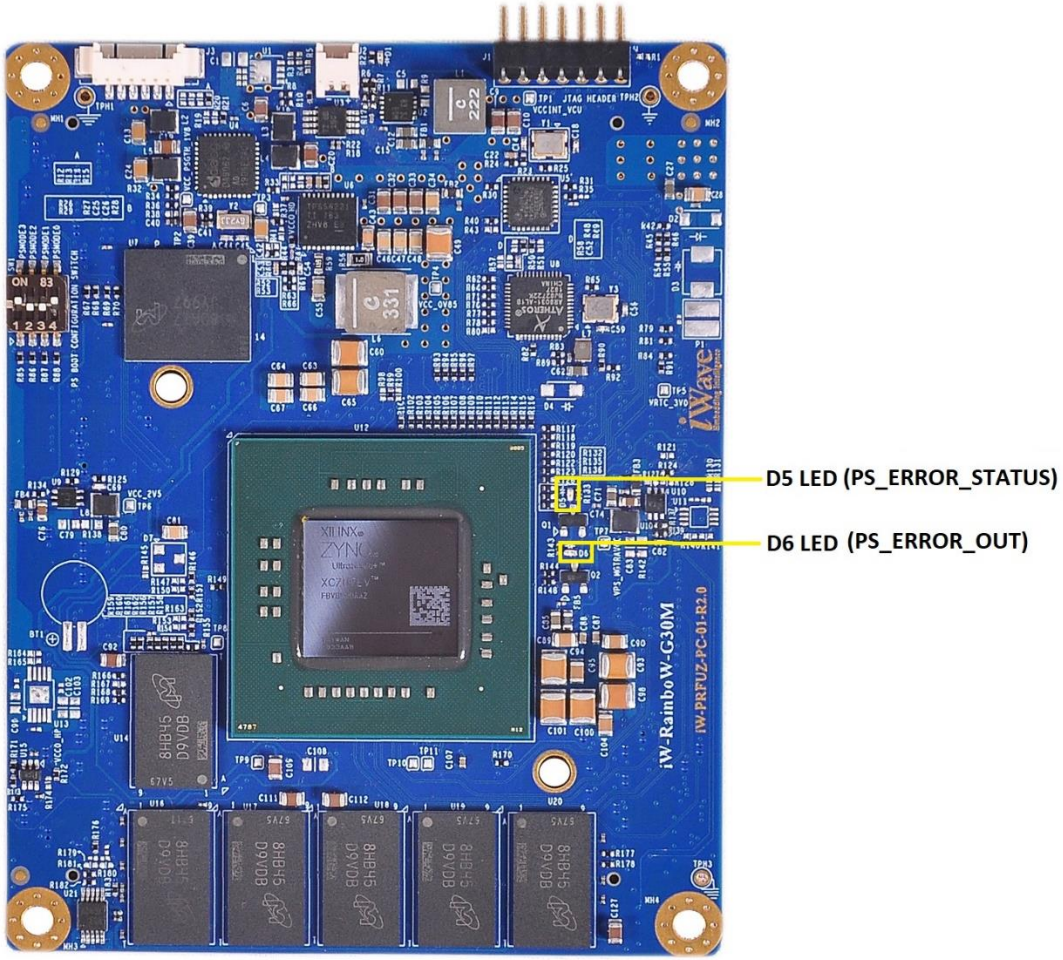


Figure 4: Error Status Indication LEDs

2.3.5 MPSoC Boot Mode Switch

The Zynq Ultrascale+ MPSoC always boots from PS first and configures the PL through software. MPSoC can support eMMC, SD1, USB0 & JTAG as boot device and configurable through mode pins. Upon device reset, MPSoC mode pins are read to determine the primary boot device.

The Zynq Ultrascale+ MPSoC SOM supports Boot Mode switch (SW1) to select the required boot device. By default, eMMC is supported as boot device. Refer the below table to select the required boot device.

Table 4: Boot Mode Switch Truth Table

Zynq Ultrascale+ MPSoC Boot Mode	SW1 (4 Position Switch)				
	PS Mode 3	PS Mode 2	PS Mode 1	PS Mode 0	Switch Position Image
PS JTAG	OFF	OFF	OFF	OFF	
SD1	OFF	ON	OFF	ON	
eMMC (Default)	OFF	ON	ON	OFF	
USB0	OFF	ON	ON	ON	

2.3.6 MPSoC System Monitor/ADC

The Zynq Ultrascale+ MPSoC contain two System Monitor block (SYSMONE4), one in the PL (PL SYSMON) and another in the PS (PS SYSMON). It is used to enhance the overall safety, security and reliability of the system by monitoring the physical environment via on-chip power supply and temperature sensors.

The PL SYSMON uses 10-bit 200kSPS ADC to digitize the sensor/ADC inputs. It monitors the die temperature in the PL and several internal PL and PS power supply nodes. The PL SYSMON can also monitor up to 17 external analog channels which includes 16 auxiliary analog inputs and one VP_VN dedicated input. The external auxiliary inputs can be routed through any PL Bank. The ADC voltage reference is selectable between an internal reference and the external pins VREFP and VREFN. In Zynq Ultrascale+ MPSoC SOM, 1.25V external voltage reference is supported.

The PS SYSMON uses 10-bit 1MSPS ADC to digitize the sensor inputs. It is located in the PS LPD and monitors two temperature points & several internal fixed voltage nodes. The PS has two temperature sensors, one is physically located in the PS SYSMON near the RPU. The second, remote sensor is located in the FPD near the APU. The ADC always uses an internally generated voltage reference.

2.4 PMIC with RTC

The Zynq Ultrascale+ MPSoC SOM supports Dialog semiconductor DA9062 PMIC. The I2C0 module of Zynq Ultrascale+ MPSoC PS is used for PMIC interface through MIO pins with I2C address 0x58.

PMIC's LDO3 is connected to I/O voltage of PL HD Banks (PL Bank 45 & 46) and by default set to 1.8V. The I/O voltage is configurable through software after bootup. PMIC supports reset output and connected to Zynq Ultrascale+ MPSoC PS (PS_POR_B) for power on reset. Also PMIC supports IRQ output for events indication and connected to MPSoC's PS GPIO (PS_MIO2_500).

The PMIC supports Real Time Clock functionality. It uses the Coin cell battery power from Board to Board Connector2 pin68 for RTC backup power. The PMIC can support backup battery charging to charge Lithium-Manganese coin cell batteries and super capacitors if required.

2.5 Memory

2.5.1 DDR4 SDRAM with ECC for PS

The Zynq Ultrascale+ MPSoC SOM supports 64bit, 4GB DDR4 RAM memory for MPSoC's PS. Four 16 bit, 1GB DDR4 SDRAM ICs are used to support a total on board RAM memory of 4GB. Also, Zynq Ultrascale+ MPSoC SOM supports 8bit ECC for RAM memory. These DDR4 devices operates at 1.2 voltage level. DDR4 memory is connected to the hard memory controller of the MPSoC PS. The RAM size can be expandable up to maximum of 32GB based on the availability of higher density 16bit DDR4 device.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.2 DDR4 SDRAM for PL

The Zynq Ultrascale+ MPSoC SOM supports 16bit, 1GB DDR4 RAM memory for MPSoC's PL. One 16 bit, 1GB DDR4 SDRAM IC is used to support RAM memory of 1GB for PL. This device operates at 1.2 voltage level. In Zynq Ultrascale+ MPSoC SOM, Bank65 is used for PL DDR4 interface. The RAM size can be expandable up to maximum of 4GB based on the availability of higher density 16bit DDR4 device.

The Zynq Ultrascale+ MPSoC SOM supports 300MHz LVDS Oscillator on board for PL DDR4 reference clock and connected to Bank65 AG8 & AH8 dedicated clock input pins through AC Coupling capacitors.

*Note: Refer **ORDERING INFORMATION** section for exact RAM size used on the SOM based on the Product Part Number.*

2.5.3 eMMC Flash

The Zynq Ultrascale+ MPSoC SOM supports 8GB eMMC Flash memory for Boot & Storage of Zynq Ultrascale+ MPSoC PS. This eMMC Flash memory is directly connected to the SD0 controller of the MPSOC's PS through MIO pins and operates at 1.8V Voltage level. This SD/SDIO controller supports eMMC4.51 standard with up to 8bit HS200 mode. The eMMC Flash size can be expandable up to maximum of 128GB based on the availability of higher density eMMC Flash device.

*Note: Refer **ORDERING INFORMATION** section for exact eMMC Flash size used on the SOM based on the Product Part Number.*

2.6 On SOM Fearures

2.6.1 JTAG Header

The Zynq Ultrascale+ MPSoC SOM supports 14Pin JTAG Header (J1) for JTAG interface. JTAG Interface Signals are directly connected from MPSoC's PS BANK 503 to this Header and operates at 1.8V Voltage level. JTAG interface signals are also connected to Board to Board Connector2 to access from carrier board.

Internally the Zynq Ultrascale+ MPSoC implements both an ARM debug access port (DAP) inside PS as well as a standard JTAG test access port (TAP) controller inside the PL. The JTAG Header (J1) is physically located on topside of the SOM as shown below. JTAG-HS2 Programming Cable can be directly connected to this JTAG Header.

Number of Pins - 14
Connector Part - 877601416 from Molex
Mating Connector - 0791077006 from Molex

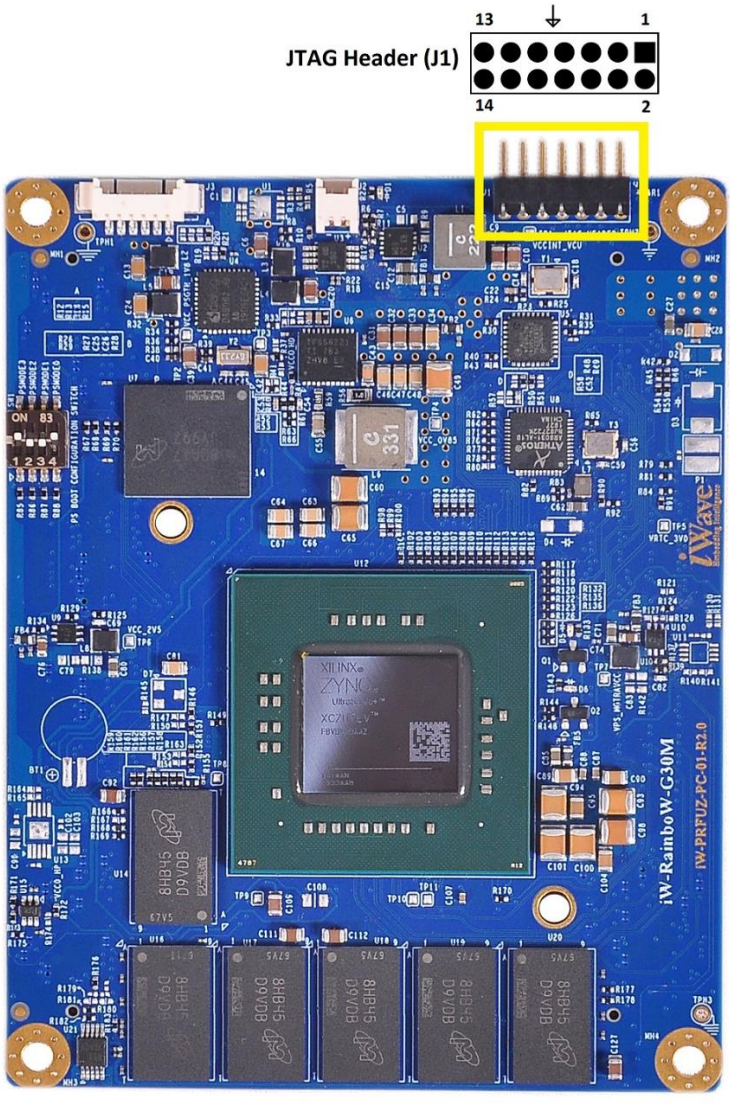


Figure 5: JTAG Header

Table 5: JTAG Header Pinout

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	NC	-			-	NC.
2	VCC_1V8	-	-	-	O, 1.8V Power	Supply Voltage.
3	GND	-	-	-	Power	Ground.
4	PS_JTAG_TMS	PS_JTAG_TMS	503	L21	I, 1.8V LVCMOS/4.7K PU	JTAG Test Mode Select.
5	GND	-	-	-	Power	Ground.
6	PS_JTAG_TCK	PS_JTAG_TCK	503	L19	I, 1.8V LVCMOS/4.7K PU	JTAG Test Clock.
7	GND	-			Power	Ground.
8	PS_JTAG_TDO	PS_JTAG_TDO	503	M20	O, 1.8V/LVCMOS	JTAG Test Data Output.
9	GND	-	-	-	Power	Ground.
10	PS_JTAG_TDI	PS_JTAG_TDI	503	L20	I, 1.8V LVCMOS/4.7K PU	JTAG Test Data Input.
11	GND	-	-	-	Power	Ground.
12	NC	-	-	-	-	NC.
13	GND	-	-	-	Power	Ground.
14	JTAG_RESETB	-	-	-	I, 1.8V LVCMOS/10K PU	JTAG Test Reset.

2.6.2 Fan Header

The Zynq Ultrascale+ MPSoC SOM supports a Fan Header (J2) to connect cooling Fan if required. Also in SOM, there are mounting holes in either side of the MPSoC device which can be used to fix the heatsink & Fan if required. The Fan Header (J2) is physically located on topside of the SOM as shown below.

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

Compatible Fan (Example) - AFB0505MB from Delta Electronics

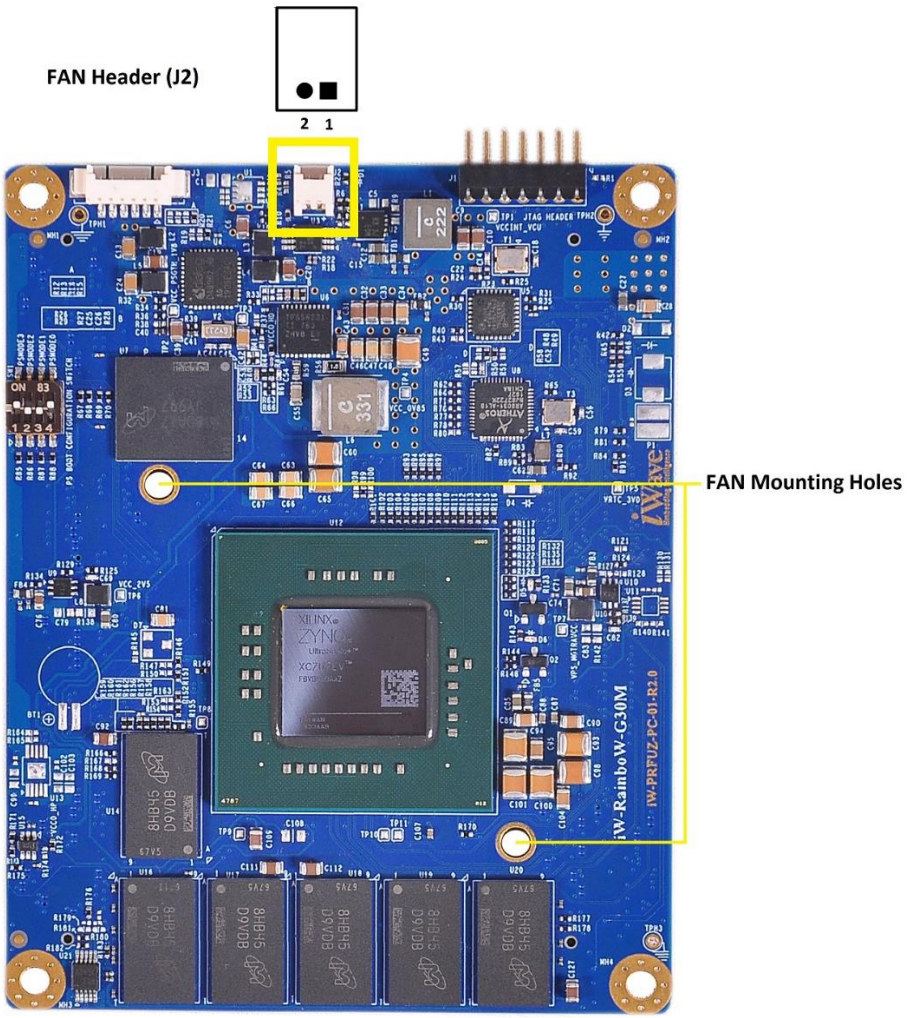


Figure 6: Fan Header

Table 6: Fan Header Pinout

Pin No	Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1	VCC_5V	-	-	-	O, 5V Power	Supply Voltage.
2	GND	-	-	-	Power	Ground.

2.7 Board to Board Connector1

The Zynq Ultrascale+ MPSoC SOM supports two 240pin High speed ground plane ruggedized terminal strip Connectors for interfaces expansion. All the effort is made in Zynq Ultrascale+ MPSoC SOM design to provide the maximum interfaces of Zynq Ultrascale+ MPSoC to the carrier board by adding these two Board to Board Connectors.

The Zynq Ultrascale+ MPSoC SOM Board to Board Connector1 pinout is provided in the below table and the interfaces which are available at Board to Board Connector1 are explained in the following sections. The Board to Board Connector1 (J5) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240
Connector Part Number - QTH-120-01-L-D-A
Mating Connector - QSH-120-01-L-D-A from Samtech
Staking Height - 5mm

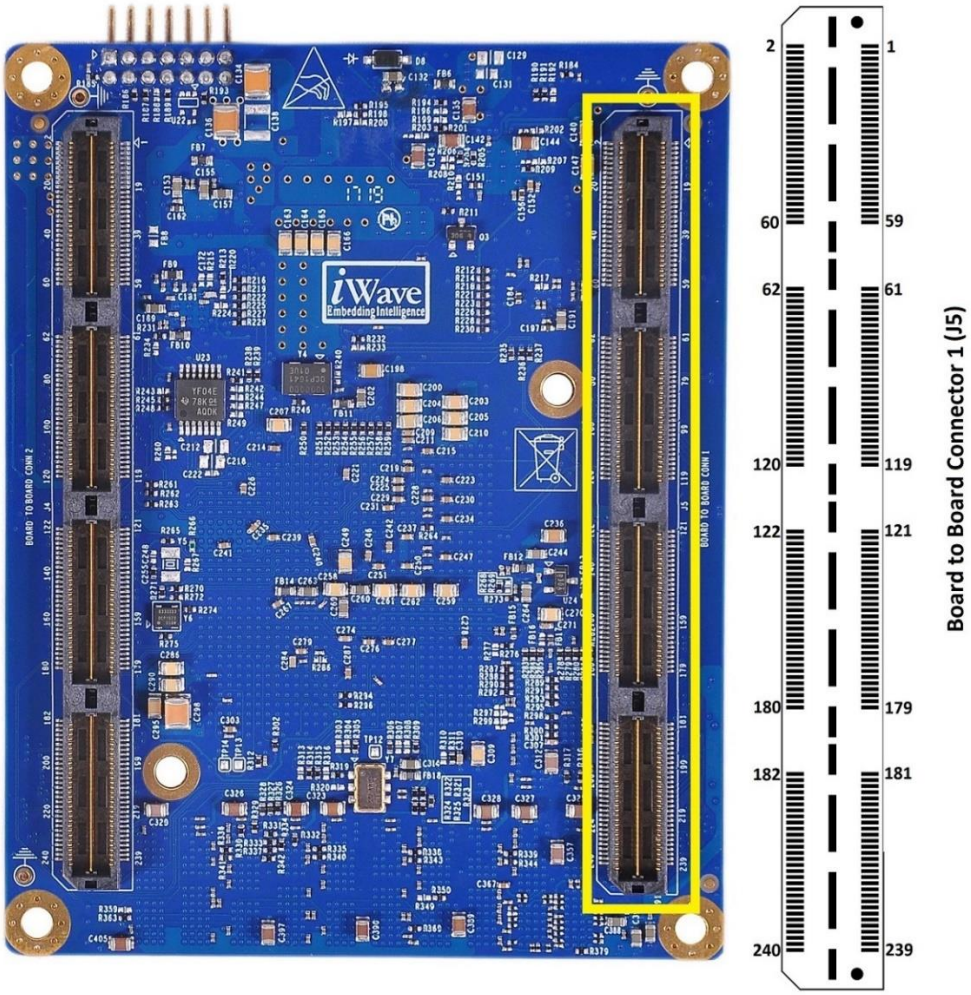


Figure 7: Board to Board Connector1

Table 7: Board to Board Connector1 Pinout

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GND	1	2	GND
GTHTXP0_223	3	4	GTREFCLK0P_223
GTHTXN0_223	5	6	GTREFCLK0N_223
GND	7	8	GND
GTHTXP1_223	9	10	NC
GTHTXN1_223	11	12	PL_A17_LVDS45_L11P
GND	13	14	PL_A16_LVDS45_L11N
GTHRXN1_223	15	16	PL_C17_LVDS45_L10P
GTHRXP1_223	17	18	PL_B16_LVDS45_L10N
GND	19	20	GND
GTHRXN0_223	21	22	PL_D15_LVDS45_L8N_HDGC
GTHRXP0_223	23	24	PL_E15_LVDS45_L8P_HDGC
GND	25	26	GND
PL_B15_LVDS45_L12P	27	28	PL_L14_LVDS45_L1N
PL_A15_LVDS45_L12N	29	30	PL_L15_LVDS45_L1P
PL_D16_LVDS45_L9P	31	32	PL_K15_LVDS45_L2P
PL_C16_LVDS45_L9N	33	34	PL_K14_LVDS45_L2N
GND	35	36	GND
GTHTXP2_223	37	38	PL_J16_LVDS45_L4P
GTHTXN2_223	39	40	PL_H16_LVDS45_L4N
GND	41	42	PL_J14_LVDS45_L3N
GTHTXP3_223	43	44	PL_J15_LVDS45_L3P
GTHTXN3_223	45	46	PL_A14_LVDS46_L11P
GND	47	48	PL_A13_LVDS46_L11N
GTHRXN3_223	49	50	PL_B12_LVDS46_L12P
GTHRXP3_223	51	52	PL_A12_LVDS46_L12N
GND	53	54	GND
GTHRXN2_223	55	56	PL_D17_LVDS45_L7N_HDGC
GTHRXP2_223	57	58	PL_E17_LVDS45_L7P_HDGC
GND	59	60	GND
Key			**Key**
GND	61	62	GND
PS_MGTRTXP0_505	63	64	GTREFCLK1P_223
PS_MGTRTXN0_505	65	66	GTREFCLK1N_223
GND	67	68	GND
NC	69	70	PL_C14_LVDS46_L10P
NC	71	72	PL_B14_LVDS46_L10N
GND	73	74	PL_D12_LVDS46_L9P
PS_MGTREFCLK0N_505	75	76	PL_C12_LVDS46_L9N
PS_MGTREFCLK0P_505	77	78	NC
GND	79	80	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
PS_MGTRRXN0_505	81	82	PL_F15_LVDS45_L6N_HDGC
PS_MGTRRXP0_505	83	84	PL_F16_LVDS45_L6P_HDGC
GND	85	86	GND
PL_K12_LVDS46_L1P	87	88	PL_G14_LVDS46_L4N
PL_K11_LVDS46_L1N	89	90	PL_H14_LVDS46_L4P
PL_K13_LVDS46_L2P	91	92	PL_H13_LVDS46_L3P
PL_J12_LVDS46_L2N	93	94	PL_H12_LVDS46_L3N
GND	95	96	GND
GTHTXP0_224	97	98	GTREFCLK0P_224
GTHTXN0_224	99	100	GTREFCLK0N_224
GND	101	102	GND
GTHTXP1_224	103	104	NC
GTHTXN1_224	105	106	NC
GND	107	108	NC
GTHRXN1_224	109	110	NC
GTHRXP1_224	111	112	NC
GND	113	114	GND
GTHRXN0_224	115	116	PL_F13_LVDS46_L5N_HDGC
GTHRXP0_224	117	118	PL_G13_LVDS46_L5P_HDGC
GND	119	120	GND
Key			**Key**
GND	121	122	GND
GTHTXP2_224	123	124	PL_F12_LVDS46_L6P_HDGC
GTHTXN2_224	125	126	PL_E12_LVDS46_L6N_HDGC
GND	127	128	NC
GTHTXP3_224	129	130	PL_E14_LVDS46_L7P_HDGC
GTHTXN3_224	131	132	PL_E13_LVDS46_L7N_HDGC
GND	133	134	NC
GTHRXN3_224	135	136	NC
GTHRXP3_224	137	138	NC
GND	139	140	GND
GTHRXN2_224	141	142	PL_C13_LVDS46_L8N_HDGC
GTHRXP2_224	143	144	PL_D14_LVDS46_L8P_HDGC
GND	145	146	GND
NC	147	148	NC
NC	149	150	NC
NC	151	152	NC
NC	153	154	NC
GND	155	156	GND
PS_MGTRTXP1_505	157	158	GTREFCLK1P_224
PS_MGTRTXN1_505	159	160	GTREFCLK1N_224
GND	161	162	GND

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
NC	163	164	NC
NC	165	166	NC
GND	167	168	NC
PS_MGTREFCLK1N_505	169	170	NC
PS_MGTREFCLK1P_505	171	172	NC
GND	173	174	GND
PS_MGTRRXN1_505	175	176	NC
PS_MGTRRXP1_505	177	178	SPI0_SS2(PS_MIO1_500)
GND	179	180	GND
Key			**Key**
GND	181	182	GND
GTHTXP0_225	183	184	GTREFCLK0P_225
GTHTXN0_225	185	186	GTREFCLK0N_225
GND	187	188	GND
GTHTXP1_225	189	190	GEM3_TX_CLK/USB1_CLK(PS_MIO 64_502)
GTHTXN1_225	191	192	GEM3_TXD0/USB1_DIR(PS_MIO65 _502)
GND	193	194	GEM3_TXD1/USB1_DATA2(PS_MIO 66_502)
GTHRXN1_225	195	196	GEM3_TXD2/USB1_NXT(PS_MIO67 _502)
GTHRXP1_225	197	198	GEM3_TXD3/USB1_DATA0(PS_MIO 68_502)
GND	199	200	GND
GTHRXN0_225	201	202	NC
GTHRXP0_225	203	204	NC
GND	205	206	GND
CAN0_RX(PS_MIO38_501)	207	208	NC
CAN0_TX(PS_MIO39_501)	209	210	GEM3_TX_CTL/USB1_DATA1(PS_M IO69_502)
CAN1_RX(PS_MIO41_501)	211	212	GEM3_RX_CLK/USB1_STP(PS_MIO 70_502)
CAN1_TX(PS_MIO40_501)	213	214	GEM3_RX_CTL/USB1_DATA7(PS_M IO75_502)
GND	215	216	GND
GTHTXP2_225	217	218	GTREFCLK1P_225
GTHTXN2_225	219	220	GTREFCLK1N_225
GND	221	222	GND
GTHTXP3_225	223	224	GEM3_RXD0/USB1_DATA3 (PS_MIO71_502)

Signal Name	B2B-1 Pin	B2B-1 Pin	Signal Name
GTHTXN3_225	225	226	GEM3_RXD1/USB1_DATA4(PS_MIO 72_502)
GND	227	228	GEM3_RXD2/USB1_DATA5(PS_MIO 73_502)
GTHRXN3_225	229	230	GEM3_RXD3/USB1_DATA6(PS_MIO 74_502)
GTHRXP3_225	231	232	SOMPWR_EN
GND	233	234	GND
GTHRXN2_225	235	236	NC
GTHRXP2_225	237	238	NC
GND	239	240	GND

Important Note: The signal name (with ball name) in pinout is mentioned based on the ZU4/5 device

2.7.1 PS Interfaces

The interfaces which are supported in Board to Board Connector1 from Zynq Ultrascale+ MPSoC's PS is explained in the following section.

2.7.1.1 PS-GTR Transceivers

The Zynq Ultrascale+ MPSoC supports four Multi-Gigabit PS-GTR transceivers with data rate from 1.25Gbps to 6.0Gbps. This PS-GTR transceiver lanes provide I/O path for MPSoC MAC controllers and their link partner outside. At any given time, these four lanes can be used for any of below mentioned peripheral standards.

- x1, x2, or x4 lane of PCIe at Gen1 (2.5Gb/s) or Gen2 (5.0Gb/s) rates
- 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 or 2 SATA channels at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
- 1 or 2 USB3.0 channels at 5.0Gb/s
- 1-4 Ethernet SGMII channels at 1.25Gb/s

The available peripheral standard option for each PS-GTR transceiver lane in Zynq Ultrascale+ MPSoC is shown below. This is user programmable via the high-speed I/O multiplexer (HS-MIO) of MPSoC.

PS Peripheral Interface	Lane0	Lane1	Lane2	Lane3
PCIe (x1, x2 or x4)	PCIe0	PCIe1	PCIe2	PCIe3
SATA (1 or 2 channels)	SATA0	SATA1	SATA0	SATA1
DisplayPort (TX only)	DP1	DP0	DP1	DP0
USB0	USB0	USB0	USB0	-
USB1	-	-	-	USB1
SGMII0	SGMII0	-	-	-
SGMII1	-	SGMII1	-	-
SGMII2	-	-	SGMII2	-
SGMII3	-	-	-	SGMII3

The Zynq Ultrascale+ MPSoC SOM supports two PS GTR transceivers (Lane0 & Lane1) on Board to Board Connector1 and another two PS GTR transceivers (Lane2 & Lane3) on Board to Board Connector2. Each PS GTR transceiver lane supports one dedicated reference clock input pair with the ability to share reference clocks between lanes.

In Zynq Ultrascale+ MPSoC SOM, the end user is responsible for sourcing the reference clocks to the PS-GTR lanes through Board to Board Connectors. This gives full flexibility to end user to select the required peripheral standards on PS-GTR lanes.

For more details on PS-GTR transceiver pinouts on Board to Board Connector1, refer the below table.

Table 8: PS-GTR pinout description

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
PS-GTR Lane0 Pins						
63	PS_MGTRTXP0_505	PS_MGTRTXP0_505	505	M27	O, DIFF	PS-GTR Lane0 High speed differential transmitter positive.
65	PS_MGTRTXN0_505	PS_MGTRTXN0_505	505	M28	O, DIFF	PS-GTR Lane0 High speed differential transmitter negative.
75	PS_MGTREFCLK0N_505	PS_MGTREFCLK0N_505	505	M24	I, DIFF	PS-GTR Lane0 differential reference clock negative.
77	PS_MGTREFCLK0P_505	PS_MGTREFCLK0P_505	505	M23	I, DIFF	PS-GTR Lane0 differential reference clock positive.
81	PS_MGTRRXN0_505	PS_MGTRRXN0_505	505	L30	I, DIFF	PS-GTR Lane0 High speed differential receiver negative.
83	PS_MGTRRXP0_505	PS_MGTRRXP0_505	505	L29	I, DIFF	PS-GTR Lane0 High speed differential receiver positive.
PS-GTR Lane1 Pins						
157	PS_MGTRTXP1_505	PS_MGTRTXP1_505	505	K27	O, DIFF	PS-GTR Lane1 High speed differential transmitter positive.
159	PS_MGTRTXN1_505	PS_MGTRTXN1_505	505	K28	O, DIFF	PS-GTR Lane1 High speed differential transmitter negative.
169	PS_MGTREFCLK1N_505	PS_MGTREFCLK1N_505	505	L26	I, DIFF	PS-GTR Lane1 differential reference clock negative.
171	PS_MGTREFCLK1P_505	PS_MGTREFCLK1P_505	505	L25	I, DIFF	PS-GTR Lane1 differential reference clock positive.
175	PS_MGTRRXN1_505	PS_MGTRRXN1_505	505	J30	I, DIFF	PS-GTR Lane1 High speed differential receiver negative.
177	PS_MGTRRXP1_505	PS_MGTRRXP1_505	505	J29	I, DIFF	PS-GTR Lane1 High speed differential receiver positive.

2.7.1.2 RGMII/ULPI Interface

The Zynq Ultrascale+ MPSoC SOM supports RGMII or ULPI interface on Board to Board Connector1. In Zynq Ultrascale+ MPSoC PS, GEM3 RGMII interface and USB1 ULPI interface are multiplexed on the same pins. So either one interface only can be used at a time. In Zynq Ultrascale+ MPSoC SOM, these MIO pins are directly connected from MPSoC to Board to Board conenctor1. If RGMII/ULPI interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.9** for available alternate functions.

The Zynq Ultrascale+ MPSoC gigabit Ethernet controller (GEM) implements a 10/100/1000 Mb/s Ethernet MAC that is compatible with the IEEE Standard for Ethernet (IEEE Std 802.3-2008). GEM controller supports MDIO interface for external PHY Management and it can be used through any PL Bank IOs through EMIO interface in SOM.

The Zynq Ultrascale+ MPSoC USB2.0 OTG controller is capable for USB2.0 implementations as a host, a device, or On-the-Go. This controller uses the ULPI protocol to connect external ULPI PHY. Also this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes.

For more details on RGMII/ULPI Interface pinouts on Board to Board Connector1, refer the below table.

Table 9: RGMII/ULPI Interface pinout description

B2B1 Pin No	B2B Connector 1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
190	GEM3_TX_CLK/USB1_CLK(PS_MIO64_502)	PS_MIO64_502	502	B30	O, 1.8V LVCMOS	GEM3 RGMII Transmit Clock or USB1 ULPI Clock.
192	GEM3_TXD0/USB1_DIR(PS_MIO65_502)	PS_MIO65_502	502	D25	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA0 or USB1 ULPI Direction Control.
194	GEM3_TXD1/USB1_DATA2(PS_MIO66_502)	PS_MIO66_502	502	C27	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA1 or USB1 ULPI Bi-Directional Data2.
196	GEM3_TXD2/USB1_NXT(PS_MIO67_502)	PS_MIO67_502	502	C28	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA2 or USB1 ULPI NXT.
198	GEM3_TXD3/USB1_DATA0(PS_MIO68_502)	PS_MIO68_502	502	C29	O, 1.8V LVCMOS	GEM3 RGMII Transmit DATA3 or USB1 ULPI Bi-Directional Data0.
210	GEM3_TX_CTL/USB1_DATA1(PS_MIO69_502)	PS_MIO69_502	502	D27	O, 1.8V LVCMOS	GEM3 RGMII Transmit Control or USB1 ULPI Bi-Directional Data1.
212	GEM3_RX_CLK/USB1_STP(PS_MIO70_502)	PS_MIO70_502	502	D26	I, 1.8V LVCMOS	GEM3 RGMII Receive Clock or USB1 ULPI STP.

B2B1 Pin No	B2B Connector 1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
214	GEM3_RX_CTL/USB1_DATA7(PS_MIO75_502)	PS_MIO75_502	502	D29	I, 1.8V LVCMOS	GEM3 RGMII Receive control or USB1 ULPI Bi-Directional Data7.
224	GEM3_RXD0/USB1_DATA3(PS_MIO71_502)	PS_MIO71_502	502	D30	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA0 or USB1 ULPI Bi-Directional Data3.
226	GEM3_RXD1/USB1_DATA4(PS_MIO72_502)	PS_MIO72_502	502	E27	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA1 or USB1 ULPI Bi-Directional Data4.
228	GEM3_RXD2/USB1_DATA5(PS_MIO73_502)	PS_MIO73_502	502	E30	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA2 or USB1 ULPI Bi-Directional Data5.
230	GEM3_RXD3/USB1_DATA6(PS_MIO74_502)	PS_MIO74_502	502	E29	I, 1.8V LVCMOS	GEM3 RGMII Receive DATA3 or USB1 ULPI Bi-Directional Data6.

** Signal direction is mentioned considering GEM3 RGMII interface.*

2.7.1.3 CAN Interface

The Zynq Ultrascale+ MPSoC SOM supports two CAN interfaces on Board to Board Connector1. The CAN0 & CAN1 controller of MPSoC's PS is used for CAN interface through MIO pins. This CAN controller is compatible with the ISO 11898-1, CAN 2.0A, and CAN 2.0B standards. And it supports bit rates up to 1Mb/s.

If CAN interface is not required on these pins, the same pins can be used as GPIOs or other alternate functions. Please refer PS Min Multiplexing section **2.9** for available alternate functions.

For more details on CAN Interface pinouts on Board to Board Connector1, refer the below table.

Table 10: CAN Interface pinouts

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
207	CAN0_RX (PS_MIO38_501)	PS_MIO38_501	501	C23	I, 1.8V LVCMOS	CAN0 Receive data.
209	CAN0_TX (PS_MIO39_501)	PS_MIO39_501	501	E22	O,1.8V LVCMOS	CAN0 Transmit data.
211	CAN1_RX (PS_MIO41_501)	PS_MIO41_501	501	D24	I, 1.8V LVCMOS	CAN1 Receive data.
213	CAN1_TX (PS_MIO40_501)	PS_MIO40_501	501	C24	O,1.8V LVCMOS	CAN0 Transmit data.

2.7.2 PL Interfaces

The interfaces which are supported in Board to Board Connector1 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.7.2.1 GTH High Speed Transceivers

The Zynq Ultrascale+ MPSoC supports 16 GTH transceivers through Four transceiver Quad (Bank 223, 224, 225 & 226) with line rate from 500Mbps to 16.375Gbps based on the speed grade of the MPSoC. These transceivers can be used to interface to multiple high-speed interface protocols. Each GTH transceiver quad supports two dedicated reference clock input pairs.

Zynq Ultrascale+ MPSoC Speed Grade	GTH Transceiver line rate (min)	GTH Transceiver line rate (max)
-1 Speed Grade	0.5 Gbps	12.5 Gbps
-2 Speed Grade	0.5 Gbps	16.375 Gbps
-3 Speed Grade	0.5 Gbps	16.375 Gbps

The Zynq Ultrascale+ MPSoC is capable of supporting the requirements for the different speed and temperature grade as shown below.

Zynq Ultrascale+ MPSoC Speed Grade	VCCINT	VCC_PSINTLP	VCC_PSINTFP	VCC_PSINTFP_DDR	Units
-3E Speed Grade	0.90	0.90	0.90	0.90	V
-2E Speed Grade	0.85	0.85	0.85	0.85	V
-2I Speed Grade	0.85	0.85	0.85	0.85	V
-2LE Speed Grade	0.85	0.85	0.85	0.85	V
-1E Speed Grade	0.85	0.85	0.85	0.85	V
-1I Speed Grade	0.85	0.85	0.85	0.85	V
-1Q Speed Grade	0.85	0.85	0.85	0.85	V
-1M Speed Grade	0.85	0.85	0.85	0.85	V
-1LI Speed Grade	0.85	0.85	0.85	0.85	V

Zynq Ultrascale+ MPSoC VCC_PSINTLP, VCC_PSINTFP, VCC_PSINTFP_DDR, VCCINT, VCCINT, VCCINT_IO, Voltages are sourced from the same regulator. By default, Zynq Ultrascale+ MPSoC 0.85V is sourced.

The Zynq Ultrascale+ MPSoC SOM Supports 12 GTH transceivers along with the reference clock inputs (Bank 223, 224 & 225) on Board to Board Conenctor1 and 4 GTH transceivers along with reference clock inputs (Bank 226) on Board to Board Connector2.

In Zynq Ultrascale+ MPSoC SOM, On board reference clock to the GTH transceiver quad is not supported. This must be fed from the carrier board based on the peripheral standards used on GTH transceivers. This gives full flexibility to end user to select the required peripheral standards on GTH transceivers. Also On board termination and AC coupling capacitor are not supported on transceiver lines and has to be taken care in the carrier board if required.

Note: In ZU7CG/7EG/7EV MPSoC devices, the transceiver Quad Bank223, 224, 225 & 226 is called as Bank224, 225 226 & 227 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on GTH transceiver pinouts on Board to Board Connector1, refer the below table.

Table 11: GTH Transceiver pinout description

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank223 Transceiver Quad Pins						
3	GTHTXP0_223	MGTHTXP0_223	223	W4	O, DIFF	GTH Bank223 channel0 High speed differential transmitter positive.
5	GTHTXN0_223	MGTHTXN0_223	223	W3	O, DIFF	GTH Bank223 channel0 High speed differential transmitter negative.
21	GTHRXN0_223	MGTHRXN0_223	223	V1	I, DIFF	GTH Bank223 channel0 High speed differential receiver negative.
23	GTHRXP0_223	MGTHRXP0_223	223	V2	I, DIFF	GTH Bank223 channel0 High speed differential receiver positive.
9	GTHTXP1_223	MGTHTXP1_223	223	V6	O, DIFF	GTH Bank223 channel1 High speed differential transmitter positive.
11	GTHTXN1_223	MGTHTXN1_223	223	V5	O, DIFF	GTH Bank223 channel1 High speed differential transmitter negative.
15	GTHRXN1_223	MGTHRXN1_223	223	U3	I, DIFF	GTH Bank223 channel1 High speed differential receiver negative.
17	GTHRXP1_223	MGTHRXP1_223	223	U4	I, DIFF	GTH Bank223 channel1 High speed differential receiver positive.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
37	GTHTXP2_223	MGTHTXP2_223	223	T6	O, DIFF	GTH Bank223 channel2 High speed differential transmitter positive.
39	GTHTXN2_223	MGTHTXN2_223	223	T5	O, DIFF	GTH Bank223 channel2 High speed differential transmitter negative.
55	GTHRXN2_223	MGTHRXN2_223	223	T1	I, DIFF	GTH Bank223 channel2 High speed differential receiver negative.
57	GTHRXP2_223	MGTHRXP2_223	223	T2	I, DIFF	GTH Bank223 channel2 High speed differential receiver positive.
43	GTHTXP3_223	MGTHTXP3_223	223	R4	O, DIFF	GTH Bank223 channel3 High speed differential transmitter positive.
45	GTHTXN3_223	MGTHTXN3_223	223	R3	O, DIFF	GTH Bank223 channel3 High speed differential transmitter negative.
49	GTHRXN3_223	MGTHRXN3_223	223	P1	I, DIFF	GTH Bank223 channel3 High speed differential receiver negative.
51	GTHRXP3_223	MGTHRXP3_223	223	P2	I, DIFF	GTH Bank223 channel3 High speed differential receiver positive.
4	GTREFCLK0P_223	MGTREFCLK0P_223	223	R8	I, DIFF	GTH Bank223 differential reference clock0 positive.
6	GTREFCLK0N_223	MGTREFCLK0N_223	223	R7	I, DIFF	GTH Bank223 differential reference clock0 negative.
64	GTREFCLK1P_223	MGTREFCLK1P_223	223	N8	I, DIFF	GTH Bank223 differential reference clock1 positive.
66	GTREFCLK1N_223	MGTREFCLK1N_223	223	N7	I, DIFF	GTH Bank223 differential reference clock1 negative.
Bank224 Transceiver Quad Pins						
97	GTHTXP0_224	MGTHTXP0_224	224	P6	O, DIFF	GTH Bank224 channel0 High speed differential transmitter positive.
99	GTHTXN0_224	MGTHTXN0_224	224	P5	O, DIFF	GTH Bank224 channel0 High speed differential transmitter negative.
115	GTHRXN0_224	MGTHRXN0_224	224	N3	I, DIFF	GTH Bank224 channel0 High speed differential receiver negative.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
117	GTHRXP0_224	MGTHRXP0_224	224	N4	I, DIFF	GTH Bank224 channel0 High speed differential receiver positive.
103	GTHTXP1_224	MGTHTXP1_224	224	M6	O, DIFF	GTH Bank224 channel1 High speed differential transmitter positive.
105	GTHTXN1_224	MGTHTXN1_224	224	M5	O, DIFF	GTH Bank224 channel1 High speed differential transmitter negative.
109	GTHRXN1_224	MGTHRXN1_224	224	M1	I, DIFF	GTH Bank224 channel1 High speed differential receiver negative.
111	GTHRXP1_224	MGTHRXP1_224	224	M2	I, DIFF	GTH Bank224 channel1 High speed differential receiver positive.
123	GTHTXP2_224	MGTHTXP2_224	224	L4	O, DIFF	GTH Bank224 channel2 High speed differential transmitter positive.
125	GTHTXN2_224	MGTHTXN2_224	224	L3	O, DIFF	GTH Bank224 channel2 High speed differential transmitter negative.
141	GTHRXN2_224	MGTHRXN2_224	224	K1	I, DIFF	GTH Bank224 channel2 High speed differential receiver negative.
143	GTHRXP2_224	MGTHRXP2_224	224	K2	I, DIFF	GTH Bank224 channel2 High speed differential receiver positive.
129	GTHTXP3_224	MGTHTXP3_224	224	K6	O, DIFF	GTH Bank224 channel3 High speed differential transmitter positive.
131	GTHTXN3_224	MGTHTXN3_224	224	K5	O, DIFF	GTH Bank224 channel3 High speed differential transmitter negative.
135	GTHRXN3_224	MGTHRXN3_224	224	J3	I, DIFF	GTH Bank224 channel3 High speed differential receiver negative.
137	GTHRXP3_224	MGTHRXP3_224	224	J4	I, DIFF	GTH Bank224 channel3 High speed differential receiver positive.
98	GTREFCLK0P_224	MGTREFCLK0P_224	224	L8	I, DIFF	GTH Bank224 differential reference clock0 positive.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
100	GTREFCLK0N_224	MGTREFCLK0N_224	224	L7	I, DIFF	GTH Bank224 differential reference clock0 negative.
158	GTREFCLK1P_224	MGTREFCLK1P_224	224	J8	I, DIFF	GTH Bank224 differential reference clock1 positive.
160	GTREFCLK1N_224	MGTREFCLK1N_224	224	J7	I, DIFF	GTH Bank224 differential reference clock1 negative.
Bank225 Transceiver Quad Pins						
183	GTHTXP0_225	MGTHTXP0_225	225	H6	O, DIFF	GTH Bank225 channel0 High speed differential transmitter positive.
185	GTHTXN0_225	MGTHTXN0_225	225	H5	O, DIFF	GTH Bank225 channel0 High speed differential transmitter negative.
201	GTHRXN0_225	MGTHRXN0_225	225	H1	I, DIFF	GTH Bank225 channel0 High speed differential receiver negative.
203	GTHRXP0_225	MGTHRXP0_225	225	H2	I, DIFF	GTH Bank225 channel0 High speed differential receiver positive.
189	GTHTXP1_225	MGTHTXP1_225	225	G8	O, DIFF	GTH Bank225 channel1 High speed differential transmitter positive.
191	GTHTXN1_225	MGTHTXN1_225	225	G7	O, DIFF	GTH Bank225 channel1 High speed differential transmitter negative.
195	GTHRXN1_225	MGTHRXN1_225	225	G3	I, DIFF	GTH Bank225 channel1 High speed differential receiver negative.
197	GTHRXP1_225	MGTHRXP1_225	225	G4	I, DIFF	GTH Bank225 channel1 High speed differential receiver positive.
217	GTHTXP2_225	MGTHTXP2_225	225	F6	O, DIFF	GTH Bank225 channel2 High speed differential transmitter positive.
219	GTHTXN2_225	MGTHTXN2_225	225	F5	O, DIFF	GTH Bank225 channel2 High speed differential transmitter negative.
235	GTHRXN2_225	MGTHRXN2_225	225	F1	I, DIFF	GTH Bank225 channel2 High speed differential receiver negative.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
237	GTHRXP2_225	MGTHRXP2_225	225	F2	I, DIFF	GTH Bank225 channel2 High speed differential receiver positive.
223	GTHTXP3_225	MGTHTXP3_225	225	E8	O, DIFF	GTH Bank225 channel3 High speed differential transmitter positive.
225	GTHTXN3_225	MGTHTXN3_225	225	E7	O, DIFF	GTH Bank225 channel3 High speed differential transmitter negative.
229	GTHRXN3_225	MGTHRXN3_225	225	E3	I, DIFF	GTH Bank225 channel3 High speed differential receiver negative.
231	GTHRXP3_225	MGTHRXP3_225	225	E4	I, DIFF	GTH Bank225 channel3 High speed differential receiver positive.
184	GTREFCLK0P_225	MGTREFCLK0P_225	225	H10	I, DIFF	GTH Bank225 differential reference clock0 positive.
186	GTREFCLK0N_225	MGTREFCLK0N_225	225	H9	I, DIFF	GTH Bank225 differential reference clock0 negative.
218	GTREFCLK1P_225	MGTREFCLK1P_225	225	F10	I, DIFF	GTH Bank225 differential reference clock1 positive.
220	GTREFCLK1N_225	MGTREFCLK1N_225	225	F9	I, DIFF	GTH Bank225 differential reference clock1 negative.

2.7.2.2 PL IOs – HD BANK45

The Zynq Ultrascale+ MPSoC SOM supports 11 Differential IOs/22 Single Ended (SE) IOs on Board to Board Connector1 from MPSoC's PL High-Density (HD) Bank45. Upon these 11 Differential IOs/22 SE IOs, upto 3 HDGC Global Clock Inputs and upto 8 PLSYSMON auxiliary analog inputs are available.

The IO voltage of PL Bank45 (& Bank46) is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as Differential IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for PL Bank45. By default, IO voltage of PL Bank45 is set as 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank45 signals are routed as Differential IOs to Board to Board Connector1. Even though PL Bank45 signals are routed as Differential IOs, these pins can be used as SE IOs if required. The Board to Board Connector1 pins 22, 24, 56, 58, 82 & 84 are HDGC Global Clock Input capable pins of PL Bank45. Also Board to Board Connector1 pins 12, 14, 18, 16, 27, 28, 29, 30, 31, 32, 33, 34, 38, 40, 42 & 44 are PLSYSMON auxiliary analog Input capable pins of PL Bank45.

Note: In ZU7CG/7EG/7EV MPSoC devices, the PL Bank45 & PL Bank46 is called as PL Bank48 and PL Bank47 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank45 pinouts on Board to Board Connector1, refer the below table.

Table 12: PL IO HD Bank45 pinout description

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
12	PL_A17_LVDS45_L11P	IO_L11P_AD9P_45	45	A17	IO, 1.8V	PL Bank45 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
14	PL_A16_LVDS45_L11N	IO_L11N_AD9N_45	45	A16	IO, 1.8V	PL Bank45 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
16	PL_C17_LVDS45_L10P	IO_L10P_AD10P_45	45	C17	IO, 1.8V	PL Bank45 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
18	PL_B16_LVDS45_L10N	IO_L10N_AD10N_45	45	B16	IO, 1.8V	PL Bank45 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
22	PL_D15_LVDS45_L8N_HDGC	IO_L8N_HDGC_45	45	D15	IO, 1.8V	PL Bank45 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
24	PL_E15_LVDS45_L8P_HDGC	IO_L8P_HDGC_45	45	E15	IO, 1.8V	PL Bank45 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
27	PL_B15_LVDS45_L12P	IO_L12P_AD8P_45	45	B15	IO, 1.8V	PL Bank45 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
28	PL_L14_LVDS45_L1N	IO_L1N_AD15N_45	45	L14	IO, 1.8V	PL Bank45 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
29	PL_A15_LVDS45_L12N	IO_L12N_AD8N_45	45	A15	IO, 1.8V	PL Bank45 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
30	PL_L15_LVDS45_L1P	IO_L1P_AD15P_45	45	L15	IO, 1.8V	PL Bank45 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
31	PL_D16_LVDS45_L9P	IO_L9P_AD11P_45	45	D16	IO, 1.8V	PL Bank45 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
32	PL_K15_LVDS45_L2P	IO_L2P_AD14P_45	45	K15	IO, 1.8V	PL Bank45 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
33	PL_C16_LVDS45_L9N	IO_L9N_AD11N_45	45	C16	IO, 1.8V	PL Bank45 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
34	PL_K14_LVDS45_L2N	IO_L2N_AD14N_45	45	K14	IO, 1.8V	PL Bank45 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
38	PL_J16_LVDS45_L4P	IO_L4P_AD12P_45	45	J16	IO, 1.8V	PL Bank45 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
40	PL_H16_LVDS45_L4N	IO_L4N_AD12N_45	45	H16	IO, 1.8V	PL Bank45 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
42	PL_J14_LVDS45_L3N	IO_L3N_AD13N_45	45	J14	IO, 1.8V	PL Bank45 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
44	PL_J15_LVDS45_L3P	IO_L3P_AD13P_45	45	J15	IO, 1.8V	PL Bank45 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
56	PL_D17_LVDS45_L7N_HDGC	IO_L7N_HDGC_45	45	D17	IO, 1.8V	PL Bank45 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
58	PL_E17_LVDS45_L7P_HDGC	IO_L7P_HDGC_45	45	E17	IO, 1.8V	PL Bank45 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.
82	PL_F15_LVDS45_L6N_HDGC	IO_L6N_HDGC_45	45	F15	IO, 1.8V	PL Bank45 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or Single ended I/O.
84	PL_F16_LVDS45_L6P_HDGC	IO_L6P_HDGC_45	45	F16	IO, 1.8V	PL Bank45 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or Single ended I/O.

**IO Type of IOs originating from ZU7/5/4 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU7/5/4 MPSoC datasheet.*

2.7.2.3 PL IOs – HD BANK46

The Zynq Ultrascale+ MPSoC SOM supports 12 Differential IOs/24 Single Ended (SE) IOs on Board to Board Connector1 from MPSoC's PL High-Density (HD) Bank46. Upon these 12 Differential IOs/24 SE IOs, upto 4 HDGC Global Clock Inputs and upto 12 PLSYSMON auxiliary analog inputs are available.

The IO voltage of Bank46 (& Bank45) is connected from LDO3 output of the PMIC and supports variable IO voltage setting. IO voltage is configurable from 1.2V to 3.3V through software. While using as Differential IOs or Single Ended IOs, make sure to set the PMIC LDO3 to output appropriate IO voltage for PL Bank46. By default, IO voltage of PL Bank46 is set as 1.8V. For more details about supported IO standard, refer the Zynq Ultrascale+ MPSoC datasheet.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank46 signals are routed as Differential IOs to Board to Board Connector1. Even though PL Bank46 signals are routed as Differential IOs, these pins can be used as SE IOs if required. The Board to Board Connector1 pins 116, 118, 124, 126, 130, 132, 142 & 144 are HDGC Global Clock Input capable pins of PL Bank46. Also Board to Board Connector1 pins 46, 48, 50, 52, 70, 72, 74, 76, 87, 88, 89, 90, 91, 92, 93, 94, 116, 118, 124, 126, 130, 132, 142 & 144 are PLSYSMON auxiliary analog Input capable pins of PL Bank46.

Note: In ZU7CG/7EG/7EV MPSoC devices, the PL Bank45 & PL Bank46 is called as PL Bank48 and PL Bank47 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on PL HD Bank46 pinouts on Board to Board Connector1, refer the below table.

Table 13: PL IO HD Bank46 pinout description

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
46	PL_A14_LVDS46_L11P	IO_L11P_AD1P_46	46	A14	IO, 1.8V	PL Bank46 IO11 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
48	PL_A13_LVDS46_L11N	IO_L11N_AD1N_46	46	A13	IO, 1.8V	PL Bank46 IO11 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
50	PL_B12_LVDS46_L12P	IO_L12P_AD0P_46	46	B12	IO, 1.8V	PL Bank46 IO12 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
52	PL_A12_LVDS46_L12N	IO_L12N_AD0N_46	46	A12	IO, 1.8V	PL Bank46 IO12 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
70	PL_C14_LVDS46_L10P	IO_L10P_AD2P_46	46	C14	IO, 1.8V	PL Bank46 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
72	PL_B14_LVDS46_L10N	IO_L10N_AD2N_46	46	B14	IO, 1.8V	PL Bank46 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
74	PL_D12_LVDS46_L9P	IO_L9P_AD3P_46	46	D12	IO, 1.8V	PL Bank46 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
76	PL_C12_LVDS46_L9N	IO_L9N_AD3N_46	46	C12	IO, 1.8V	PL Bank46 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
87	PL_K12_LVDS46_L1P	IO_L1P_AD11P_46	46	K12	IO, 1.8V	PL Bank46 IO1 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
89	PL_K11_LVDS46_L1N	IO_L1N_AD11N_46	46	K11	IO, 1.8V	PL Bank46 IO1 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
91	PL_K13_LVDS46_L2P	IO_L2P_AD10P_46	46	K13	IO, 1.8V	PL Bank46 IO2 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
93	PL_J12_LVDS46_L2N	IO_L2N_AD10N_46	46	J12	IO, 1.8V	PL Bank46 IO2 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
88	PL_G14_LVDS46_L4N	IO_L4N_AD8N_46	46	G14	IO, 1.8V	PL Bank46 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
90	PL_H14_LVDS46_L4P	IO_L4P_AD8P_46	46	H14	IO, 1.8V	PL Bank46 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
92	PL_H13_LVDS46_L3P	IO_L3P_AD9P_46	46	H13	IO, 1.8V	PL Bank46 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
94	PL_H12_LVDS46_L3N	IO_L3N_AD9N_46	46	H12	IO, 1.8V	PL Bank46 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
116	PL_F13_LVDS46_L5N_HDGC	IO_L5N_HDGC_AD7N_46	46	F13	IO, 1.8V	PL Bank46 IO5 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input7 negative or Single ended I/O.
118	PL_G13_LVDS46_L5P_HDGC	IO_L5P_HDGC_AD7P_46	46	G13	IO, 1.8V	PL Bank46 IO5 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input7 positive or Single ended I/O.

B2B1 Pin No	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
124	PL_F12_LVDS46_L6P_HDGC	IO_L6P_HDGC_AD6P_46	46	F12	IO, 1.8V	PL Bank46 IO6 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input6 positive or Single ended I/O.
126	PL_E12_LVDS46_L6N_HDGC	IO_L6N_HDGC_AD6N_46	46	E12	IO, 1.8V	PL Bank46 IO6 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input6 negative or Single ended I/O.
130	PL_E14_LVDS46_L7P_HDGC	IO_L7P_HDGC_AD5P_46	46	E14	IO, 1.8V	PL Bank46 IO7 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input5 positive or Single ended I/O.
132	PL_E13_LVDS46_L7N_HDGC	IO_L7N_HDGC_AD5N_46	46	E13	IO, 1.8V	PL Bank46 IO7 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input5 negative or Single ended I/O.
142	PL_C13_LVDS46_L8N_HDGC	IO_L8N_HDGC_AD4N_46	46	C13	IO, 1.8V	PL Bank46 IO8 differential negative. Same pin can be configured as HDGC Global Clock Input differential negative or PLSYSMON differential analog input4 negative or Single ended I/O.
144	PL_D14_LVDS46_L8P_HDGC	IO_L8P_HDGC_AD4P_46	46	D14	IO, 1.8V	PL Bank46 IO8 differential positive. Same pin can be configured as HDGC Global Clock Input differential positive or PLSYSMON differential analog input4 positive or Single ended I/O.

**IO Type of IOs originating from ZU7/5/4 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU7/5/4 MPSoC datasheet.*

2.7.3 Power Control Input

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board to Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin in Board to Board Connector1. Also in Board to Board Connector1, Ground pins are distributed throughout the connector for better performance.

For more details on Power control & Ground pins on Board to Board Connector1, refer the below table.

Table 14: Power Control and Ground pinouts

B2B-1 Pin No.	B2B Connector1 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
232	SOMPWR_EN	NA	NA	NA	I, 5V	Active High SOM power enable. *Important Note:* *High– SOM power ON* *Low – SOM Power OFF*
1, 7, 13, 19, 25, 35, 41, 47, 53, 59, 61, 67, 73, 79, 85, 95, 101, 107, 113, 119, 121, 127, 133, 139, 145, 155, 161, 167, 173, 179, 181, 187, 193, 199, 205, 215, 221, 227, 233, 239, 2, 8, 20, 26, 36, 54, 60, 62, 68, 80, 86, 96, 102, 114, 120, 122, 140, 146, 156, 162, 174, 180, 182, 188, 200, 206, 216, 222, 234, 240	GND	NA	NA	NA	Power	Ground.

2.8 Board to Board Connector2

The Zynq Ultrascale+ MPSoC SOM Board to Board connector2 pinout is provided in the below table and the interfaces which are available at Board to Board Connector2 are explained in the following sections. The Board to Board Connector2 (J4) is physically located on bottom side of the SOM as shown below.

Number of Pins - 240

Connector Part Number - QTH-120-01-L-D-A

Mating Connector - QSH-120-01-L-D-A from Samtech

Staking Height - 5mm

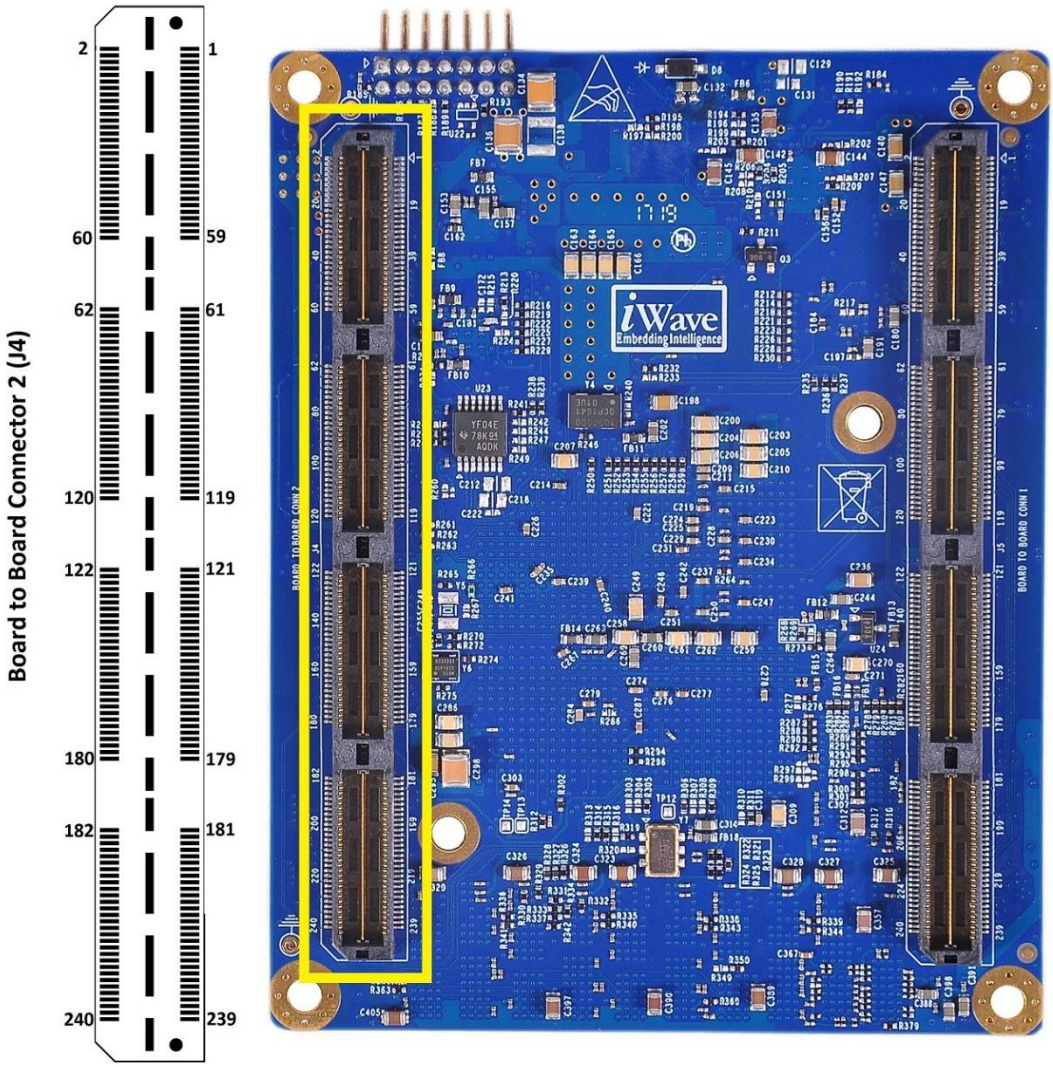


Figure 8: Board to Board Connector2

Table 15: Board to Board Connector2 Pinout

Signal	B2B-2 Pin	B2B-2 Pin	Signal
VCC_5V	1	2	VCC_5V
VCC_5V	3	4	VCC_5V
VCC_5V	5	6	VCC_5V
VCC_5V	7	8	VCC_5V
VCC_5V	9	10	VCC_5V
VCC_5V	11	12	VCC_5V
VCC_5V	13	14	VCC_5V
VCC_5V	15	16	VCC_5V
VCC_5V	17	18	VCC_5V
VCC_5V	19	20	VCC_5V
GND	21	22	GND
GND	23	24	GND
NC	25	26	USB_OTG_DM
PS_JTAG_TDI	27	28	USB_OTG_DP
PS_JTAG_TMS	29	30	GND
PS_JTAG_TCK	31	32	USB_PWR_EN
PS_JTAG_TDO	33	34	USB_OTG_ID
RESET_SW_IN	35	36	VBUS_USB
GND	37	38	I2C1_SDA(PS_MIO25_500)
GPHY_DTXRXM	39	40	SD1_WP(PS_MIO44_501)
GPHY_DTXRXP	41	42	SD1_CD(PS_MIO45_501)
GND	43	44	SD1_PWR(PS_MIO43_501)
GPHY_CTXRXM	45	46	I2C0_SDA(PS_MIO11_500)
GPHY_CTXRXP	47	48	I2C0_SCL(PS_MIO10_500)
GND	49	50	UART1_TX(PS_MIO08_500)
GPHY_BTXRXM	51	52	UART1_RX(PS_MIO09_500)
GPHY_BTXRXP	53	54	UART0_TX(PS_MIO07_500)
GND	55	56	UART0_RX(PS_MIO06_500)
GPHY_ATXRXM	57	58	GPHY_LINK_LED2
GPHY_ATXRXP	59	60	GPHY_ACTIVITY_LED1
Key			Key
SPI0_SCLK(PS_MIO0_500)	61	62	SD1_DATA3(PS_MIO49_501)
SPI0_SS0(PS_MIO3_500)	63	64	SD1_DATA2(PS_MIO48_501)
SPI0_MOSI(PS_MIO5_500)	65	66	SD1_DATA1(PS_MIO47_501)
SPI0_MISO(PS_MIO4_500)	67	68	VRTC_3V0
SD1_DATA0(PS_MIO46_501)	69	70	I2C1_SCL(PS_MIO24_500)
SD1_CMD(PS_MIO50_501)	71	72	SD1_CLK(PS_MIO51_501)
GND	73	74	GND
PL_AE1_LVDS66_L20N	75	76	PL_AA2_LVDS66_L24P
PL_AD1_LVDS66_L20P	77	78	PL_AA1_LVDS66_L24N
PL_AA5_LVDS66_L18N	79	80	PL_AC1_LVDS66_L23N

Signal	B2B-2 Pin	B2B-2 Pin	Signal
PL_AA6_LVDS66_L18P	81	82	PL_AB1_LVDS66_L23P
PL_AB9_LVDS66_L5N	83	84	PL_AB3_LVDS66_L22N_DBC
PL_AB10_LVDS66_L5P	85	86	PL_AA3_LVDS66_L22P_DBC
PL_W8_LVDS66_L9P	87	88	PL_AD2_LVDS66_L19P_DBC
PL_Y8_LVDS66_L9N	89	90	PL_AE2_LVDS66_L19N_DBC
PL_Y10_LVDS66_L6P	91	92	PL_Y7_LVDS66_L10P_QBC
PL_AA10_LVDS66_L6N	93	94	PL_AA7_LVDS66_L10N_QBC
PL_AA12_LVDS66_L2P	95	96	PL_AD6_LVDS66_L8N
PL_AA11_LVDS66_L2N	97	98	PL_AC6_LVDS66_L8P
PL_AB11_LVDS66_L3P	99	100	PL_AC9_LVDS66_L7P_QBC
PL_AC11_LVDS66_L3N	101	102	PL_AD9_LVDS66_L7N_QBC
PL_AC12_LVDS66_L1P_DBC	103	104	PL_AD11_LVDS66_L4P_DBC
PL_AD12_LVDS66_L1N_DBC	105	106	PL_AD10_LVDS66_L4N_DBC
GND	107	108	GND
PL_AB6_LVDS66_L14P_GC	109	110	PL_AA8_LVDS66_L12P_GC
PL_AB5_LVDS66_L14N_GC	111	112	PL_AB8_LVDS66_L12N_GC
GND	113	114	GND
PL_AD7_LVDS66_L13P_GC	115	116	PL_AC8_LVDS66_L11P_GC
PL_AE7_LVDS66_L13N_GC	117	118	PL_AC7_LVDS66_L11N_GC
GND	119	120	GND
Key			Key
PL_AC4_LVDS66_L17N	121	122	PL_AC16_LVDS64_L15P
PL_AB4_LVDS66_L17P	123	124	PL_AD16_LVDS64_L15N
PL_AE4_LVDS66_L16N_QBC	125	126	PL_AA14_LVDS64_L4P_DBC
PL_AD4_LVDS66_L16P_QBC	127	128	PL_AB14_LVDS64_L4N_DBC
GND	129	130	GND
PL_AC17_LVDS64_L17P	131	132	PL_AG18_LVDS64_L23P
PL_AC18_LVDS64_L17N	133	134	PL_AH18_LVDS64_L23N
PL_AD19_LVDS64_L18P	135	136	PL_AG16_LVDS64_L19P_DBC
PL_AE19_LVDS64_L18N	137	138	PL_AH16_LVDS64_L19N_DBC
PL_AD5_LVDS66_L15P	139	140	PL_AE14_LVDS64_L2P
PL_AE5_LVDS66_L15N	141	142	PL_AE13_LVDS64_L2N
PL_AC2_LVDS66_L21N	143	144	PL_AC14_LVDS64_L3P
PL_AC3_LVDS66_L21P	145	146	PL_AD14_LVDS64_L3N
PL_AE18_LVDS64_L24P	147	148	PL_AD15_LVDS64_L6P
PL_AF18_LVDS64_L24N	149	150	PL_AE15_LVDS64_L6N
PL_AH17_LVDS64_L21P	151	152	PL_AK13_LVDS64_L8P
PL_AJ17_LVDS64_L21N	153	154	PL_AK12_LVDS64_L8N
PL_AJ16_LVDS64_L20P	155	156	PL_AJ14_LVDS64_L9P
PL_AK16_LVDS64_L20N	157	158	PL_AK14_LVDS64_L9N
PL_AK17_LVDS64_L22P_DBC	159	160	PL_AB15_LVDS64_L5N
PL_AK18_LVDS64_L22N_DBC	161	162	PL_AA15_LVDS64_L5P

Signal	B2B-2 Pin	B2B-2 Pin	Signal
PL_AA13_LVDS64_L1P_DBC	163	164	PL_AJ15_LVDS64_L10P_QBC
PL_AB13_LVDS64_L1N_DBC	165	166	PL_AK15_LVDS64_L10N_QBC
GND	167	168	GND
PL_AD17_LVDS64_L14P_GC	169	170	PL_AF16_LVDS64_L13P_GC
PL_AE17_LVDS64_L14N_GC	171	172	PL_AF17_LVDS64_L13N_GC
GND	173	174	GND
PL_AF15_LVDS64_L12P_GC	175	176	PL_AG14_LVDS64_L11P_GC
PL_AG15_LVDS64_L12N_GC	177	178	PL_AH14_LVDS64_L11N_GC
GND	179	180	GND
Key			Key
PL_AH13_LVDS64_L7N_QBC	181	182	PL_AA16_LVDS64_L16P_QBC
PL_AG13_LVDS64_L7P_QBC	183	184	PL_AB16_LVDS64_L16N_QBC
GND	185	186	GND
GTHRXP0_226	187	188	GTREFCLK0P_226
GTHRXN0_226	189	190	GTREFCLK0N_226
GND	191	192	GND
GTHTXP0_226	193	194	GTHRXP3_226
GTHTXN0_226	195	196	GTHRXN3_226
GND	197	198	GND
GTHRXP1_226	199	200	GTHTXP3_226
GTHRXN1_226	201	202	GTHTXN3_226
GND	203	204	GND
GTHTXP1_226	205	206	PS_MGTRRXP3_505
GTHTXN1_226	207	208	PS_MGTRRXN3_505
GND	209	210	GND
GTHRXP2_226	211	212	PS_MGTRTXP3_505
GTHRXN2_226	213	214	PS_MGTRTXN3_505
GND	215	216	GND
GTHTXP2_226	217	218	PS_MGTREFCLK3P_505
GTHTXN2_226	219	220	PS_MGTREFCLK3N_505
GND	221	222	GND
GTREFCLK1P_226	223	224	NC
GTREFCLK1N_226	225	226	NC
GND	227	228	GND
PS_MGTRRXP2_505	229	230	PS_MGTREFCLK2P_505
PS_MGTRRXN2_505	231	232	PS_MGTREFCLK2N_505
GND	233	234	GND
PS_MGTRTXP2_505	235	236	NC
PS_MGTRTXN2_505	237	238	NC
GND	239	240	GND

Important Note: The signal name (with ball name) in pinout is mentioned based on the ZU4/5 device.

2.8.1 PS Interfaces

The interfaces which are supported in Board to Board Conenector2 from Zynq Ultrascale+ MPSoC's PS is explained in the following section.

2.8.1.1 PS-GTR High Speed Transceivers

The Zynq Ultrascale+ MPSoC SOM supports two PS GTR transceivers (Lane2 & Lane3) on Board to Board Connector2. For more details on PS-GTR transceivers, refer section ***2.7.1.1***.

For more details on PS-GTR transceiver pinouts on Board to Board Connector2, refer the below table.

Table 16: PS-GTR pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
PS-GTR Lane2 Pins						
235	PS_MGTRTXP2_505	PS_MGTRTXP2_505	505	J25	O, DIFF	PS-GTR Lane2 High speed differential transmitter positive.
237	PS_MGTRTXN2_505	PS_MGTRTXN2_505	505	J26	O, DIFF	PS-GTR Lane2 High speed differential transmitter negative.
229	PS_MGTRRXP2_505	PS_MGTRRXP2_505	505	H27	I, DIFF	PS-GTR Lane2 High speed differential receiver positive.
231	PS_MGTRRXN2_505	PS_MGTRRXN2_505	505	H28	I, DIFF	PS-GTR Lane2 High speed differential receiver negative.
230	PS_MGTREFCLK2P_505	PS_MGTREFCLK2P_505	505	K23	I, DIFF	PS-GTR Lane2 differential reference clock positive.
232	PS_MGTREFCLK2N_505	PS_MGTREFCLK2N_505	505	K24	I, DIFF	PS-GTR Lane2 differential reference clock negative.
PS-GTR Lane3 Pins						
212	PS_MGTRTXP3_505	PS_MGTRTXP3_505	505	G25	O, DIFF	PS-GTR Lane3 High speed differential transmitter positive.
214	PS_MGTRTXN3_505	PS_MGTRTXN3_505	505	G26	O, DIFF	PS-GTR Lane3 High speed differential transmitter negative.
206	PS_MGTRRXP3_505	PS_MGTRRXP3_505	505	G29	I, DIFF	PS-GTR Lane3 High speed differential receiver positive.
208	PS_MGTRRXN3_505	PS_MGTRRXN3_505	505	G30	I, DIFF	PS-GTR Lane3 High speed differential receiver negative.
218	PS_MGTREFCLK3P_505	PS_MGTREFCLK3P_505	505	H23	I, DIFF	PS-GTR Lane3 differential reference clock positive.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
220	PS_MGTREFCLK 3N_505	PS_MGTREFCL K3N_505	505	H24	I, DIFF	PS-GTR Lane3 differential reference clock negative.

Note: if PS-GTR lane3 is selected as USB 3.0 then USB1 2.0 only can be used.

2.8.1.2 Gigabit Ethernet Interface

The Zynq Ultrascale+ MPSoC SOM supports one 10/100/1000 Mbps Ethernet interface on Board to Board Connector2.The MAC is integrated in the Zynq Ultrascale+ MPSoC PS and connected to the external Gigabit Ethernet PHY "AR8031" on SOM. This Gigabit Ethernet PHY is interfaced with GEM0 interface of MPSoC's PS through MIO pins and works at 1.8V IO voltage level.

In Zynq Ultrascale+ MPSoC SOM, PS GPIO "PS_MIO42_501" is used for Ethernet PHY reset and also shared with USB ULPI PHY reset. Also SOM supports Ethernet PHY interrupt through PS GPIO "PS_MIO12_500". This PHY supports active high Link and Activity LED indication signals and available on Board to Board Connector2. Since MAC and PHY are supported on SOM itself, only Magnetics is required on the carrier board.

Important Note: GPHY_ACTIVITY_LED1 signal is muxed with PHYADDRESS2 pin. The same GPHY_ACTIVITY_LED1 signal is connected to 60th pin of Board to Board connector2 to support Gigabit Ethernet Activity LED.

For more details on Gigabit Ethernet Interface pinouts on Board to Board Connector2, refer the below table.

Table 17: Gigabit Ethernet pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
39	GPHY_DTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 negative.
41	GPHY_DTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 4 positive.
45	GPHY_CTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 negative.
47	GPHY_CTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 3 positive.
51	GPHY_BTXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 negative.
53	GPHY_BTXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 2 positive.
57	GPHY_ATXRXM	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 negative.
59	GPHY_ATXRXP	NA	NA	NA	IO, GBE	Gigabit Ethernet differential pair 1 positive.
58	GPHY_LINK_LED2	NA	NA	NA	O, 2.5V CMOS	Gigabit Ethernet link status LED.
60	GPHY_ACTIVITY_LED1	NA	NA	NA	O, 2.5V CMOS	Gigabit Ethernet speed status LED

2.8.1.3 USB2.0 OTG Interface

The Zynq Ultrascale+ MPSoC SOM supports one USB2.0 OTG interface on Board to Board Connector2. USB0 OTG controller of Zynq Ultrascale+ MPSoC PS is used for USB2.0 OTG interface. The USB OTG controller is capable of fulfilling a wide range of applications for USB2.0 implementations as a host, a device or On-the-Go. Also this controller supports all high-speed, full-speed and low-speed transfers in both device and host modes. While using USB3.0 interface through PS-GTR, this USB2.0 OTG interface will co-work with USB3.0 interface.

The USB OTG controller uses the ULPI protocol to connect external ULPI PHY via the MIO pins. The Zynq Ultrascale+ MPSoC SOM supports "USB3320" ULPI transceiver from Microchip and works at 1.8V IO voltage level. In Zynq Ultrascale+ MPSoC SOM, PS GPIO "PS_MIO42_501" is used for USB ULPI PHY reset and also shared with Gigabit Ethernet PHY reset. It supports active high power enable signal on Board to Board Connector2 from USB PHY for external VBUS power control.

Also Zynq Ultrascale+ MPSoC SOM supports USB ID & USB VBUS inputs from Board to Board Connector2 and connected to USB PHY for USB Host/Device detection & VBUS monitoring respectively. If USB ID pin is grounded, then USB Host is detected and if it is floated, USB device is detected.

For more details on USB2.0 OTG Interface pinouts on Board to Board Connector2, refer the below table.

Table 18: USB2.0 OTG pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
26	USB_OTG_DM	NA	NA	NA	IO, USB	USB OTG data negative.
28	USB_OTG_DP	NA	NA	NA	IO, USB	USB OTG data positive.
32	USB_PWR_EN	NA	NA	NA	O, 3.3V CMOS	USB active high power enable output to control external USB VBUS.
34	USB_OTG_ID	NA	NA	NA	I, 3.3V CMOS	USB OTG ID input for USB host or device detection.
36	VBUS_USB	NA	NA	NA	I, 5V Power	USB VBUS for VBUS monitoring.

2.8.1.4 SD/SDIO Interface

The Zynq Ultrascale+ MPSoC SOM supports SD/SDIO interface on Board to Board Connector2. The SD1 controller of MPSoC's PS is used for SD/SDIO interface through MIO pins. This SD/SDIO controller is compatible with the standard SD Host Controller Specification Version 3.0. It supports different speed mode like Standard mode (19Mhz), High Speed mode (50Mhz), SDR12 (25Mhz), SDR25 (25Mhz), SDR50 (100Mhz), SDR104 (200Mhz) & DDR50 mode (50Mhz). Also in SD mode, data transfers in 1-bit and 4-bit modes.

The Zynq Ultrascale+ MPSoC SOM supports Card Detect, Write Protect & Power Enable/Voltage Select pins through MIO pins.

For more details on SD/SDIO Interface pinouts on Board to Board Connector2, refer the below table.

Table 19: SD/SDIO pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
40	SD1_WP(PS_MIO 44_501)	PS_MIO44_501	501	E24	I, 1.8V LVCMOS/4.7K PU	SD1 Write Protect.
42	SD1_CD(PS_MIO4 5_501)	PS_MIO45_501	501	F23	I, 1.8V LVCMOS/4.7K PU	SD1 Card Detect.
44	SD1_PWR(PS_MI O43_501)	PS_MIO43_501	501	F22	O, 1.8V LVCMOS	SD1 Power Enable/Voltage select through PS GPIO.
62	SD1_DATA3(PS_ MIO49_501)	PS_MIO49_501	501	G21	IO, 1.8V LVCMOS/10K PU	SD1 Data3.
64	SD1_DATA2(PS_ MIO48_501)	PS_MIO48_501	501	J21	IO, 1.8V LVCMOS/10K PU	SD1 Data2.
66	SD1_DATA1(PS_ MIO47_501)	PS_MIO47_501	501	K21	IO, 1.8V LVCMOS/10K PU	SD1 Data1.
69	SD1_DATA0(PS_ MIO46_501)	PS_MIO46_501	501	K20	IO, 1.8V LVCMOS/10K PU	SD1 Data0.
71	SD1_CMD(PS_MI O50_501)	PS_MIO50_501	501	J20	IO, 1.8V LVCMOS/10K PU	SD1 Command.
72	SD1_CLK(PS_MIO 51_501)	PS_MIO51_501	501	H21	O, 1.8V LVCMOS/10KPU	SD1 Clock.

2.8.1.5 SPI Interface

The Zynq Ultrascale+ MPSoC SOM supports one SPI interface with one chip select on Board to Board Connector2 and second chip select on Board to Board conenctor1. The SPI0 controller of MPSoC's PS is used for SPI interface through MIO pins. It can function in master mode, slave mode or multi-master mode and supports full-duplex operation.

For more details on SPI Interface pinouts on Board to Board Connector2, refer the below table.

Table 20: SPI pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
61	SPI0_SCLK(PS_MIO0_500)	PS_MIO0_500	500	H17	O, 1.8V LVCMOS	SPI Clock output.
63	SPI0_SS0(PS_MIO3_500)	PS_MIO3_500	500	D19	O, 1.8V LVCMOS	SPI Chip select 0.
65	SPI0_MOSI(PS_MIO5_500)	PS_MIO5_500	500	C19	IO, 1.8V LVCMOS	SPI Master output Slave input.
67	SPI0_MISO(PS_MIO4_500)	PS_MIO4_500	500	J17	IO, 1.8V LVCMOS	SPI Master input Slave output.
178	SPI0_SS2(PS_MIO1_500)	PS_MIO1_500	500	A20	I/O, 1.8V LVCMOS	SPI chip select2. Same pin can be configured as GPIO.

2.8.1.6 Debug UART Interface

The Zynq Ultrascale+ MPSoC SOM supports one Debug UART interface on Board to Board Connector2. The UART0 controller of MPSoC's PS is used for Debug UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter.

For more details on Debug UART pinouts on Board to Board Connector2, refer the below table.

Table 21: Debug UART pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
54	UART0_TX(PS_MIO07_500)	PS_MIO07_500	500	E19	O, 1.8V LVCMOS	Debug UART0 Transmit data line for Debug.
56	UART0_RX(PS_MIO06_500)	PS_MIO06_500	500	D20	I, 1.8V LVCMOS	Debug UART0 Receive data line for Debug.

2.8.1.7 Data UART Interface

The Zynq Ultrascale+ MPSoC SOM supports one DATA UART interface on Board to Board Connector2. The UART1 controller of MPSoC's PS is used for Data UART interface through MIO pins. This controller supports full-duplex asynchronous receiver and transmitter path with programmable baud rates. Each path includes a 64- Byte FIFIO.

For more details on Data UART pinouts on Board to Board Connector2, refer the below table.

Table 22: Data UART pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
50	UART1_TX(PS_MIO08_500)	PS_MIO08_500	500	E20	O, 1.8V LVCMOS	UART1 Transmit data line.
52	UART1_RX(PS_MIO09_500)	PS_MIO09_500	500	F20	I, 1.8V LVCMOS	UART1 Receive data line.

2.8.1.8 I2C Interface

The Zynq Ultrascale+ MPSoC SOM supports one I2C interface on Board to Board Connector2. The I2C0 module of MPSoC's PS is used for I2C interface through MIO pins and compatible with the standard NXP I2C bus protocol. It supports standard mode with data transfer rates up to 100kbps and Fast mode with data transfer rates up to 400kbps. It can function as a master or a slave in a multi-master design. The master can be programmed to use both normal (7-bit) addressing and extended (10-bit) addressing modes. Since flexible I2C standard allows multiple devices to be connected to the single bus, I2C0 interface is also connected to On-SOM PMIC with I2C address 0x58 in the Zynq Ultrascale+ MPSoC SOM. Also one more I2C interface (I2C1) can be taken out on Board to Board Connector2 which is multiplexed with PS GPIOs.

For more details on I2C Interface pinouts on Board to Board Connector2, refer the below table.

Table 23: I2C Interface pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
46	I2C0_SDA(PS_MIO11_500)	PS_MIO11_500	500	G18	IO, 1.8V OD/ 4.7K PU	I2C0 data.
48	I2C0_SCL(PS_MIO10_500)	PS_MIO10_500	500	F18	O, 1.8V OD/ 4.7K PU	I2C0 clock.
38	I2C1_SDA(PS_MIO25_500)	PS_MIO25_500	500	B18	IO, 1.8V	General Purpose I/O. Can be configured as I2C1_SDA.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
70	I2C1_SCL(PS_MIO24_500)	PS_MIO24_500	500	A18	IO, 1.8V	General Purpose I/O. Can be configured as I2C1_SCL.

2.8.1.9 JTAG Interface

The Zynq Ultrascale+ MPSoC SOM supports JTAG interface on Board to Board Connector2. The Zynq Ultrascale+ MPSoC's PS and PL share a common set of JTAG pins and each have their own TAP controller which are chained together inside the Zynq Ultrascale MPSoC. These JTAG interface signals are also connected to on-board JTAG connector.

For more details on JTAG Interface pinouts on Board to Board Connector2, refer the below table.

Table 24: JTAG pinout description

B2B-2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
27	PS_JTAG_TDI	PS_JTAG_TDI	503	L20	I, 1.8V LVCMOS/4.7K	JTAG Test Data Input.
29	PS_JTAG_TMS	PS_JTAG_TMS	503	L21	I, 1.8V LVCMOS/4.7K	JTAG Test Mode Select.
31	PS_JTAG_TCK	PS_JTAG_TCK	503	L19	I, 1.8V LVCMOS/4.7K	JTAG Test Clock.
33	PS_JTAG_TDO	PS_JTAG_TDO	503	M20	O, 1.8V LVCMOS	JTAG Test Data Output.

2.8.2 PL Interfaces

The interfaces which are supported in Board to Board Connector2 from Zynq Ultrascale+ MPSoC's PL is explained in the following section.

2.8.2.1 GTH High Speed Transceivers

The Zynq Ultrascale+ MPSoC SOM Supports 4 GTH transceivers along with reference clock inputs (Bank226) on Board to Board Connector2. For more details on GTH transceivers, refer section ***2.7.2.1***.

Note: In ZU7CG/7EG/7EV MPSoC devices, the transceiver Quad Bank223, 224, 225 & 226 is called as Bank224, 225 226 & 227 respectively. Only the Bank Numbering is different and all other functionalities remain same.

For more details on GTH transceiver pinouts on Board to Board Connector2, refer the below table.

Table 25: GTH Transceiver pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
Bank226 Transceiver Quad Pins						
187	GTHRXP0_226	MGTHRXP0_226	226	D2	I, DIFF	GTH Bank226 channel0 High speed differential receiver positive.
189	GTHRXN0_226	MGTHRXN0_226	226	D1	I, DIFF	GTH Bank226 channel0 High speed differential receiver negative.
193	GTHTXP0_226	MGTHTXP0_226	226	D6	O, DIFF	GTH Bank226 channel0 High speed differential transmitter positive.
195	GTHTXN0_226	MGTHTXN0_226	226	D5	O, DIFF	GTH Bank226 channel0 High speed differential transmitter negative.
199	GTHRXP1_226	MGTHRXP1_226	226	C4	I, DIFF	GTH Bank226 channel1 High speed differential receiver positive.
201	GTHRXN1_226	MGTHRXN1_226	226	C3	I, DIFF	GTH Bank226 channel1 High speed differential receiver negative.
205	GTHTXP1_226	MGTHTXP1_226	226	C8	O, DIFF	GTH Bank226 channel1 High speed differential transmitter positive.
207	GTHTXN1_226	MGTHTXN1_226	226	C7	O, DIFF	GTH Bank226 channel1 High speed differential transmitter negative.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
211	GTHRXP2_226	MGTHRXP2_226	226	B2	I, DIFF	GTH Bank226 channel2 High speed differential receiver positive.
213	GTHRXN2_226	MGTHRXN2_226	226	B1	I, DIFF	GTH Bank226 channel2 High speed differential receiver negative.
217	GTHTXP2_226	MGTHTXP2_226	226	B6	O, DIFF	GTH Bank226 channel2 High speed differential transmitter positive.
219	GTHTXN2_226	MGTHTXN2_226	226	B5	O, DIFF	GTH Bank226 channel2 High speed differential transmitter negative.
194	GTHRXP3_226	MGTHRXP3_226	226	A4	I, DIFF	GTH Bank226 channel3 High speed differential receiver positive.
196	GTHRXN3_226	MGTHRXN3_226	226	A3	I, DIFF	GTH Bank226 channel3 High speed differential receiver negative.
200	GTHTXP3_226	MGTHTXP3_226	226	A8	O, DIFF	GTH Bank226 channel3 High speed differential transmitter positive.
202	GTHTXN3_226	MGTHTXN3_226	226	A7	O, DIFF	GTH Bank226 channel3 High speed differential transmitter negative.
188	GTREFCLK0P_226	MGTREFCLK0P_226	226	D10	I, DIFF	GTH Bank226 differential reference clock0 positive.
190	GTREFCLK0N_226	MGTREFCLK0N_226	226	D9	I, DIFF	GTH Bank226 differential reference clock0 negative.
223	GTREFCLK1P_226	MGTREFCLK1P_226	226	B10	I, DIFF	GTH Bank226 differential reference clock1 positive.
225	GTREFCLK1N_226	MGTREFCLK1N_226	226	B9	I, DIFF	GTH Bank226 differential reference clock1 negative.

2.8.2.2 PL IOs – HP BANK64

The Zynq Ultrascale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board to Board Connector2 from MPSoC's PL High Performance (HP) Bank64. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available. I/O voltage of this PL HP Bank64 is fixed to 1.8V.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank64 signals are routed as LVDS IOs to Board to Board Connector2. Even though PL Bank64 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board

Connector2 pins 169, 170, 171, 172, 175, 176, 177 & 178 are GC Global Clock Input capable pins of PL Bank64. Also Board to Board Connector2 pins 122, 124, 126, 128, 131, 133, 135, 136, 137, 138, 144, 146, 148, 150, 151, 152,153, 154, 155, 156,157, 158,159, 160, 161, 162, 164, 166, 181, 182, 183, 184 are PLSYSMON auxiliary analog Input capable pins of PL Bank64.

For more details on PL HP Bank64 pinouts on Board to Board Connector2, refer the below table.

Table 26: PL HP Bank64 pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
131	PL_AC17_LVDS64_L17P	IO_L17P_T2U_N8_AD10P_64	64	AC17	IO, 1.8V	PL Bank64 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
133	PL_AC18_LVDS64_L17N	IO_L17N_T2U_N9_AD10N_64	64	AC18	IO, 1.8V	PL Bank64 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
135	PL_AD19_LVDS64_L18P	IO_L18P_T2U_N10_AD2P_64	64	AD19	IO, 1.8V	PL Bank64 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
137	PL_AE19_LVDS64_L18N	IO_L18N_T2U_N11_AD2N_64	64	AE19	IO, 1.8V	PL Bank64 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
147	PL_AE18_LVDS64_L24P	IO_L24P_T3U_N10_64	64	AE18	IO, 1.8V	PL Bank64 IO24 differential positive. Same pin can be configured as Single ended I/O.
149	PL_AF18_LVDS64_L24N	IO_L24N_T3U_N11_64	64	AF18	IO, 1.8V	PL Bank64 IO24 differential negative. Same pin can be configured as Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
151	PL_AH17_LVDS64_L21P	IO_L21P_T3L_N4_AD8P_64	64	AH17	IO, 1.8V	PL Bank64 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.
153	PL_AJ17_LVDS64_L21N	IO_L21N_T3L_N5_AD8N_64	64	AJ17	IO, 1.8V	PL Bank64 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
155	PL_AJ16_LVDS64_L20P	IO_L20P_T3L_N2_AD1P_64	64	AJ16	IO, 1.8V	PL Bank64 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
157	PL_AK16_LVDS64_L20N	IO_L20N_T3L_N3_AD1N_64	64	AK16	IO, 1.8V	PL Bank64 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
159	PL_AK17_LVDS64_L22P_DBC	IO_L22P_T3U_N6_DBC_AD0P_64	64	AK17	IO, 1.8V	PL Bank64 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
161	PL_AK18_LVDS64_L22N_DBC	IO_L22N_T3U_N7_DBC_AD0N_64	64	AK18	IO, 1.8V	PL Bank64 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
163	PL_AA13_LVDS64_L1P_DBC	IO_L1P_T0L_N0_DBC_64	64	AA13	IO, 1.8V	PL Bank64 IO1 differential positive. Same pin can be configured as Single ended I/O.
165	PL_AB13_LVDS64_L1N_DBC	IO_L1N_T0L_N1_DBC_64	64	AB13	IO, 1.8V	PL Bank64 IO1 differential negative. Same pin can be configured as Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
169	PL_AD17_LVDS64_L14P_GC	IO_L14P_T2L_N2_GC_64	64	AD17	IO, 1.8V	PL Bank64 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
171	PL_AE17_LVDS64_L14N_GC	IO_L14N_T2L_N3_GC_64	64	AE17	IO, 1.8V	PL Bank64 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
175	PL_AF15_LVDS64_L12P_GC	IO_L12P_T1U_N10_GC_64	64	AF15	IO, 1.8V	PL Bank64 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
177	PL_AG15_LVDS64_L12N_GC	IO_L12N_T1U_N11_GC_64	64	AG15	IO, 1.8V	PL Bank64 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
181	PL_AH13_LVDS64_L7N_QBC	IO_L7N_T1L_N1_QBC_AD13N_64	64	AH13	IO, 1.8V	PL Bank64 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
183	PL_AG13_LVDS64_L7P_QBC	IO_L7P_T1L_N0_QBC_AD13P_64	64	AG13	IO, 1.8V	PL Bank64 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
122	PL_AC16_LVDS64_L15P	IO_L15P_T2L_N4_AD11P_64	64	AC16	IO, 1.8V	PL Bank64 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
124	PL_AD16_LVDS64_L15N	IO_L15N_T2L_N5_AD11N_64	64	AD16	IO, 1.8V	PL Bank64 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
126	PL_AA14_LVDS64_L4P_DBC	IO_L4P_T0U_N6_DBC_AD7P_64	64	AA14	IO, 1.8V	PL Bank64 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
128	PL_AB14_LVDS64_L4N_DBC	IO_L4N_T0U_N7_DBC_AD7N_64	64	AB14	IO, 1.8V	PL Bank64 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
132	PL_AG18_LVDS64_L23P	IO_L23P_T3U_N8_64	64	AG18	IO, 1.8V	PL Bank64 IO23 differential positive. Same pin can be configured as Single ended I/O.
134	PL_AH18_LVDS64_L23N	IO_L23N_T3U_N9_64	64	AH18	IO, 1.8V	PL Bank64 IO23 differential negative. Same pin can be configured as Single ended I/O.
136	PL_AG16_LVDS64_L19P_DBC	IO_L19P_T3L_N0_DBC_AD9P_64	64	AG16	IO, 1.8V	PL Bank64 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
138	PL_AH16_LVDS64_L19N_DBC	IO_L19N_T3L_N1_DBC_AD9N_64	64	AH16	IO, 1.8V	PL Bank64 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
140	PL_AE14_LVDS64_L2P	IO_L2P_T0L_N2_64	64	AE14	IO, 1.8V	PL Bank64 IO2 differential positive. Same pin can be configured as Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
142	PL_AE13_LVDS64_L2N	IO_L2N_T0L_N3_64	64	AE13	IO, 1.8V	PL Bank64 IO2 differential negative. Same pin can be configured as Single ended I/O.
144	PL_AC14_LVDS64_L3P	IO_L3P_T0L_N4_AD15P_64	64	AC14	IO, 1.8V	PL Bank64 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
146	PL_AD14_LVDS64_L3N	IO_L3N_T0L_N5_AD15N_64	64	AD14	IO, 1.8V	PL Bank64 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
148	PL_AD15_LVDS64_L6P	IO_L6P_T0U_N10_AD6P_64	64	AD15	IO, 1.8V	PL Bank64 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
150	PL_AE15_LVDS64_L6N	IO_L6N_T0U_N11_AD6N_64	64	AE15	IO, 1.8V	PL Bank64 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
152	PL_AK13_LVDS64_L8P	IO_L8P_T1L_N2_AD5P_64	64	AK13	IO, 1.8V	PL Bank64 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
154	PL_AK12_LVDS64_L8N	IO_L8N_T1L_N3_AD5N_64	64	AK12	IO, 1.8V	PL Bank64 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
156	PL_AJ14_LVDS64_L9P	IO_L9P_T1L_N4_AD12P_64	64	AJ14	IO, 1.8V	PL Bank64 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
158	PL_AK14_LVDS64_L9N	IO_L9N_T1L_N5_AD12N_64	64	AK14	IO, 1.8V	PL Bank64 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.
160	PL_AB15_LVDS64_L5N	IO_L5N_T0U_N9_AD14N_64	64	AB15	IO, 1.8V	PL Bank64 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
162	PL_AA15_LVDS64_L5P	IO_L5P_T0U_N8_AD14P_64	64	AA15	IO, 1.8V	PL Bank64 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O
164	PL_AJ15_LVDS64_L10P_QBC	IO_L10P_T1U_N6_QBC_AD4P_64	64	AJ15	IO, 1.8V	PL Bank64 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.
166	PL_AK15_LVDS64_L10N_QBC	IO_L10N_T1U_N7_QBC_AD4N_64	64	AK15	IO, 1.8V	PL Bank64 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
170	PL_AF16_LVDS64_L13P_GC	IO_L13P_T2L_N0_GC_QBC_64	64	AF16	IO, 1.8V	PL Bank64 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
172	PL_AF17_LVDS64_L13N_GC	IO_L13N_T2L_N1_GC_QBC_64	64	AF17	IO, 1.8V	PL Bank64 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
176	PL_AG14_LVDS64_L11P_GC	IO_L11P_T1U_N8_GC_64	64	AG14	IO, 1.8V	PL Bank64 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
178	PL_AH14_LVDS64_L11N_GC	IO_L11N_T1U_N9_GC_64	64	AH14	IO, 1.8V	PL Bank64 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
182	PL_AA16_LVDS64_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_64	64	AA16	IO, 1.8V	PL Bank64 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
184	PL_AB16_LVDS64_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_64	64	AB16	IO, 1.8V	PL Bank64 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.

**IO Type of IOs originating from ZU7/5/4 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU7/5/4 MPSoC datasheet.*

2.8.2.3 PL IOs –HP BANK66

The Zynq Ultrascale+ MPSoC SOM supports 24 LVDS IOs/48 Single Ended (SE) IOs on Board to Board Connector2 from MPSoC's PL High Performance (HP) Bank66. Upon these 24 LVDS IOs/48 SE IOs, upto 4 GC Global Clock Inputs and upto 16 PLSYSMON auxiliary analog inputs are available. I/O voltage of this PL HP Bank66 is fixed to 1.8V.

In the Zynq Ultrascale+ MPSoC SOM, PL Bank66 signals are routed as LVDS IOs to Board to Board Connector2. Even though PL Bank66 signals are routed as LVDS IOs, these pins can be used as SE IOs if required. The Board to Board Connector2 pins 109, 111, 110, 112, 115, 117, 116 & 118 are GC Global Clock Input capable pins of PL Bank66. Also Board to Board Connector2 pins 75, 77, 79, 81, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 98, 99, 100, 101, 102, 104, 106, 121, 123, 125, 127, 139, 141, 143 & 145 are PLSYSMON auxiliary analog Input capable pins of PL Bank66.

For more details on PL HP Bank66 pinouts on Board to Board Connector2, refer the below table.

Table 27: PL HP Bank66 pinout description

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
75	PL_AE1_LVDS66_L20N	IO_L20N_T3L_N3_AD1N_66	66	AE1	IO, 1.8V	PL Bank66 IO20 differential negative. Same pin can be configured as PLSYSMON differential analog input1 negative or Single ended I/O.
77	PL_AD1_LVDS66_L20P	IO_L20P_T3L_N2_AD1P_66	66	AD1	IO, 1.8V	PL Bank66 IO20 differential positive. Same pin can be configured as PLSYSMON differential analog input1 positive or Single ended I/O.
79	PL_AA5_LVDS66_L18N	IO_L18N_T2U_N11_AD2N_66	66	AA5	IO, 1.8V	PL Bank66 IO18 differential negative. Same pin can be configured as PLSYSMON differential analog input2 negative or Single ended I/O.
81	PL_AA6_LVDS66_L18P	IO_L18P_T2U_N10_AD2P_66	66	AA6	IO, 1.8V	PL Bank66 IO18 differential positive. Same pin can be configured as PLSYSMON differential analog input2 positive or Single ended I/O.
83	PL_AB9_LVDS66_L5N	IO_L5N_T0U_N9_AD14N_66	66	AB9	IO, 1.8V	PL Bank66 IO5 differential negative. Same pin can be configured as PLSYSMON differential analog input14 negative or Single ended I/O.
85	PL_AB10_LVDS66_L5P	IO_L5P_T0U_N8_AD14P_66	66	AB10	IO, 1.8V	PL Bank66 IO5 differential positive. Same pin can be configured as PLSYSMON differential analog input14 positive or Single ended I/O.
87	PL_W8_LVDS66_L9P	IO_L9P_T1L_N4_AD12P_66	66	W8	IO, 1.8V	PL Bank66 IO9 differential positive. Same pin can be configured as PLSYSMON differential analog input12 positive or Single ended I/O.
89	PL_Y8_LVDS66_L9N	IO_L9N_T1L_N5_AD12N_66	66	Y8	IO, 1.8V	PL Bank66 IO9 differential negative. Same pin can be configured as PLSYSMON differential analog input12 negative or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
91	PL_Y10_LVDS66_L6P	IO_L6P_T0U_N10_AD6P_66	66	Y10	IO, 1.8V	PL Bank66 IO6 differential positive. Same pin can be configured as PLSYSMON differential analog input6 positive or Single ended I/O.
93	PL_AA10_LVDS66_L6N	IO_L6N_T0U_N11_AD6N_66	66	AA10	IO, 1.8V	PL Bank66 IO6 differential negative. Same pin can be configured as PLSYSMON differential analog input6 negative or Single ended I/O.
95	PL_AA12_LVDS66_L2P	IO_L2P_T0L_N2_66	66	AA12	IO, 1.8V	PL Bank66 IO2 differential positive. Same pin can be configured as Single ended I/O.
97	PL_AA11_LVDS66_L2N	IO_L2N_T0L_N3_66	66	AA11	IO, 1.8V	PL Bank66 IO2 differential negative. Same pin can be configured as Single ended I/O.
99	PL_AB11_LVDS66_L3P	IO_L3P_T0L_N4_AD15P_66	66	AB11	IO, 1.8V	PL Bank66 IO3 differential positive. Same pin can be configured as PLSYSMON differential analog input15 positive or Single ended I/O.
101	PL_AC11_LVDS66_L3N	IO_L3N_T0L_N5_AD15N_66	66	AC11	IO, 1.8V	PL Bank66 IO3 differential negative. Same pin can be configured as PLSYSMON differential analog input15 negative or Single ended I/O.
103	PL_AC12_LVDS66_L1P_DBC	IO_L1P_T0L_N0_DBC_66	66	AC12	IO, 1.8V	PL Bank66 IO1 differential positive. Same pin can be configured as Single ended I/O.
105	PL_AD12_LVDS66_L1N_DBC	IO_L1N_T0L_N1_DBC_66	66	AD12	IO, 1.8V	PL Bank66 IO1 differential negative. Same pin can be configured as Single ended I/O.
109	PL_AB6_LVDS66_L14P_GC	IO_L14P_T2L_N2_GC_66	66	AB6	IO, 1.8V	PL Bank66 IO14 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
111	PL_AB5_LVDS66_L14N_GC	IO_L14N_T2L_N3_GC_66	66	AB5	IO, 1.8V	PL Bank66 IO14 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
115	PL_AD7_LVDS66_L13P_GC	IO_L13P_T2L_N0_GC_QBC_66	66	AD7	IO, 1.8V	PL Bank66 IO13 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
117	PL_AE7_LVDS66_L13N_GC	IO_L13N_T2L_N1_GC_QBC_66	66	AE7	IO, 1.8V	PL Bank66 IO13 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
121	PL_AC4_LVDS66_L17N	IO_L17N_T2U_N9_AD10N_66	66	AC4	IO, 1.8V	PL Bank66 IO17 differential negative. Same pin can be configured as PLSYSMON differential analog input10 negative or Single ended I/O.
123	PL_AB4_LVDS66_L17P	IO_L17P_T2U_N8_AD10P_66	66	AB4	IO, 1.8V	PL Bank66 IO17 differential positive. Same pin can be configured as PLSYSMON differential analog input10 positive or Single ended I/O.
125	PL_AE4_LVDS66_L16N_QBC	IO_L16N_T2U_N7_QBC_AD3N_66	66	AE4	IO, 1.8V	PL Bank66 IO16 differential negative. Same pin can be configured as PLSYSMON differential analog input3 negative or Single ended I/O.
127	PL_AD4_LVDS66_L16P_QBC	IO_L16P_T2U_N6_QBC_AD3P_66	66	AD4	IO, 1.8V	PL Bank66 IO16 differential positive. Same pin can be configured as PLSYSMON differential analog input3 positive or Single ended I/O.
76	PL_AA2_LVDS66_L24P	IO_L24P_T3U_N10_66	66	AA2	IO, 1.8V	PL Bank66 IO24 differential positive. Same pin can be configured as Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
78	PL_AA1_LVDS 66_L24N	IO_L24N_T3U_ N11_66	66	AA1	IO, 1.8V	PL Bank66 IO24 differential negative. Same pin can be configured as Single ended I/O.
80	PL_AC1_LVDS6 6_L23N	IO_L23N_T3U_ N9_66	66	AC1	IO, 1.8V	PL Bank66 IO23 differential negative. Same pin can be configured as Single ended I/O.
82	PL_AB1_LVDS6 6_L23P	IO_L23P_T3U_N 8_66	66	AB1	IO, 1.8V	PL Bank66 IO23 differential positive. Same pin can be configured as Single ended I/O.
84	PL_AB3_LVDS6 6_L22N_DBC	IO_L22N_T3U_ N7_DBC_AD0N_ 66	66	AB3	IO, 1.8V	PL Bank66 IO22 differential negative. Same pin can be configured as PLSYSMON differential analog input0 negative or Single ended I/O.
86	PL_AA3_LVDS 66_L22P_DBC	IO_L22P_T3U_N 6_DBC_AD0P_6 6	66	AA3	IO, 1.8V	PL Bank66 IO22 differential positive. Same pin can be configured as PLSYSMON differential analog input0 positive or Single ended I/O.
88	PL_AD2_LVDS 66_L19P_DBC	IO_L19P_T3L_N 0_DBC_AD9P_6 6	66	AD2	IO, 1.8V	PL Bank66 IO19 differential positive. Same pin can be configured as PLSYSMON differential analog input9 positive or Single ended I/O.
90	PL_AE2_LVDS6 6_L19N_DBC	IO_L19N_T3L_N 1_DBC_AD9N_6 6	66	AE2	IO, 1.8V	PL Bank66 IO19 differential negative. Same pin can be configured as PLSYSMON differential analog input9 negative or Single ended I/O.
92	PL_Y7_LVDS66 _L10P_QBC	IO_L10P_T1U_N 6_QBC_AD4P_6 6	66	Y7	IO, 1.8V	PL Bank66 IO10 differential positive. Same pin can be configured as PLSYSMON differential analog input4 positive or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
94	PL_AA7_LVDS 66_L10N_QBC	IO_L10N_T1U_ N7_QBC_AD4N_ 66	66	AA7	IO, 1.8V	PL Bank66 IO10 differential negative. Same pin can be configured as PLSYSMON differential analog input4 negative or Single ended I/O.
96	PL_AD6_LVDS 66_L8N	IO_L8N_T1L_N3 _AD5N_66	66	AD6	IO, 1.8V	PL Bank66 IO8 differential negative. Same pin can be configured as PLSYSMON differential analog input5 negative or Single ended I/O.
98	PL_AC6_LVDS6 6_L8P	IO_L8P_T1L_N2 _AD5P_66	66	AC6	IO, 1.8V	PL Bank66 IO8 differential positive. Same pin can be configured as PLSYSMON differential analog input5 positive or Single ended I/O.
100	PL_AC9_LVDS6 6_L7P_QBC	IO_L7P_T1L_N0 _QBC_AD13P_6 6	66	AC9	IO, 1.8V	PL Bank66 IO7 differential positive. Same pin can be configured as PLSYSMON differential analog input13 positive or Single ended I/O.
102	PL_AD9_LVDS 66_L7N_QBC	IO_L7N_T1L_N1 _QBC_AD13N_6 6	66	AD9	IO, 1.8V	PL Bank66 IO7 differential negative. Same pin can be configured as PLSYSMON differential analog input13 negative or Single ended I/O.
104	PL_AD11_LVD S66_L4P_DBC	IO_L4P_T0U_N6 _DBC_AD7P_66	66	AD11	IO, 1.8V	PL Bank66 IO4 differential positive. Same pin can be configured as PLSYSMON differential analog input7 positive or Single ended I/O.
106	PL_AD10_LVD S66_L4N_DBC	IO_L4N_T0U_N 7_DBC_AD7N_6 6	66	AD10	IO, 1.8V	PL Bank66 IO4 differential negative. Same pin can be configured as PLSYSMON differential analog input7 negative or Single ended I/O.
110	PL_AA8_LVDS 66_L12P_GC	IO_L12P_T1U_N 10_GC_66	66	AA8	IO, 1.8V	PL Bank66 IO12 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.

B2B2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination*	Description
112	PL_AB8_LVDS66_L12N_GC	IO_L12N_T1U_N11_GC_66	66	AB8	IO, 1.8V	PL Bank66 IO12 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
116	PL_AC8_LVDS66_L11P_GC	IO_L11P_T1U_N8_GC_66	66	AC8	IO, 1.8V	PL Bank66 IO11 differential positive. Same pin can be configured as GC Global Clock Input differential positive or Single ended I/O.
118	PL_AC7_LVDS66_L11N_GC	IO_L11N_T1U_N9_GC_66	66	AC7	IO, 1.8V	PL Bank66 IO11 differential negative. Same pin can be configured as GC Global Clock Input differential negative or Single ended I/O.
139	PL_AD5_LVDS66_L15P	IO_L15P_T2L_N4_AD11P_66	66	AD5	IO, 1.8V	PL Bank66 IO15 differential positive. Same pin can be configured as PLSYSMON differential analog input11 positive or Single ended I/O.
141	PL_AE5_LVDS66_L15N	IO_L15N_T2L_N5_AD11N_66	66	AE5	IO, 1.8V	PL Bank66 IO15 differential negative. Same pin can be configured as PLSYSMON differential analog input11 negative or Single ended I/O.
143	PL_AC2_LVDS66_L21N	IO_L21N_T3L_N5_AD8N_66	66	AC2	IO, 1.8V	PL Bank66 IO21 differential negative. Same pin can be configured as PLSYSMON differential analog input8 negative or Single ended I/O.
145	PL_AC3_LVDS66_L21P	IO_L21P_T3L_N4_AD8P_66	66	AC3	IO, 1.8V	PL Bank66 IO21 differential positive. Same pin can be configured as PLSYSMON differential analog input8 positive or Single ended I/O.

**IO Type of IOs originating from ZU7/5/4 MPSoC is configurable. Hence for exact IO type configuration options, refer Xilinx ZU7/5/4 MPSoC datasheet.*

2.8.3 Power & Reset Input

The Zynq Ultrascale+ MPSoC SOM works with 5V power input (VCC) from Board to Board Connector2 and generates all other required powers internally On-SOM itself. SOM power can be enabled/disabled from the carrier board through SOM Power enable pin (pin232) in Board to Board Connector1. Also in Board to Board Connector2, Ground pins are distributed throughout the connector for better performance.

The Zynq Ultrascale+ MPSoC SOM supports VCC_RTC coin cell power input from Board to Board Connector2 and connected to PMIC's VBBAT pin for real time clock backup voltage. Also it supports warm reset input from Board to Board Connector2 and connected to PS_SRST_B pin of MPSoC.

For more details on Power pins on Board to Board Connector2, refer the below table.

B2B-2 Pin No	B2B Connector2 Pin Name	MPSoC Pin Name	MPSoC Bank	MPSoC Pin No	Signal Type/ Termination	Description
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13,14, 15, 16, 17, 18, 19, 20	VCC_5V	NA	NA	NA	I, 5V Power	Supply Voltage.
21, 23, 37, 43, 49, 55, 73, 107, 113, 119, 129, 167, 173, 179, 185, 191, 197, 203, 209, 215, 221, 227, 233, 239, 22, 24, 30, 74, 108, 114, 120, 130, 168, 174, 180, 186, 192, 198, 204, 210, 216, 222, 228, 234, 240	GND	NA	NA	NA	Power	Ground.
68	VRTC_3V0	NA	NA	NA	I, 3V Power	3V backup coin cell input for RTC.
35	RESET_SW_IN	PS_SRST_B	503	P20	I, 1.8V LVCMOS/ 4.7K PU	Active low reset input.

2.9 Zynq Ultrascale+ MPSoC PS Pin Multiplexing on Board to Board Connectors

The Zynq Ultrascale+ MPSoC PS IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of MPSoC PS IO pins can be configured as GPIO if required. The below table provides the details of PS pin connections on Zynq Ultrascale+ MPSoC with selected pin function (highlighted) and available alternate functions. This table has been prepared by referring PS I/O configuration in Xilinx Vivado Design Suite. To know the complete available alternate functions, refer the PS I/O configuration in the latest Vivado Design Suite

Table 28: PS IOMUX on Zynq Ultrascale+ MPSoC SOM

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
On SOM Features from MPSoC PS																
eMMC FLASH	NA	PS_MIO13_500	GPIO13	NFC_CE	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
	NA	PS_MIO14_500	GPIO14	NFC_CLE	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	-
	NA	PS_MIO15_500	GPIO15	NFC_ALE	eMMC_DATA2	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	NA	PS_MIO16_500	GPIO16	NFC_DATA0	eMMC _DATA3	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	NA	PS_MIO17_500	GPIO17	NFC_DATA1	eMMC _DATA4	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	-
	NA	PS_MIO18_500	GPIO18	NFC_DATA2	eMMC _DATA5	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	-
	NA	PS_MIO19_500	GPIO19	NFC_DATA3	eMMC _DATA6	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	-
	NA	PS_MIO20_500	GPIO20	NFC_DATA4	eMMC _DATA7	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	-
	NA	PS_MIO21_500	GPIO21	NFC_DATA5	eMMC _CMD	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	-
	NA	PS_MIO22_500	GPIO22	NFC_WE_B	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
	NA	PS_MIO23_500	GPIO23	NFC_DATA6	eMMC_Reset	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
GEM0	NA	PS_MIO26_501	GPIO26	GEM0_TX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	NA	PS_MIO27_501	GPIO27	GEM0_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
	NA	PS_MIO28_501	GPIO28	GEM0_TXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	NA	PS_MIO29_501	GPIO29	GEM0_TXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
	NA	PS_MIO30_501	GPIO30	GEM0_TXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
	NA	PS_MIO31_501	GPIO31	GEM0_TX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	NA	PS_MIO32_501	GPIO32	GEM0_RX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	NA	PS_MIO33_501	GPIO33	GEM0_RXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	NA	PS_MIO34_501	GPIO34	GEM0_RXD1	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	NA	PS_MIO35_501	GPIO35	GEM0_RXD2	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	NA	PS_MIO36_501	GPIO36	GEM0_RXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	NA	PS_MIO37_501	GPIO37	GEM0_RX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	NA	PS_MIO76_502	GPIO76	GEM0_MDC	-	SD1_CLK	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	-	-
	NA	PS_MIO77_502	GPIO77	GEM0_MDIO	-	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	-	-
	NA	PS_MIO12_500	GPIO12	-	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	NA	PS_MIO42_501	GPIO42	GEM1_TXD3	eMMC _DATA1	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_MISO	-	UART0_RX	-	-
USB2.0	NA	PS_MIO52_502	GPIO52	GEM2_TX_CLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	USB0_CLK
	NA	PS_MIO53_502	GPIO53	GEM2_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	USB0_DIR
	NA	PS_MIO54_502	GPIO54	GEM2_TXD1	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TDO	SPI0_SS1	-	UART0_RX	-	USB0_DATA2
	NA	PS_MIO55_502	GPIO55	GEM2_TXD2	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	USB0_NXT
	NA	PS_MIO56_502	GPIO56	GEM2_TXD3	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-		UART1_TX	USB0_DATA0
	NA	PS_MIO57_502	GPIO57	GEM2_TX_CTL	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-		UART1_RX	USB0_DATA1
	NA	PS_MIO58_502	GPIO58	GEM2_RX_CLK	-	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	-	SPI1_SCLK	UART0_RX	-	USB0_STP
	NA	PS_MIO59_502	GPIO59	GEM2_RXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	-	SPI1_SS2	UART0_TX	-	USB0_DATA3
	NA	PS_MIO60_502	GPIO60	GEM2_RXD1	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	-	SPI1_SS1	-	UART1_TX	USB0_DATA4
	NA	PS_MIO61_502	GPIO61	GEM2_RXD2	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	-	SPI1_SS0	-	UART1_RX	USB0_DATA5
	NA	PS_MIO62_502	GPIO62	GEM2_RXD3	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB0_DATA6
	NA	PS_MIO63_502	GPIO63	GEM2_RX_CTL	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB0_DATA7

Interface/ Function	B2B Connector Pin Number	Zynq Ultrascale+ MPSoC Pin Name	GPIO	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12	Function 13
Board to Board Connector1 Interfaces from MPSoC PS																
GEM3/USB1	190	PS_MIO64_502	GPIO64	GEM3_TX_CLK	eMMC _CLK	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_SCLK	-	-	UART1_TX	USB1_CLK
	192	PS_MIO65_502	GPIO65	GEM3_TXD0	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_SS2	-	-	UART1_RX	USB1_DIR
	194	PS_MIO66_502	GPIO66	GEM3_TXD1	eMMC _CMD	-	CAN0_RX	-	I2C0_SCL	-	-	SPI0_SS1	-	UART0_RX	-	USB1_DATA2
	196	PS_MIO67_502	GPIO67	GEM3_TXD2	eMMC_DATA0	-	CAN0_TX	-	I2C0_SDA	-	-	SPI0_SS0	-	UART0_TX	-	USB1_NXT
	198	PS_MIO68_502	GPIO68	GEM3_TXD3	eMMC _DATA1	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	USB1_DATA0
	210	PS_MIO69_502	GPIO69	GEM3_TX_CTL	eMMC_DATA2	SD1_WP	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MIOSI	-	-	UART1_RX	USB1_DATA1
	212	PS_MIO70_502	GPIO70	GEM3_RX_CLK	eMMC _DATA3	SD1_PWR	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SCLK	UART0_RX	-	USB1_STP
	224	PS_MIO71_502	GPIO71	GEM3_RXD0	eMMC _DATA4	SD1_DATA0	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS2	UART0_TX	-	USB1_DATA3
	226	PS_MIO72_502	GPIO72	GEM3_RXD1	eMMC _DATA5	SD1_DATA1	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SS1	-	UART1_TX	USB1_DATA4
	228	PS_MIO73_502	GPIO73	GEM3_RXD2	eMMC _DATA6	SD1_DATA2	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS0	-	UART1_RX	USB1_DATA5
	230	PS_MIO74_502	GPIO74	GEM3_RXD3	eMMC _DATA7	SD1_DATA3	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	USB1_DATA6
	214	PS_MIO75_502	GPIO75	GEM3_RX_CTL	eMMC_Reset	SD1_CMD	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	USB1_DATA7
CAN0	207	PS_MIO38_501	GPIO38	GEM1_TX_CLK	eMMC _CLK	-	CAN0_RX	-	I2C0_SCL	-	PJTAG_TCK	SPI0_SCLK	-	UART0_RX	-	-
	209	PS_MIO39_501	GPIO39	GEM1_TXD0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TDI	SPI0_SS2	-	UART0_TX	-	-
CAN1	213	PS_MIO40_501	GPIO40	GEM1_TXD1	eMMC _CMD	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TDO	SPI0_SS1	-	-	UART1_TX	-
	211	PS_MIO41_501	GPIO41	GEM1_TXD2	eMMC_DATA0	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TMS	SPI0_SS0	-	-	UART1_RX	-
GPIO	178	PS_MIO1_500	GPIO1	QSPI_MISO	-	-	-	CAN1_RX	-	I2C1_SDA	PJTAG_TDI	SPI0_SS2	-	-	UART1_RX	-
Board to Board Connector2 Interfaces from MPSoC PS																
SD1(4-Bit)	40	PS_MIO44_501	GPIO44	GEM1_RX_CLK	eMMC _DATA3	SD1_WP	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_SCLK	-	UART1_TX	-
	42	PS_MIO45_501	GPIO45	GEM1_RXD0	eMMC _DATA4	SD1_CD	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_SS2	-	UART1_RX	-
	44	PS_MIO43_501	GPIO43	GEM1_TX_CTL	eMMC_DATA2	SD1_PWR	CAN0_TX	-	I2C0_SDA	-	-	SPI0_MIOSI	-	UART0_TX	-	-
	69	PS_MIO46_501	GPIO46	GEM1_RXD1	eMMC _DATA5	SD1_DATA0	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_SS1	UART0_RX	-	-
	66	PS_MIO47_501	GPIO47	GEM1_RXD2	eMMC _DATA6	SD1_DATA1	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_SS0	UART0_TX	-	-
	64	PS_MIO48_501	GPIO48	GEM1_RXD3	eMMC _DATA7	SD1_DATA2	-	CAN1_TX	-	I2C1_SCL	-	-	SPI1_MISO	-	UART1_TX	-
	62	PS_MIO49_501	GPIO49	GEM1_RX_CTL	eMMC_Reset	SD1_DATA3	-	CAN1_RX	-	I2C1_SDA	-	-	SPI1_MIOSI	-	UART1_RX	-
	71	PS_MIO50_501	GPIO50	GEM1_MDC	-	SD1_CMD	CAN0_RX	-	I2C0_SCL	-	-	-	-	UART0_RX	-	-
	72	PS_MIO51_501	GPIO51	GEM1_MDIO	-	SD1_CLK	CAN0_TX	-	I2C0_SDA	-	-	-	-	UART0_TX	-	-
SPI	61	PS_MIO0_500	GPIO0	QSPI_SCLK	-	-	-	CAN1_TX	-	I2C1_SCL	PJTAG_TCK	SPI0_SCLK	-	-	UART1_TX	-
	63	PS_MIO3_500	GPIO3	QSPI_SS0	-	-	CAN0_TX	-	I2C0_SDA	-	PJTAG_TMS	SPI0_SS0	-	UART0_TX	-	-
	67	PS_MIO4_500	GPIO4	-	-	-	-	CAN1_TX	-	I2C1_SCL	-	SPI0_MISO	-	-	UART1_TX	-
	65	PS_MIO5_500	GPIO5	-	-	-	-	CAN1_RX	-	I2C1_SDA	-	SPI0_MOSI	-	-	UART1_RX	-
I2C0	46	PS_MIO11_500	GPIO11	-	-	-	CAN0_TX	-	I2C0_SDA	-	-	-	SPI1_MIOSI	UART0_TX	-	-
	48	PS_MIO10_500	GPIO10	NFC_RB_N	-	-	CAN0_RX	-	I2C0_SCL	-	-	-	SPI1_MISO	UART0_RX	-	-
GPIOs/I2C1	38	PS_MIO25_500	GPIO25	NFC_RE_N	-	-	-	CAN1_RX	-	I2C1_SDA	-	-	-	-	UART1_RX	-
	70	PS_MIO24_500	GPIO24	NFC_DATA7	-	-	-	CAN1_TX	-	I2C1_SCL	-	-	-	-	UART1_TX	-
JTAG	27	PS_JTAG_TDI	-	PS_JTAG_TDI	-	-	-	-	-	-	-	-	-	-	-	-
	29	PS_JTAG_TMS	-	PS_JTAG_TMS	-	-	-	-	-	-	-	-	-	-	-	-
	31	PS_JTAG_TCK	-	PS_JTAG_TCK	-	-	-	-	-	-	-	-	-	-	-	-
	33	PS_JTAG_TDO	-	PS_JTAG_TDO	-	-	-	-	-	-	-	-	-	-	-	-

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq Ultrascale+ MPSoC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of Zynq Ultrascale+ MPSoC SOM.

Table 29: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[2]	0V	3V	3.15V	±20mV

[1] Zynq Ultrascale+ MPSoC SOM is designed to work with VCC_5V input power rail from Board to Board Connector2.

[2] Zynq Ultrascale+ MPSoC SOM uses this voltage as backup power source to PMIC RTC when VCC_5V is off. This is an optional power and required only if RTC functionality is used.

3.1.2 Power Input Sequencing

The Zynq Ultrascale+ MPSoC SOM Power Input sequence requirement is explained below.

Power up Sequence:

- VRTC_3V0 must come up at the same time or before VCC_5V comes up.
- SOMPWR_EN signal from Board to Board Connector1 must be high at the same time or after VCC_5V comes up.

Power down Sequence:

- SOMPWR_EN signal from Board to Board Connector1 must be low at the same time or before VCC_5V goes down.
- VCC_5V must go down at the same time or before VRTC_3V0 goes down.

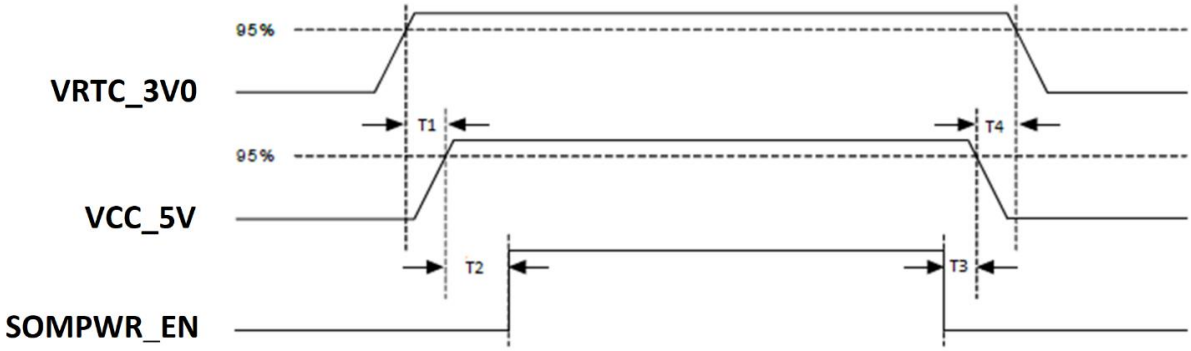


Figure 9: Power Input Sequencing

Table 30: Power Sequence Timing

Item	Description	Value
T1	VRTC_3V0[1] rise time to VCC_5V rise time	≥ 0 ms
T2	VCC_5V rise time to SOMPWR_EN rise time	≥ 0 ms
T3	SOMPWR_EN fall time to VCC_5V fall time	≥ 0 ms
T4	VCC_5V fall time to VRTC_3V0 fall time	≥ 0 ms

[1] VRTC_3V0 is the RTC Battery backup supply. This is an optional power.

Important Note: VCC_5V input power to other all the powers are getting stable around 50ms in SOM, Make sure that from the carrier board IOs shall not driving before all the SOM powers are stable.

3.1.3 Power Consumption

Table 31: Power Consumption

Task/Status	Power Rail	Current Drawn/Power Consumption
Typical Power Test: • File transfer between storage devices eMMC, SD, USB3.0 & SATA • Dual Ethernet (GEM0 & GEM3) ping test (65507 packet size) • Run the VPU test • Run the GPU test • Run the Dhrystone application • GTH Transceivers Loopback • Run 3G SDI In & SDI out	VCC_5V	3.45A/17.25W

Note: This measurement is done in ZU19EG -1 speed grade SOM with iWave's FPGA Design & PetaLinux BSP release.

For more accurate power estimation, iWave recommends to use Xilinx Power Estimator (XPE) tool and calculate the MPSoC power. Also add extra 3A for other On-SOM peripherals power.

For reference, we have calculated the Zynq Ultrascale+ MPSoC (ZU7/5/4) Theoretical Power Estimation by using Xilinx Power Estimator (XPE) tool with various FPGA utilisation and ambient temperature as shown below.

FPGA Utilisation (%)	SOM Theoretical Power Estimation @ 5V			
	25 C Ambient		60 C Ambient	
	TYP	Max	TYP	Max
50	6.515A/32.575W	7.818A/39.09W	7.441A/37.205W	8.922A/44.61W
80	7.476A/37.38W	8.964A/44.82W	8.631A/43.155W	10.358A/51.79W
100	8.199A/40.995W	9.838A/49.190W	9.595A/47.975W	13.021/65.105W

Note: This calculation is based on 7EV device with maximum Process @ -3 Speed Grade

3.2 Environmental Characteristics

3.2.1 Temperature Specification

The below table provides the Environment specification of Zynq Ultrascale+ MPSoC SOM.

Table 32: Temperature Specification

Parameters	Min	Max
Operating temperature range - Industrial[1]	-40°C	85°C
Operating temperature range - Extended[1]	0°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 RoHS2 Compliance

iWave's Zynq Ultrascale+ MPSoC SOM is designed by using RoHS2 compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

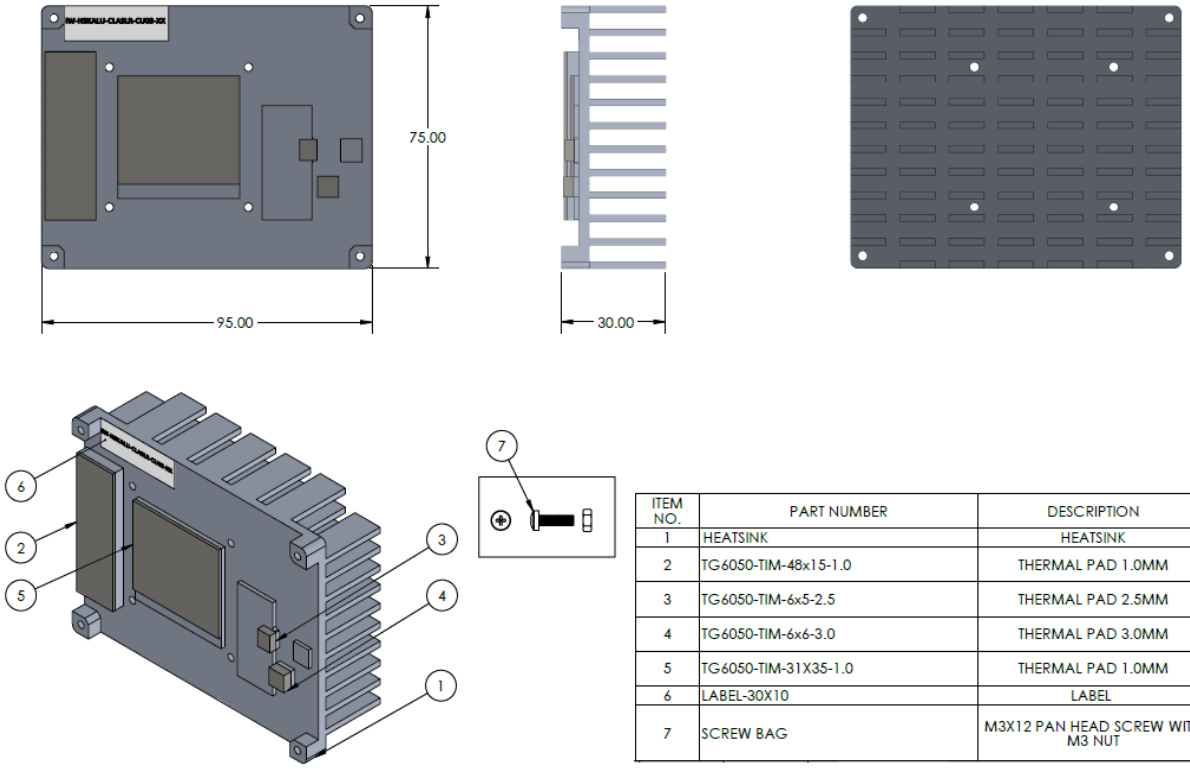
iWave's Zynq Ultrascale+ MPSoC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique Heat sink must be used. Always remember that, if you use more effective thermal solution, you will get more performance out of the CPU.

iWave supports Heat Sink Solution for Zynq Ultrascale+ MPSoC SOM. Please refer the below figure for Heat Sink dimension details. For Heat Sink ordering information, please refer section **4 ORDERING INFORMATION**.



ITEM NO.	PART NUMBER	DESCRIPTION	QTY.
1	HEATSINK	HEATSINK	1
2	TG6050-TIM-48x15-1.0	THERMAL PAD 1.0MM	1
3	TG6050-TIM-6x5-2.5	THERMAL PAD 2.5MM	1
4	TG6050-TIM-6x6-3.0	THERMAL PAD 3.0MM	1
5	TG6050-TIM-31X35-1.0	THERMAL PAD 1.0MM	1
6	LABEL-30X10	LABEL	1
7	SCREW BAG	M3X12 PAN HEAD SCREW WITH M3 NUT	4

Figure 10: Heat Sink Dimensions

3.3 MechanicalCharacteristics

3.3.1 Zynq Ultrascale+ MPSoC SOM Mechanical Dimensions

Zynq Ultrascale+ MPSoC SOM PCB size is 95mm x 75mm x 1.6mm and weight is 45g. SOM mechanical dimension is shown below.

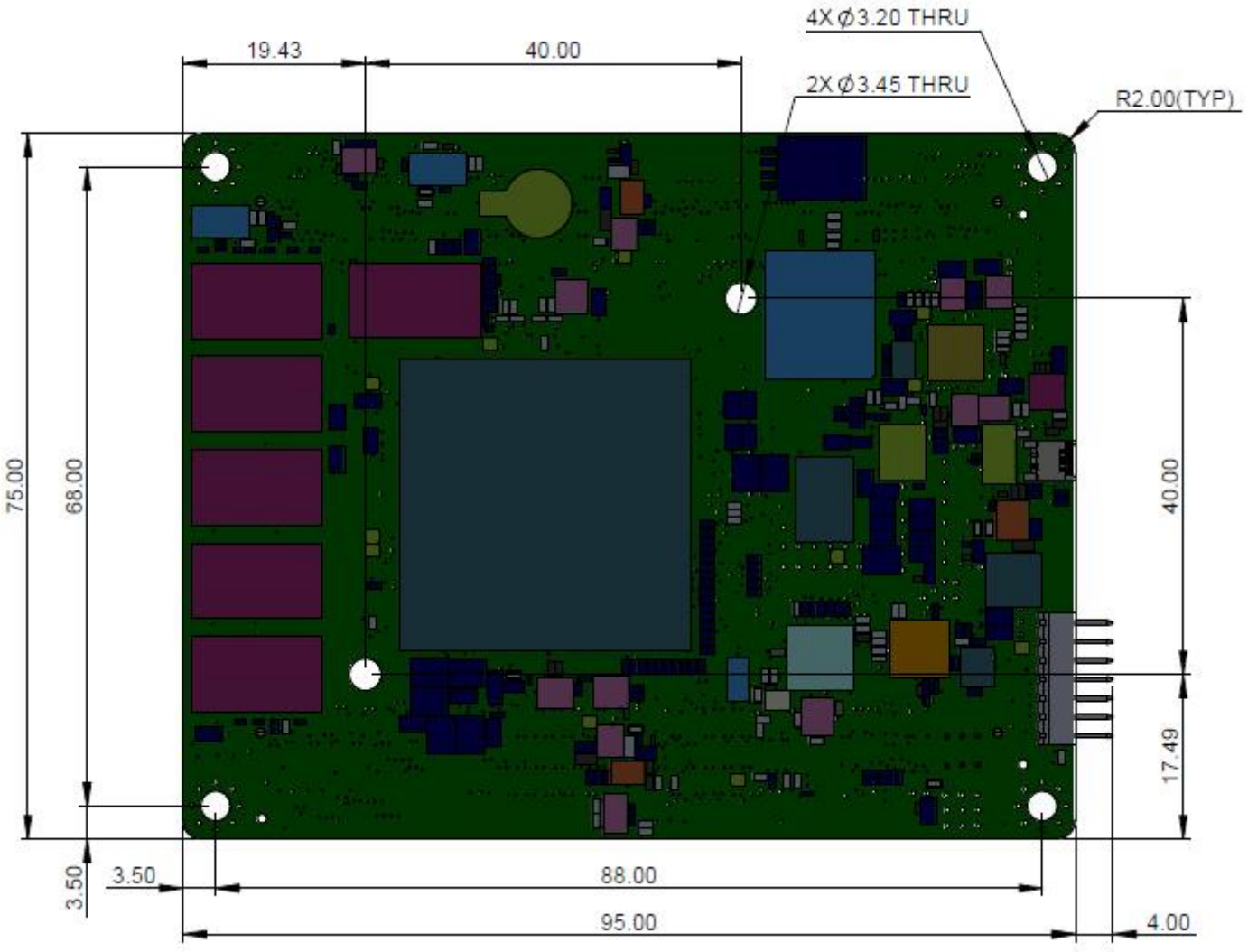


Figure 11: Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Top View

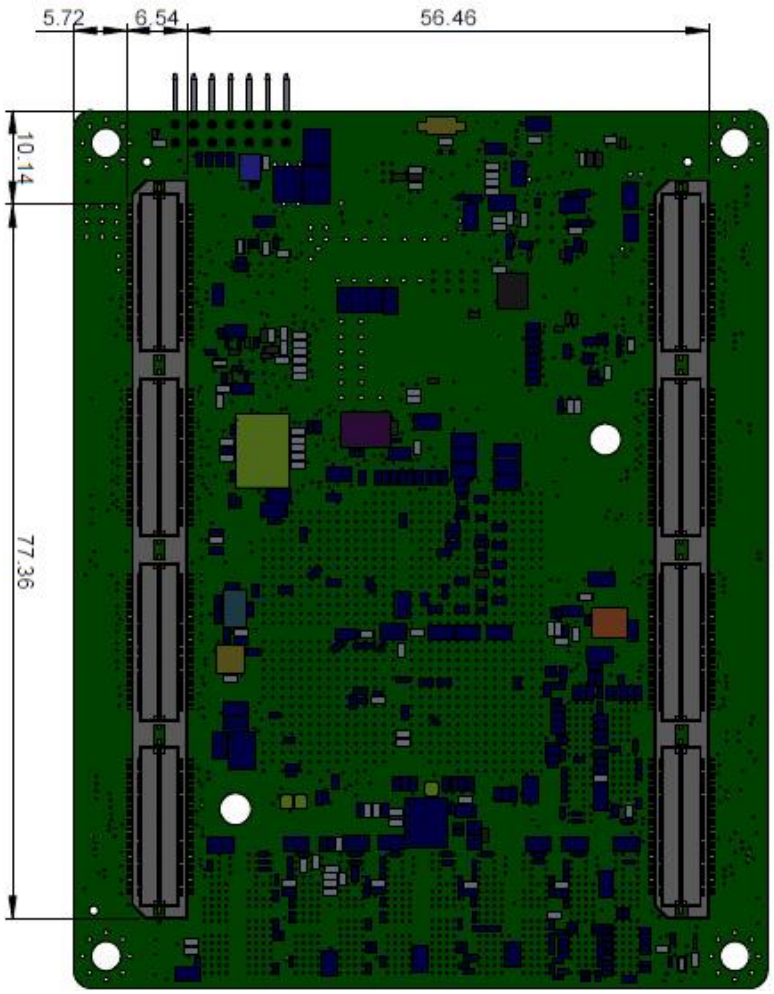


Figure 12: Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Bottom View

Zynq Ultrascale+ MPSoC SOM PCB thickness is 1.6mm±0.1mm, top side maximum height component is JTAG Header(4.30mm) followed by Fan Header (3.5mm) and bottom side maximum height component is Board to Board Connectors (4.27mm) followed by Bulk capacitors (2.5mm). Please refer the below figure which gives height details of the Zynq Ultrascale+ MPSoC SOM.

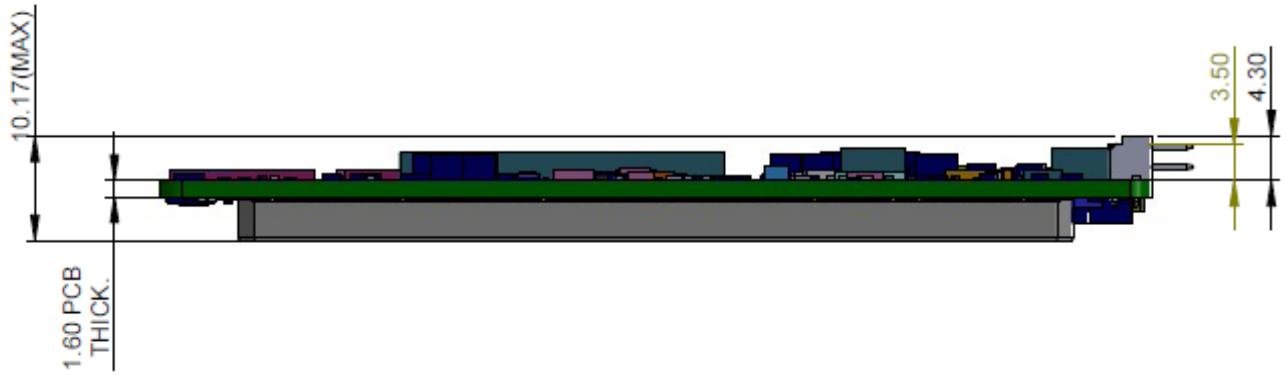


Figure 13: Mechanical dimension of Zynq Ultrascale+ MPSoC SOM - Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different Zynq Ultrascale+ MPSoC SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 33: Orderable Product Part Numbers

Product Part Number	Description	Temperature
ZU7 MPSoC based SOM		
iW-G30M-C7EV-4E004G-E008G-BIA	ZU7EV (-1) MPSOC(XCZU7EV-1FBVB900I), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Industrial
iW-G30M-C7EV-4E004G-E008G-LIA	ZU7EV (-1) MPSOC(XCZU7EV-1FBVB900I), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC- Linux	Industrial
iW-G30M-C7CG-4E004G-E008G-BIA	ZU7CG (-1) MPSOC(XCZU7CG-1FBVB900I), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC- Boot code	Industrial
iW-G30M-C7CG-4E004G-E008G-LIA	ZU7CG (-1) MPSOC (XCZU7CG-1FBVB900I), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Industrial
iW-G30M-C7EV-4E004G-E008G-BEA	ZU7EV (-1) MPSOC(XCZU7EV-1FBVB900E), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended
iW-G30M-C7EV-4E004G-E008G-LEA	ZU7EV (-1) MPSOC(XCZU7EV-1FBVB900E), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC- Linux	Extended
iW-G30M-C7CG-4E004G-E008G-BEA	ZU7CG (-1) MPSOC(XCZU7CG-1FBVB900E), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended
iW-G30M-C7CG-4E004G-E008G-LEA	ZU7CG (-1) MPSOC(XCZU7CG-1FBVB900E), 4GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Extended
ZU5 MPSoC based SOM		
iW-G30M-C5EV-4E002G-E008G-LIA	ZU5EV (-1) MPSOC (XCZU5EV-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Industrial
iW-G30M-C5EV-4E002G-E008G-BIA	ZU5EV (-1) MPSOC(XCZU5EV-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Industrial
iW-G30M-C5EV-4E002G-E008G-LEA	ZU5EV (-1) MPSOC (XCZU5EV-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Extended
iW-G30M-C5EV-4E002G-E008G-BEA	ZU5EV (-1) MPSOC(XCZU5EV-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended

Product Part Number	Description	Temperature
ZU4 MPSoC based SOM		
iW-G30M-C4EV-4E002G-E008G-BIA	ZU4EV (-1) MPSOC (XCZU4EV-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Industrial
iW-G30M-C4EV-4E002G-E008G-LIA	ZU4EV (-1) MPSOC (XCZU4EV-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Industrial
iW-G30M-C4EG-4E002G-E008G-BIA	ZU4EG (-1) MPSOC (XCZU4EG-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Industrial
iW-G30M-C4EG-4E002G-E008G-LIA	ZU4EG (-1) MPSOC (XCZU4EG-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Industrial
iW-G30M-C4CG-4E002G-E008G-BIA	ZU4CG (-1) MPSOC (XCZU4CG-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Industrial
iW-G30M-C4CG-4E002G-E008G-LIA	ZU4CG (-1) MPSoC (XCZU4CG-1FBVB900I), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Industrial
iW-G30M-C4EV-4E002G-E008G-BEA	ZU4EV (-1) MPSOC (XCZU4EV-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended
iW-G30M-C4EV-4E002G-E008G-LEA	ZU4EV (-1) MPSOC (XCZU4EV-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Extended
iW-G30M-C4EG-4E002G-E008G-BEA	ZU4EG (-1) MPSOC (XCZU4EG-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended
iW-G30M-C4EG-4E002G-E008G-LEA	ZU4EG (-1) MPSOC (XCZU4EG-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Extended
iW-G30M-C4CG-4E002G-E008G-BEA	ZU4CG (-1) MPSOC (XCZU4CG-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Boot code	Extended
iW-G30M-C4CG-4E002G-E008G-LEA	ZU4CG (-1) MPSOC (XCZU4CG-1FBVB900E), 2GB PS DDR4 with ECC, 1GB PL DDR4, 8GB EMMC - Linux	Extended
Heat Sink		
iW-HSKALU-CLASLR-CU03	Heat Sink for Zynq Ultrascale+ MPSoC SOM	-

Important Note: Some of the above-mentioned Part Number is subject to MOQ purchase. Please contact iWave for further details.

Note: For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX

5.1 Zynq Ultrascale+ MPSoC SOM Development Platform

iWave Systems supports iW-RainboW-G30D – Zynq Ultrascale+ MPSoC SOM Development Platform which is targeted for quick validation of Zynq Ultrascale+ MPSoC based SOM. iWave's Zynq Ultrascale+ MPSoC Development Board incorporates Zynq Ultrascale+ MPSoC SOM and High performance Carrier board with complete BSP support.

For more details on Zynq Ultrascale+ MPSoC SOM Development Platform, visit the below web link.

https://www.iwavesystems.com/product/dev-kits/fpga/ultrascale-dev-kit/zynq-ultrascale-dev-kit.html

Figure 14: Zynq Ultrascale+ MPSoC SOM Development Platform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