Zynq-7000 SoC

SODIMM Development Platform

Hardware User Guide

iWave

Embedding Intelligence

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India – 560076

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1. INTRODUCTION

1.1 Purpose

The Zynq-7000 SoC SODIMM Development platform incorporates Zynq-7000 SoC based SODIMM SOM and SODIMM Carrier board for complete validation of Zynq-7000 SoC functionality. This document is the Hardware User Guide for the Zynq-7000 SoC SODIMM Carrier Board and provides detailed information on the overall design & usage of the Carrier Board from a Hardware Systems perspective. The details about the Zynq-7000 SoC SODIMM SOM hardware is explained in Zynq-7000 SoC SODIMM SOM hardware user guide document.

1.2 Overview

iWave's Zynq-7000 SoC SODIMM Development platform incorporates Zynq 7000 SoC SODIMM SOM which is based on Xilinx's Zynq-7000 SoC and the SODIMM Carrier Board. With the 100mmx72mm size, carrier board is packed with all the necessary on-board connectors to validate the features of Zynq-7000 SoC SODIMM SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor Signal
CPU	Central Processing Unit
FMC	FPGA Mezzanine Card
GPIO	General Purpose Input Output
HPC	High Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
NPTH	Non Plated Through hole
PCB	Printed Circuit Board
PTH	Plated Through hole
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SOM	System On Module
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
TMDS	Transition-Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Zynq-7000 SoC Datasheet & Reference Manual
- Zynq-7000 SoC SODIMM SOM Hardware User Guide

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Zynq-7000 SoC SODIMM Development platform carrier board features with high level block diagram and detailed information about each block.

2.1 Zynq SODIMM Carrier Board Block Diagram

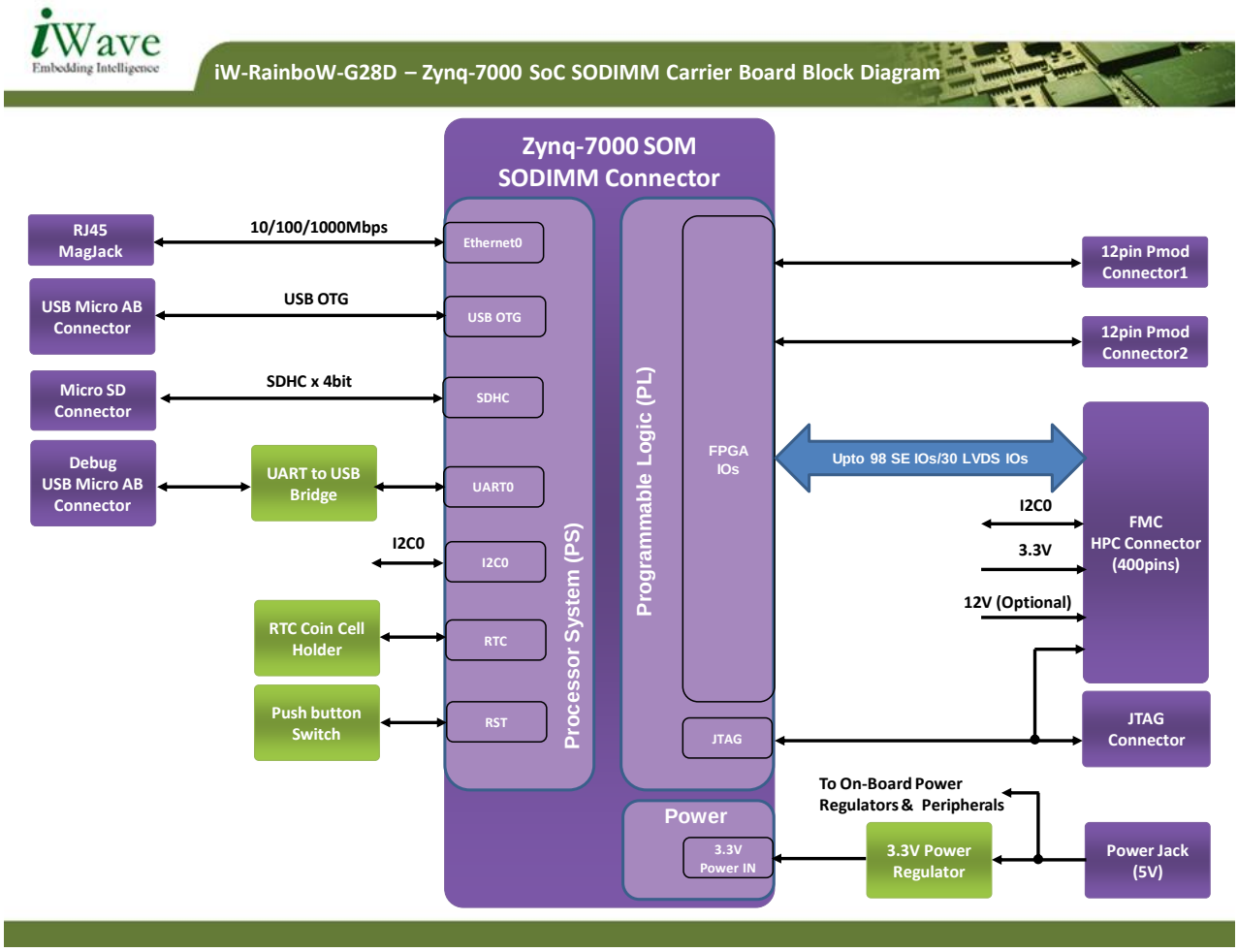

Figure 1: Zynq-7000 SoC SODIMM Carrier Board Block Diagram

2.2 Zynq-7000 SoC SODIMM Carrier Board Features

The Zynq-7000 SoC SODIMM carrier board supports the following features to validate the Zynq-7000 SoC SOM SODIMM Edge Connector features.

Serial Interface Features

- Debug UART through USB MicroAB Connector

Communication Features

- Gigabit Ethernet through RJ45MagJack x 1
- USB2.0 OTG through MicroAB Connector x 1
- SDIO through Micro SD Connector x 1

Expansion Connectors

- FMC High Pin Count (HPC) Connector x 1
  - Upto 98 Single ended (SE) IOs/30 LVDS IOs
- 12pin PMOD Host Port Connector x 2
  - 16 Single ended (SE) IOs (8 IOs on each connector)

Additional Features

- JTAG Connector x 1
- Power ON/OFF DIP Switch x 1
- Reset Pushbutton Switch x 1
- RTC Coin Cell Holder x 1

General Specification

- Power Supply : 5V Power Input Jack
- Form Factor : 100mm X 72mm

Note: In Zynq-7000 SoC, PL Bank13 is not available in Z-7007S and Z-7010 devices and so Bank13 IOs (20 SE IOs) on FMC connector & Pmod connector1 is NC in Z-7007S and Z-7010 SoC based SODIMM DevKit.

2.3 SODIMM Connector

The Zynq-7000 SoC SODIMM Carrier board supports 200 Pin SODIMM Edge mating connector for SODIMM SOM attachment. This standard 200-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This SODIMM Edge mating connector (J7) is physically located at the top of the board as shown below.

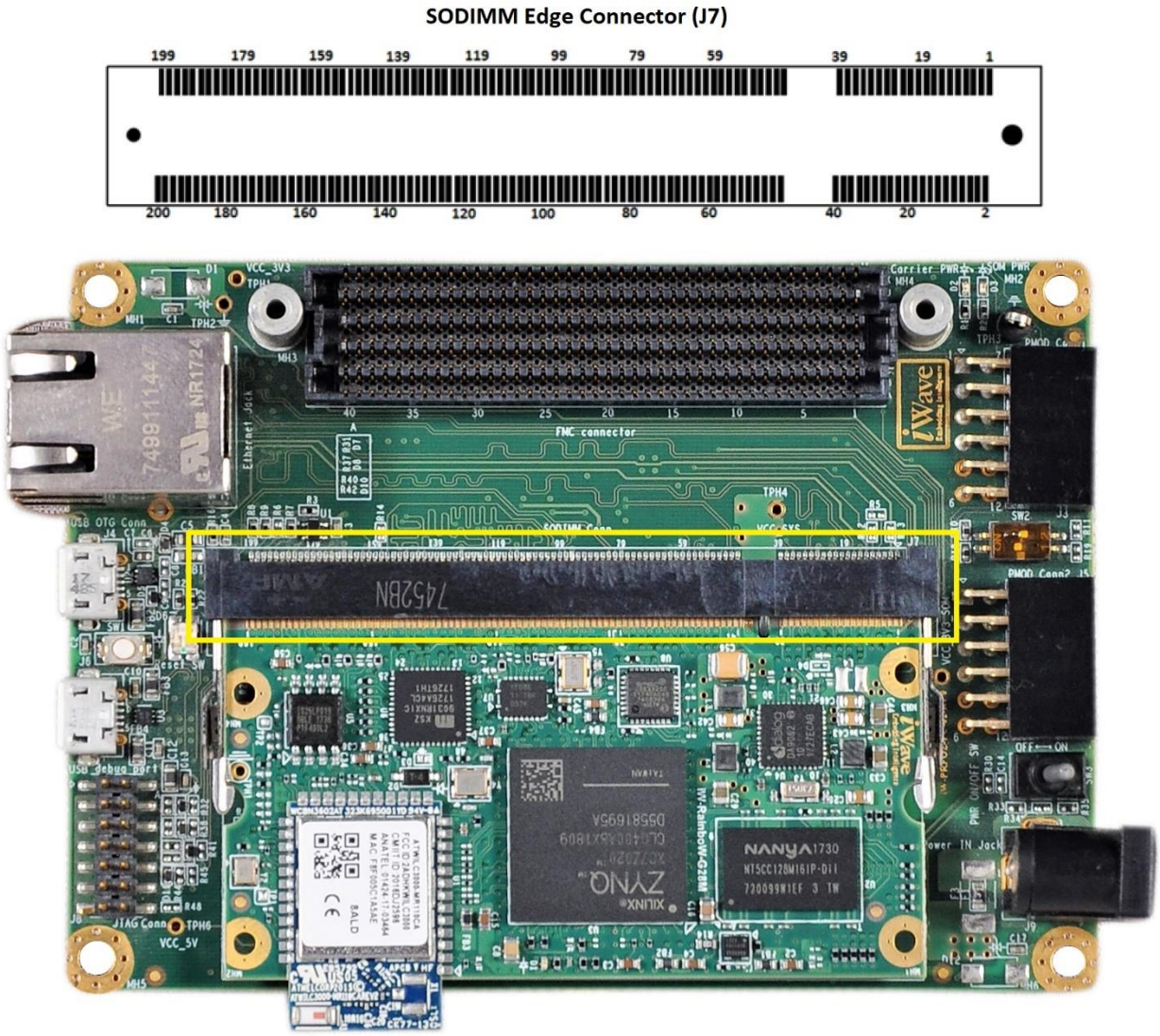

Figure 2: SODIMM Edge Connector

Table 3: SODIMM Edge Connector Pin Out

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
1	GND	Power	Ground.
2	GPHY_ATXRXM	IO, DIFF	Ethernet transmit differential pair 0 negative. This pin is connected to RJ45 Magjack.
3	NC	NA	NC.
4	GPHY_ATXRXP	IO, DIFF	Ethernet transmit differential pair 0 positive. This pin is connected to RJ45 Magjack.
5	GND	Power	Ground.
6	GPHY_BTXRXM	IO, DIFF	Ethernet receive differential pair 1 negative. This pin is connected to RJ45 Magjack.
7	PL_IO_L19N_T3_VREF_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. *Note: Optionally this pin is connected to E13th pin of FMC connector (J1) through resistor and default not populated.*
8	GPHY_BTXRXP	IO, DIFF	Ethernet receive differential pair 1 positive. This pin is connected to RJ45 Magjack.
9	PL_IO_L19P_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. *Note: Optionally this pin is connected to K16th pin of FMC connector (J1) through resistor and default not populated.*
10	PL_IO_L6N_T0_VREF_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to 2nd pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to E19th pin of FMC connector (J1) through resistor and default not populated.*
11	GPHY_LINK_LED2	I, 3.3V CMOS	Gigabit Ethernet link status LED.
12	GPHY_ACTIVITY_LED1	I, 3.3V CMOS	Gigabit Ethernet speed status LED.
13	GND	Power	Ground.
14	GPHY_CTXRXM	IO, DIFF	Gigabit Ethernet differential pair 3 negative.
15	GPHY_DTXRXM	IO, DIFF	Gigabit Ethernet differential pair 4 negative.
16	GPHY_CTXRXP	IO, DIFF	Gigabit Ethernet differential pair 3 positive.
17	GPHY_DTXRXP	IO, DIFF	Gigabit Ethernet differential pair 4 positive.
18	PL_IO_L11N_T1_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K14th pin of FMC connector (J1).
19	PL_IO_L11P_T1_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K13th pin of FMC connector (J1)
20	VIN_3V3	O, 3.3V Power	Supply Voltage.

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
21	PL_IO_L22P_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K10th pin of FMC connector (J1).
22	PL_IO_L15P_T2_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to E6th pin of FMC connector (J1).
23	PL_IO_L22N_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K11th pin of FMC connector (J1).
24	PL_IO_L15N_T2_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to E7th pin of FMC connector (J1).
25	NC	NA	NC.
26	PL_IO_L12P_T1_MRCC_13	IO, 3.3V CMOS	Bank13 Clock user Multi region positive Single ended pin. This pin is connected to E2nd pin of FMC connector (J1).
27	GND	Power	Ground.
28	PL_IO_L12N_T1_MRCC_13	IO, 3.3V LVCMOS	Bank13 Clock user Multi region negative Single ended pin. This pin is connected to E3rd pin of FMC connector (J1).
29	PL_IO_L20P_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K7th pin of FMC connector (J1).
30	PL_IO_L18P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to J9th pin of FMC connector (J1).
31	PL_IO_L20N_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to K8th pin of FMC connector (J1).
32	VIN_3V3	O, 3.3V Power	Supply Voltage.
33	PL_IO_L18N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to J10th pin of FMC connector (J1).
34	PL_IO_L1N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H8th pin of FMC connector (J1).
35	PL_IO_L2N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G10th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
36	PL_IO_L1P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H7th pin of FMC connector (J1).
37	PL_IO_L2P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G9th pin of FMC connector (J1).
38	PL_IO_L10N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G13th pin of FMC connector (J1).
39	PL_IO_L10P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G12th pin of FMC connector (J1).
40	GND	Power	Ground.
41	GND	Power	Ground.
42	PL_IO_L18N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H17th pin of FMC connector (J1).
43	PL_IO_L23N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C19th pin of FMC connector (J1).
44	PL_IO_L18P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H16th pin of FMC connector (J1).
45	PL_IO_L23P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C18th pin of FMC connector (J1).
46	VIN_3V3	O, 3.3V Power	Supply Voltage.
47	PL_IO_L13N_T2_MRCC_34	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to 2nd pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to J16th pin of FMC connector (J1) through resistor and default not populated.*
48	PL_IO_L17N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F8th pin of FMC connector (J1).
49	NC	NA	NC.
50	PL_IO_L17P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F7th pin of FMC connector (J1).
51	GND	Power	Ground.

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
52	PL_IO_L13N_T2_MRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F5th pin of FMC connector (J1).
53	PL_IO_L14N_T2_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to E10th pin of FMC connector (J1).
54	PL_IO_L13P_T2_MRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F4th pin of FMC connector (J1).
55	PL_IO_L14P_T2_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to E9th pin of FMC connector (J1).
56	PL_IO_L21N_T3_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to J7th pin of FMC connector (J1).
57	PL_IO_L16N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F11th pin of FMC connector (J1).
58	PL_IO_L21P_T3_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to J6th pin of FMC connector (J1).
59	PL_IO_L16P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected to F10th pin of FMC connector (J1).
60	VIN_3V3	O, 3.3V Power	Supply Voltage.
61	PL_IO_L8N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H14th pin of FMC connector (J1).
62	PL_IO_L4N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H11th pin of FMC connector (J1).
63	PL_IO_L8P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H13th pin of FMC connector (J1).
64	PL_IO_L4P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H10th pin of FMC connector (J1).
65	GND	Power	Ground.
66	PL_IO_L7N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C11th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
67	PL_IO_L11N_T1_SRCC_34	O, 3.3V CMOS	Bank34 Clock user Single region negative Single ended pin. This pin is connected to G3rd pin of FMC connector (J1).
68	PL_IO_L7P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C10th pin of FMC connector (J1).
69	PL_IO_L11P_T1_SRCC_34	O, 3.3V LVCMOS	Bank34 Clock user Single region positive Single ended pin. This pin is connected to G2nd pin of FMC connector (J1).
70	PL_IO_L17P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C14th pin of FMC connector (J1).
71	PL_IO_L6N_T0_VREF_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 10th pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to K17th pin of FMC connector (J1) through resistor and default not populated.*
72	VIN_3V3	O, 3.3V Power	Supply Voltage.
73	PL_IO_L6P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 9th pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to F13th pin of FMC connector (J1) through resistor and default not populated.*
74	PL_IO_L17N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to C15th pin of FMC connector (J1).
75	PL_IO_0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 9th pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to C30th pin of FMC connector (J1) through resistor and default not populated.*
76	PL_IO_25_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 7th pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to C31st pin of FMC connector (J1) through resistor and default not populated.*

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
77	USB_OTG_ID	O, 3.3V CMOS	USB OTG ID input for USB host or device detection. This pin is connected from Micro USB OTG connector (J4).
78	USB_PWR_EN	I, 3.3V CMOS	USB active high power enable output to control external USB Vbus. This pin is connected to USB OTG Power switch enable pin to control USB OTG VBUS power.
79	GND	Power	Ground.
80	PL_IO_L3P_T0_DQS_PUDC_B_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. *Note: Optionally this pin is connected to J15th pin of FMC connector (J1) through resistor and default not populated.*
81	USB_OTG_DP	IO, DIFF	USB OTG data positive. This pin is connected to Micro USB OTG connector (J4).
82	NC	NA	NC.
83	USB_OTG_DM	IO, DIFF	USB OTG data negative. This pin is connected to Micro USB OTG connector (J4).
84	NC	NA	NC.
85	NC	NA	NC.
86	PL_IO_L9P_T1_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H19th pin of FMC connector (J1).
87	NC	NA	NC.
88	VIN_3V3	O, 3.3V Power	Supply Voltage.
89	PL_IO_L9N_T1_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to H20th pin of FMC connector (J1).
90	PL_IO_L12P_T1_MRCC_34	O, 3.3V LVCMOS	Bank34 Clock user Multi region positive Single ended pin. This pin is connected to H4th pin of FMC connector (J1).
91	PL_IO_L19P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 1st pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to F16th pin of FMC connector (J1) through resistor and default not populated.*

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
92	PL_IO_L12N_T1_MRCC_34	O, 3.3V LVCMOS	Bank34 Clock user Multi region negative Single ended pin. This pin is connected to H5th pin of FMC connector (J1).
93	PL_IO_L19N_T3_VREF_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 4th pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to J19th pin of FMC connector (J1) through resistor and default not populated.*
94	PL_IO_L22P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to D17th pin of FMC connector (J1).
95	GND	Power	Ground.
96	PL_IO_L22N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to D18th pin of FMC connector (J1).
97	PL_IO_L5P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to D11th pin of FMC connector (J1).
98	PL_IO_L21P_T3_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G21st pin of FMC connector (J1).
99	PL_IO_L5N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to D12th pin of FMC connector (J1).
100	PL_IO_L21N_T3_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G22nd pin of FMC connector (J1).
101	PL_IO_L20P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G15th pin of FMC connector (J1).
102	PL_IO_L16P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to D14th pin of FMC connector (J1).
103	PL_IO_L20N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is optionally connected to G16th pin of FMC connector (J1).
104	PL_IO_L16N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is optionally connected to D15th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
105	SD0_CD(PS_MIO48_501)	O, 1.8V LVCMOS/	SD0 Card Detect pin. This pin is connected from Micro SD connector for card detection.
106	VIN_3V3	O, 3.3V Power	Supply Voltage.
107	SD0_DATA0(PS_MIO42_501)	IO, 3.3V LVCMOS	SD0 Data0. This pin is connected to Micro SD connector.
108	SD0_CMD(PS_MIO41_501)	IO, 3.3V LVCMOS	SD0 command. This pin is connected to Micro SD connector.
109	SD0_CLK(PS_MIO40_501)	I, 3.3V LVCMOS	SD0 clock. This pin is connected to Micro SD connector.
110	PL_IO_L24N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 8th pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to E16th pin of FMC connector (J1) through resistor and default not populated.*
111	SD0_DATA1(PS_MIO43_501)	IO, 3.3V LVCMOS	SD0 Data1. This pin is connected to Micro SD connector
112	SD0_DATA2(PS_MIO44_501)	IO, 3.3V LVCMOS	SD0 Data2. This pin is connected to Micro SD connector
113	GND	Power	Ground.
114	SD0_DATA3(PS_MIO45_501)	IO, 3.3V LVCMOS	SD0 Data3. This pin is connected to Micro SD connector
115	I2C0_SDA(PS_MIO47_501)	IO, 3.3V OD	I2C0 data. This pin is connected to C31st pin of FMC connector (J1).
116	I2C0_SCL(PS_MIO46_501)	I, 3.3V OD	I2C0 clock. This pin is connected to C30th pin of FMC connector (J1).
117	UART0_RX(PS_MIO50_501)	O, 3.3V LVCMOS/ 10K PU	Debug UART0 Receive data line. This pin is connected from Serial to USB converter.
118	UART0_TX(PS_MIO51_501)	I, 3.3V LVCMOS	Debug UART0 Transmit data line. This pin is connected to Serial to USB converter.
119	PL_IO_L14N_T2_SRCC_34	IO, 3.3V LVCMOS	Bank34 Clock user Single region negative Single ended pin. This pin is connected to D21st pin of FMC connector (J1).
120	PL_IO_L15N_T2_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G19th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
121	PL_IO_L14P_T2_SRCC_34	IO, 3.3V LVCMOS	Bank34 Clock user Single region positive Single ended pin. This pin is connected to D20th pin of FMC connector (J1).
122	PL_IO_L15P_T2_DQS_34	O, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to G18th pin of FMC connector (J1).
123	PL_IO_L3N_T0_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected to 10th pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to F17th pin of FMC connector (J1) through resistor and default not populated.*
124	VIN_3V3	O, 3.3V Power	Supply Voltage.
125	PL_IO_L23P_T3_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G36th pin of FMC connector (J1).
126	PL_IO_L21P_T3_DQS_AD14P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H25th pin of FMC connector (J1).
127	NC	NA	NC.
128	NC	NA	NC.
129	NC	NA	NC.
130	NC	NA	NC.
131	GND	Power	Ground.
132	PL_IO_L22N_T3_AD7N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H33rd pin of FMC connector (J1).
133	PL_IO_L23N_T3_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G37th pin of FMC connector (J1).
134	PL_IO_L20P_T3_AD6P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H34th pin of FMC connector (J1).
135	NC	NA	NC.
136	PL_IO_L12P_T1_MRCC_35	O, 3.3V LVCMOS	Bank35 Clock user Single region positive Single ended pin. This pin is connected to J2nd pin of FMC connector (J1).
137	NC	NA	NC.
138	PL_IO_L22P_T3_AD7P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H22nd pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
139	PL_IO_L24P_T3_AD15P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G33rd pin of FMC connector (J1).
140	PL_IO_L21N_T3_DQS_AD14N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H26th pin of FMC connector (J1).
141	NC	NA	NC.
142	VIN_3V3	O, 3.3V Power	Supply Voltage.
143	PL_IO_L8N_T1_AD10N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to D27th pin of FMC connector (J1).
144	PL_IO_L11N_T1_SRCC_35	O, 3.3V LVCMOS	Bank35 Clock user Single region negative Single ended pin. This pin is connected to K5th pin of FMC connector (J1).
145	PL_IO_L8P_T1_AD10P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to D26th pin of FMC connector (J1).
146	PL_IO_L7P_T1_AD2P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to J12th pin of FMC connector (J1).
147	PL_IO_L7N_T1_AD2N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to J13th pin of FMC connector (J1).
148	PL_IO_L9P_T1_DQS_AD3P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G24th pin of FMC connector (J1).
149	PL_IO_L9N_T1_DQS_AD3N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G25th pin of FMC connector (J1).
150	PL_IO_L11P_T1_SRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to K4th pin of FMC connector (J1).
151	GND	Power	Ground.
152	PL_IO_L14P_T2_AD4P_SRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to D8th pin of FMC connector (J1).
153	PL_IO_L10N_T1_AD11N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G7th pin of FMC connector (J1).
154	PL_IO_L10P_T1_AD11P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G6th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
155	PL_IO_L6N_T0_VREF_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 3rd pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to K20th pin of FMC connector (J1) through resistor and default not populated.*
156	PL_IO_L16P_T2_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 3rd pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to E15th pin of FMC connector (J1) through resistor and default not populated.*
157	PL_IO_25_35	IO, 3.3V LVCMOS/ 10K PU	Bank35 User I/O Single ended pin. This pin is used to indicate the USB over current condition from USB power switch. *Note: Optionally this pin is connected to H2nd pin of FMC connector (J1) through resistor and default not populated.*
158	PL_IO_L12N_T1_MRCC_35	O, 3.3V LVCMOS	Bank35 Clock user Multi region negative Single ended pin. This pin is connected to J3rd pin of FMC connector (J1).
159	PL_IO_L14N_T2_AD4N_SRCC_35	O, 3.3V LVCMOS	Bank35 Clock user Single region negative Single ended pin. This pin is connected to D9th pin of FMC connector (J1).
160	VIN_3V3	O, 3.3V Power	Supply Voltage.
161	PL_IO_L6P_T0_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 1st pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to J18th pin of FMC connector (J1) through resistor and default not populated.*
162	PL_IO_L17P_T2_AD5P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G27th pin of FMC connector (J1).
163	PL_IO_L24N_T3_AD15N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G34th pin of FMC connector (J1).
164	PL_IO_L17N_T2_AD5N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G28th pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
165	PL_IO_L18N_T2_AD13N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to C23rd pin of FMC connector (J1).
166	PL_IO_L20N_T3_AD6N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H35th pin of FMC connector (J1).
167	PL_IO_L19P_T3_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 7th pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to E12th pin of FMC connector (J1) through resistor and default not populated.*
168	PL_IO_L16N_T2_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 4th pin of Pmod connector2 (J5). *Note: Optionally this pin is connected to F20th pin of FMC connector (J1) through resistor and default not populated.*
169	GND	Power	Ground.
170	PL_IO_L15P_T2_DQS_AD12P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H28th pin of FMC connector (J1).
171	PL_IO_L18P_T2_AD13P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to C22nd pin of FMC connector (J1).
172	PL_IO_L15N_T2_DQS_AD12N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H29th pin of FMC connector (J1).
173	PL_IO_L19N_T3_VREF_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to 8th pin of Pmod connector1 (J3). *Note: Optionally this pin is connected to F14th pin of FMC connector (J1) through resistor and default not populated.*
174	PL_IO_L1P_T0_AD0P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to C26th pin of FMC connector (J1).
175	PL_IO_L5P_T0_AD9P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H37th pin of FMC connector (J1).
176	PL_IO_L4P_T0_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to D23rd pin of FMC connector (J1).

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
177	PL_IO_L3N_T0_DQS_AD1N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G31st pin of FMC connector (J1).
178	PL_IO_L4N_T0_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to D24th pin of FMC connector (J1).
179	PL_IO_L5N_T0_AD9N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to H38th pin of FMC connector (J1).
180	VIN_3V3	O, 3.3V Power	Supply Voltage.
181	PL_IO_L3P_T0_DQS_AD1P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to G30th pin of FMC connector (J1).
182	PMIC_CTL_GPIO3	IO, 3.3V LVCMOS	NC from SOM. This pin is connected from 1st bit of SW2 DIP switch.
183	VRTC_3V0	O, 3V Power	3V backup coin cell input for RTC.
184	PMIC_CTL_GPIO4	IO, 3.3V LVCMOS	JTAG Boot Mode 0 This pin is connected from 2nd bit of SW2 DIP switch. *Note: Make sure that 2nd bit of SW2 Dip switch position in OFF state.*
185	GND	Power	Ground.
186	GND	Power	Ground.
187	PS_SRST_B_501	O, 3.3V CMOS	Active low reset button input. This pin is connected from Reset push Button (SW1).
188	NC	NA	NC.
189	PL_IO_L1N_T0_AD0N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected to C27th pin of FMC connector (J1).
190	PL_IO_L2N_T0_AD8N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from H32nd pin of FMC connector (J1).
191	JTAG_TDO	I, 3.3V CMOS	JTAG Test Data Output. This pin is connected from D30th pin of FMC connector (J1) and 8th pin of JTAG connector (J8).
192	VIN_3V3	O, 3.3V Power	Supply Voltage.
193	NC	NA	NC.
194	NC	NA	Default NC. *Note: Optionally this pin is connected to carrier board power enable circuit through resistor and default not populated.*

Pin No.	SODIMM Edge Connector Pin Name	Signal Type/ Termination	Description
195	JTAG_TDI	O, 3.3V CMOS	JTAG Test Data Input. This pin is connected to 10th pin of JTAG connector (J8).
196	PL_IO_L2P_T0_AD8P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from H31st pin of FMC connector (J1).
197	JTAG_TCK	O, 3.3V CMOS	JTAG Test Clock. This pin is connected from D29th pin of FMC connector (J1) and 6th pin of JTAG connector (J8).
198	GND	Power	Ground.
199	JTAG_TMS	O, 3.3V CMOS	JTAG Test Mode Select. This pin is connected from D33rd pin of FMC connector (J1) and 4th pin of JTAG connector (J8).
200	VBUS_USB	O, 5V Power	VUSB connected to USB OTG VBUS pin to support the USB OTG host. *Note: Recommending to connect always available 5V to this pin from carrier board to maintain compatibility with iWave's other SODIMM SOMs.*

2.4 Serial Interface Features

2.4.1 Debug UART

The Zynq SODIMM Carrier Board supports debug interface through Zynq 7000 CPU's UART0 interface. This UART0 signals from SODIMM Edge connector is connected to UART to USB Convertor "FT232RQ-REEL" and to USB Micro AB Connector (J6). This USB Micro AB Connector can be used for Debug purpose which is is physically located at the top of the board as shown below.

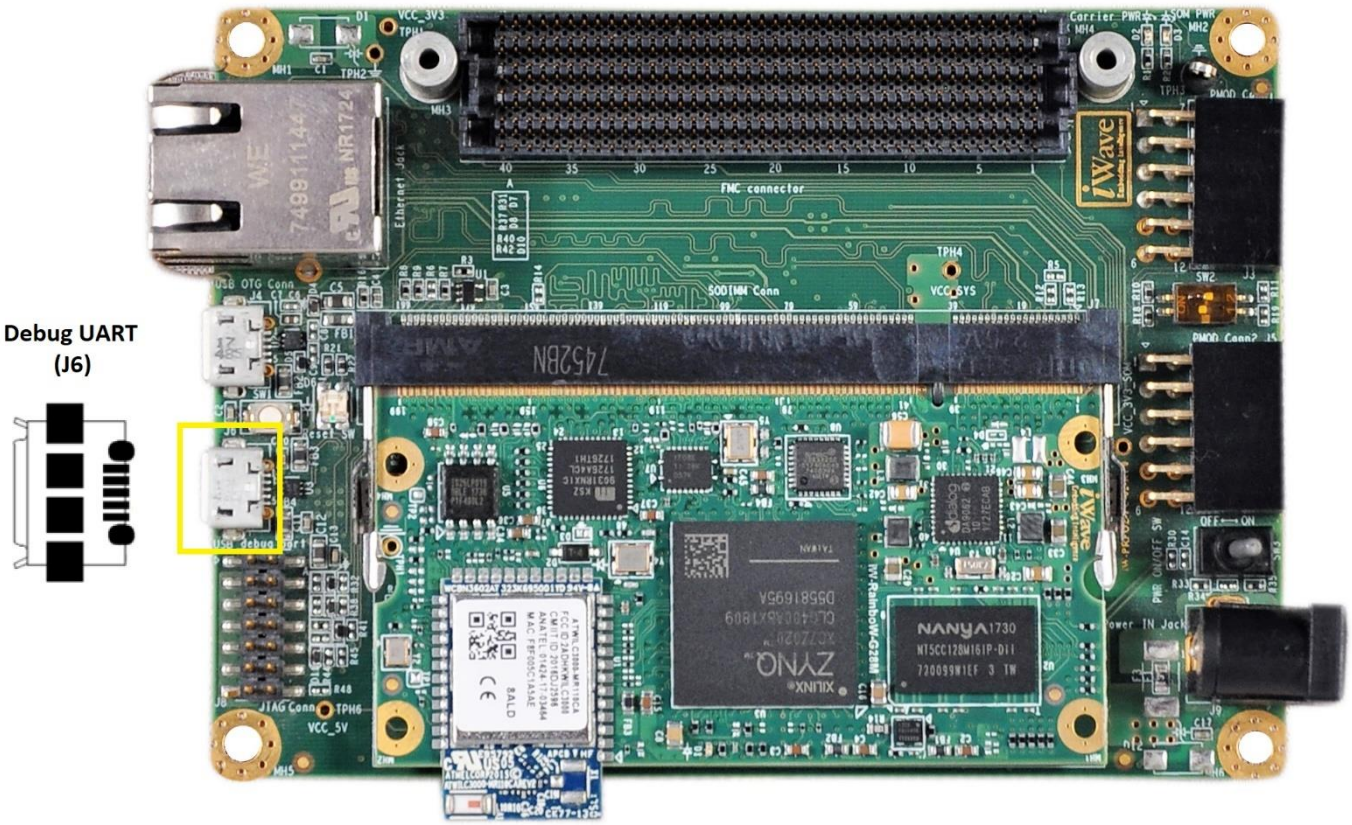

Figure 3: Debug UART

2.5 Communication Features

2.5.1 Gigabit Ethernet Port

The Zynq-7000 SoC SODIMM Carrier board supports 10/100/1000Mbps Ethernet interface through ENET0 interface of Zynq-7000 SoC PS. Ethernet PHY output signals from SODIMM Edge connector is directly connected to RJ45 Magjack (J2). The Ethernet supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack connector. This RJ45 Magjack connector is physically located at the top of the board as shown below.

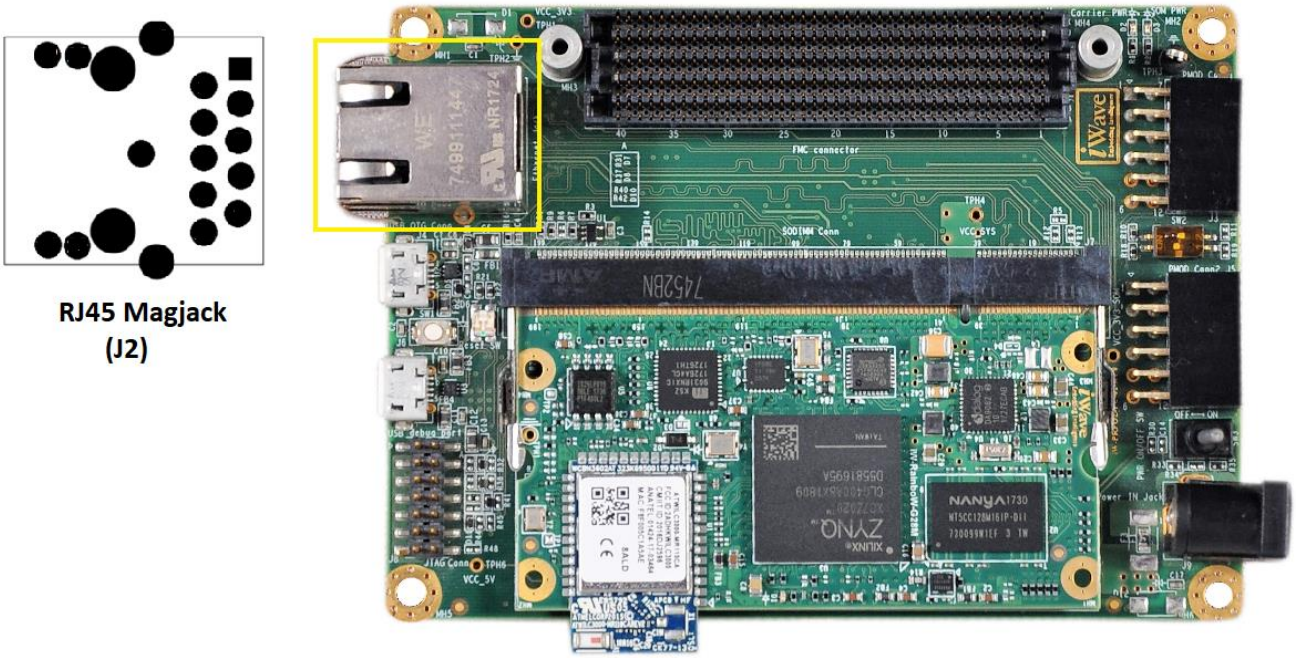

Figure 4: Gigabit Ethernet Connector

2.5.2 USB 2.0 OTG Port

The Zynq-7000 SoC SODIMM carrier Board supports USB2.0 High Speed OTG interface through USB OTG Controller of Zynq-7000 SoC PS. The Transceiver output signals from SODIMM Edge connector is directly connected to USB2.0 MicroAB connector. This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The transceiver detects the USB functionality through USB ID pin and controls the power using the USB_PWR_EN pin (78th pin) of SODIMM Connector. In Host mode, USB_PWR_EN should drive high to enable the power to the connector and in device mode, USB_PWR_EN should drive low to disable the power to the connector. This USB2.0 OTG connector (J4) is physically located at the top of the board as shown below.

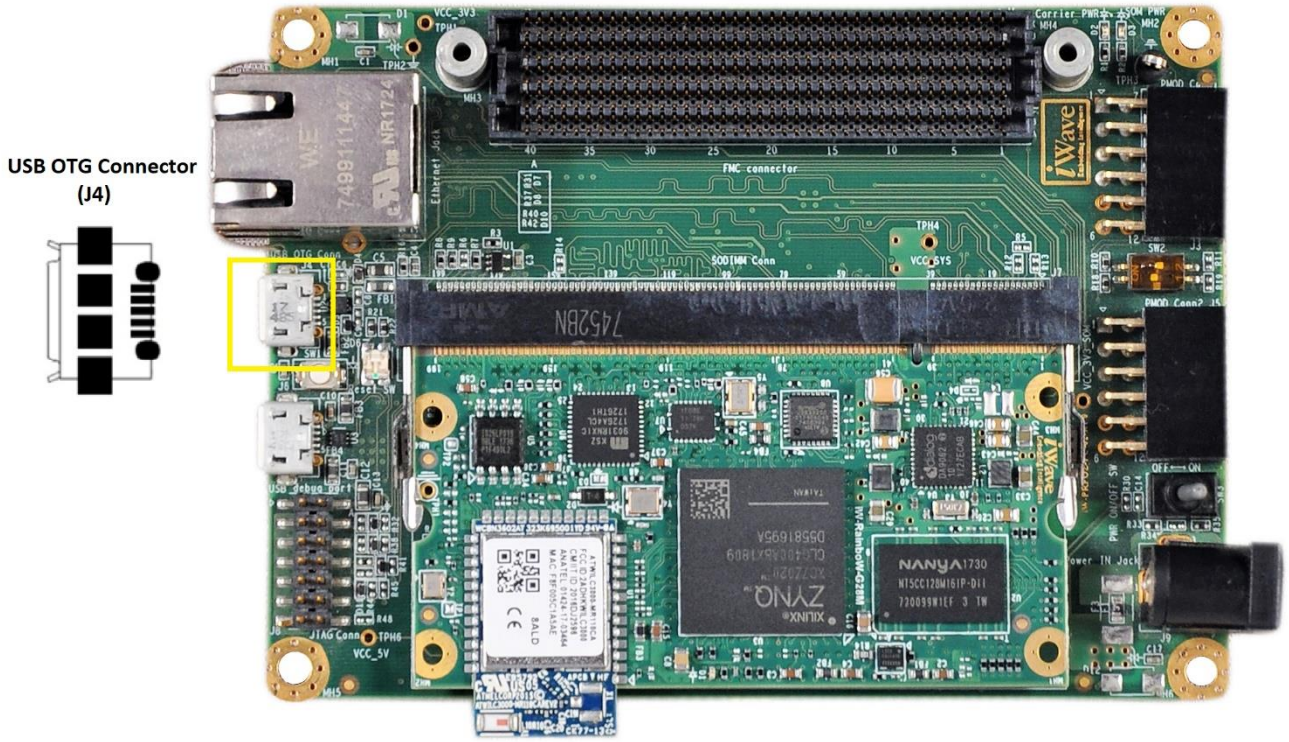

Figure 5: USB OTG Connector

2.5.3 MicroSD Port

The Zynq-7000 SoC SODIMM Carrier Board supports SDIO interface through SD0 interface of Zynq-7000 SoC PS. This SD0 signals from SODIMM Edge connector is connected to Micro SD connector (J11) to support Micro SD storage. The main power to Micro SD connector is 3.3V. This Micro SD connector (J11) is physically located at the bottom of the board as shown below.

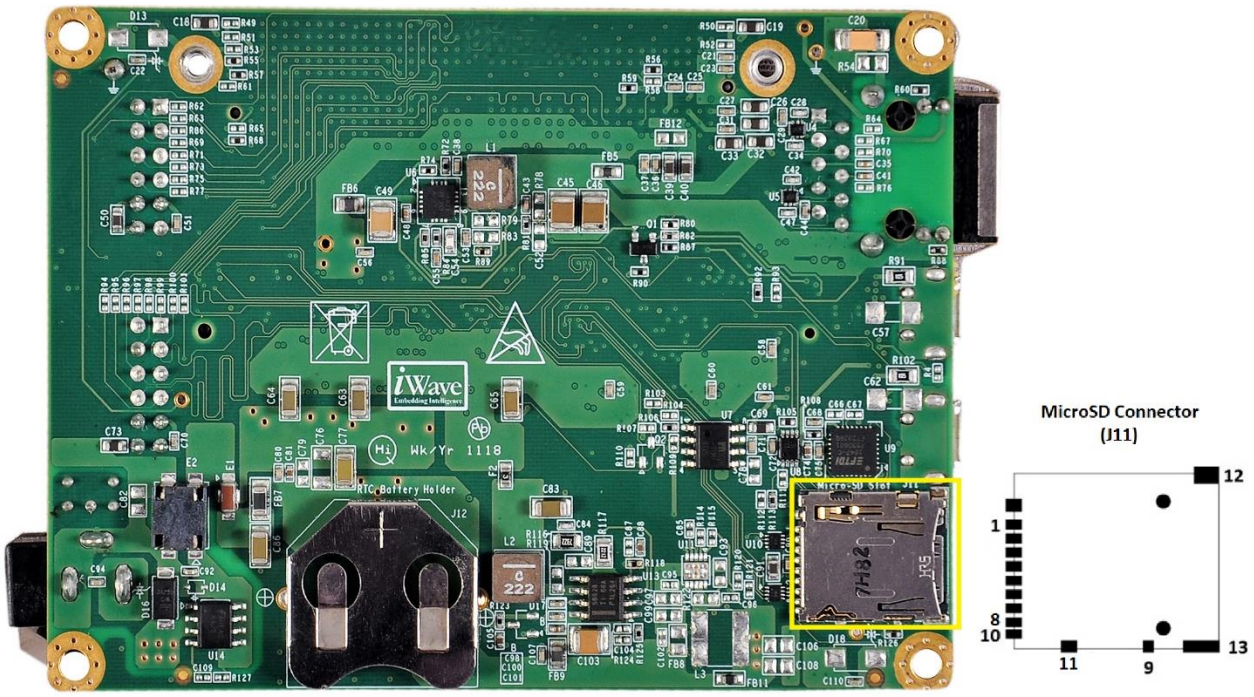

Figure 6: MicroSD Connector

Table 4: Micro SD Connector Pin Out

Pin No	Pin Name	Signal Type / Termination	Description
1	SD0_DATA2(PS_MIO44_501)	IO, 3.3V CMOS	SD Interface Data Line2.
2	SD0_DATA3(PS_MIO45_501)	IO, 3.3V CMOS	SD Interface Data Line3.
3	SD0_CMD(PS_MIO41_501)	IO, 3.3V CMOS	SD Interface Command Line.
4	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	SD0_CLK(PS_MIO40_501)	O,3.3V CMOS	SD Interface Clock.
6	VSS	Power	Ground.
7	SD0_DATA0(PS_MIO42_501)	IO, 3.3V CMOS	SD Interface Data Line0.
8	SD0_DATA1(PS_MIO43_501)	IO, 3.3V CMOS	SD Interface Data Line1.
9	SD0_CD(PS_MIO48_501)	I,3.3V CMOS	SD Interface Card Detect.
10	GND	Power	Ground.
11	GND	Power	Ground.
12	GND	Power	Ground.
13	GND	Power	Ground.

2.6 Expasnion Connectors

2.6.1 FMC Connector

The Zynq-7000 SoC SODIMM carrier board supports one 400Pin Standard FMC HPC connector for FPGA IOs expansion. This 400Pin FMC HPC connector is physically located at the top of the board as shown below.

This FMC connector supports 98 Single Ended (SE) IOs/30 LVDS IOs from Zynq-7000 SoC PL Banks.

- Upto 38 Single Ended (SE) IOs/19LVDS IOs from PL Bank34
    - Upto three clock capable SE IOs/ LVDS IOs (one MRCC and two SRCC)
- Upto 40 Single Ended (SE) IOs from PL Bank35
    - Upto three clock capable SE IOs/ LVDS IOs (one MRCC and two SRCC)
- Upto 22 Single Ended (SE)/11 LVDS IOs from PL Bank13
    - Upto four clock capable SE IOs (two MRCC and two SRCC)

Note: In Zynq-7000 SoC, PL BANK13 is not available in Z-7007S and Z-7010 devices and so BANK13 IOs (20 SE IOs) on FMC connector is NC in Z-7007S and Z-7010 SoC based SODIMM DevKit.

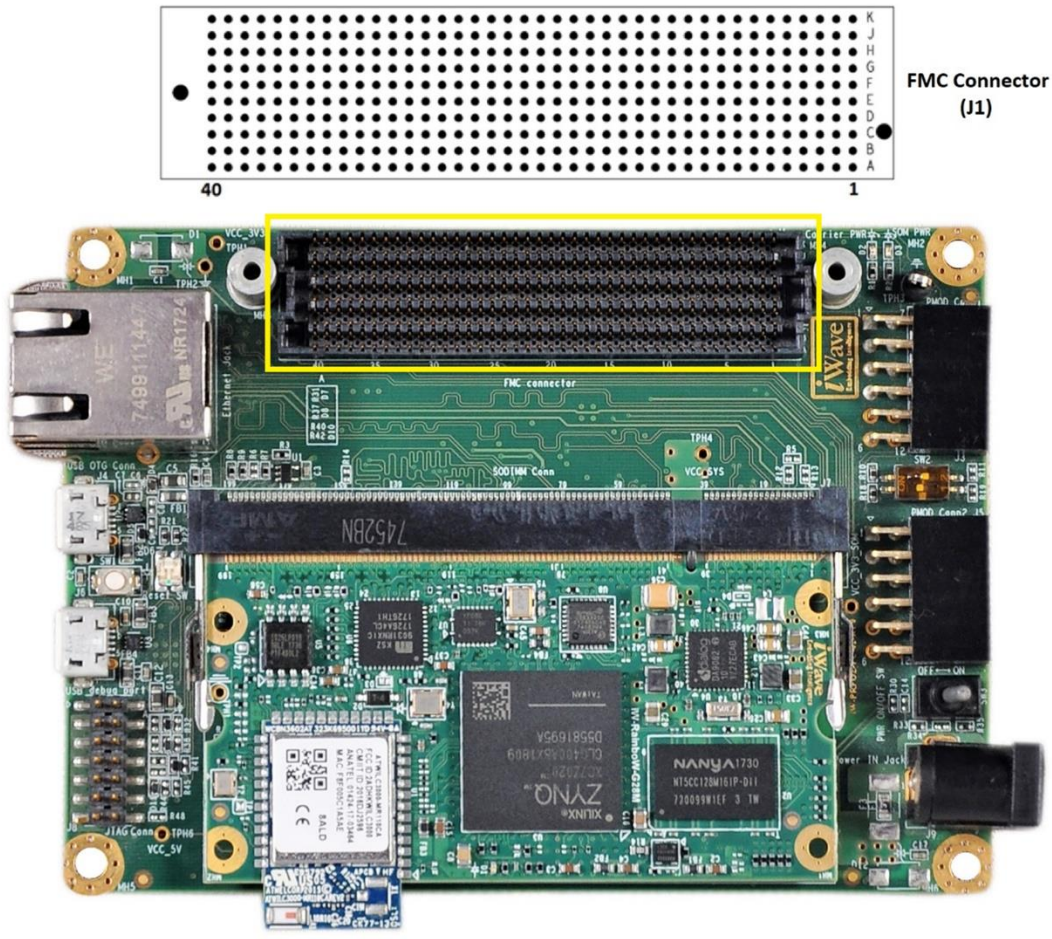

Figure 7: FMC HPC Connector

	K	J	H	G	F	E	D	C	B	A
1	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	NC	GND
2	GND	CLK1_C2M_P	PRSNT_M2C_L	CLK0_C2M_P	GND	HA01_P_CC	GND	NC	GND	NC
3	GND	CLK1_C2M_N	GND	CLK0_C2M_N	GND	HA01_P_CC	GND	NC	GND	NC
4	CLK1_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	NC	GND	NC	GND
5	CLK1_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	NC	GND	NC	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	NC	GND	NC
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	NC	GND	NC
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	NC	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	NC	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	NC
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	NC
12	GND	HA11_P	GND	LA08_P	GND	NC	LA05_N	GND	NC	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	NC	NC	GND	GND	NC	GND
14	HA10_N	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	NC
15	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	NC
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	NC	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	NC	GND
18	GND	NC	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	NC
19	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	NC
20	NC	GND	LA15_N	GND	NC	GND	LA17_P_CC	GND	NC	GND
21	GND	NC	GND	LA20_P	GND	NC	LA17_N_CC	GND	NC	GND
22	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	NC
23	NC	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	NC
24	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	NC	GND
25	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	NC	GND
26	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	NC
27	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	NC
28	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	NC	GND
29	NC	GND	LA24_N	GND	NC	GND	TCK	GND	NC	GND
30	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	NC
31	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	GND	NC
32	NC	GND	LA28_N	GND	NC	GND	3P3VAUX	GND	NC	GND
33	GND	NC	GND	LA31_P	GND	NC	TMS	GND	NC	GND
34	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	NC	GND	NC
35	NC	GND	LA30_N	GND	NC	GND	NC	NC	GND	NC
36	GND	NC	GND	LA33_P	GND	NC	3P3V	GND	NC	GND
37	NC	NC	LA32_P	LA33_N	NC	NC	GND	NC	NC	GND
38	NC	GND	LA32_N	GND	NC	GND	3P3V	GND	GND	NC
39	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC
40	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	NC	GND

Figure 8: FMC HPC Connector Pin Out

Table 5: FMC HPC Connector Pin Out

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	DP1_M2C_P	NA	NA	NC.
A3	DP1_M2C_N	NA	NA	NC.
A4	GND	GND	Power	Ground.
A5	GND	GND	Power	Ground.
A6	DP2_M2C_P	NA	NA	NC.
A7	DP2_M2C_N	NA	NA	NC.
A8	GND	GND	Power	Ground.
A9	GND	GND	Power	Ground.
A10	DP3_M2C_P	NA	NA	NC.
A11	DP3_M2C_N	NA	NA	NC.
A12	GND	GND	Power	Ground.
A13	GND	GND	Power	Ground.
A14	DP4_M2C_P	NA	NA	NC.
A15	DP4_M2C_N	NA	NA	NC.
A16	GND	GND	Power	Ground.
A17	GND	GND	Power	Ground.
A18	DP5_M2C_P	NA	NA	NC.
A19	DP5_M2C_N	NA	NA	NC.
A20	GND	GND	Power	Ground.
A21	GND	GND	Power	Ground.
A22	DP1_C2M_P	NA	NA	NC.
A23	DP1_C2M_N	NA	NA	NC.
A24	GND	GND	Power	Ground.
A25	GND	GND	Power	Ground.
A26	DP2_C2M_P	NA	NA	NC.
A27	DP2_C2M_N	NA	NA	NC.
A28	GND	GND	Power	Ground.
A29	GND	GND	Power	Ground.
A30	DP3_C2M_P	NA	NA	NC.
A31	DP3_C2M_N	NA	NA	NC.
A32	GND	GND	Power	Ground.
A33	GND	GND	Power	Ground.
A34	DP4_C2M_P	NA	NA	NC.
A35	DP4_C2M_N	NA	NA	NC.
A36	GND	GND	Power	Ground.
A37	GND	GND	Power	Ground.
A38	DP5_C2M_P	NA	NA	NC.
A39	DP5_C2M_N	NA	NA	NC.
A40	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
B1	RES1	NA	NA	NC.
B2	GND	GND	Power	Ground.
B3	GND	GND	Power	Ground.
B4	DP9_M2C_P	NA	NA	NC.
B5	DP9_M2C_N	NA	NA	NC.
B6	GND	GND	Power	Ground.
B7	GND	GND	Power	Ground.
B8	DP8_M2C_P	NA	NA	NC.
B9	DP8_M2C_N	NA	NA	NC.
B10	GND	GND	Power	Ground.
B11	GND	GND	Power	Ground.
B12	DP7_M2C_P	NA	NA	NC.
B13	DP7_M2C_N	NA	NA	NC.
B14	GND	GND	Power	Ground.
B15	GND	GND	Power	Ground.
B16	DP6_M2C_P	NA	NA	NC.
B17	DP6_M2C_N	NA	NA	NC.
B18	GND	GND	Power	Ground.
B19	GND	GND	Power	Ground.
B20	GBTCLK1_M2C_P	NA	NA	NC.
B21	GBTCLK1_M2C_N	NA	NA	NC.
B22	GND	GND	Power	Ground.
B23	GND	GND	Power	Ground.
B24	DP9_C2M_P	NA	NA	NC.
B25	DP9_C2M_N	NA	NA	NC.
B26	GND	GND	Power	Ground.
B27	GND	GND	Power	Ground.
B28	DP8_C2M_P	NA	NA	NC.
B29	DP8_C2M_N	NA	NA	NC.
B30	GND	GND	Power	Ground.
B31	GND	GND	Power	Ground.
B32	DP7_C2M_P	NA	NA	NC.
B33	DP7_C2M_N	NA	NA	NC.
B34	GND	GND	Power	Ground.
B35	GND	GND	Power	Ground.
B36	DP6_C2M_P	NA	NA	NC.
B37	DP6_C2M_N	NA	NA	NC.
B38	GND	GND	Power	Ground.
B39	GND	GND	Power	Ground.
B40	RES0	NA	NA	NC.
C1	GND	GND	Power	Ground.
C2	DP0_C2M_P	NA	NA	NC.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
C3	DP0_C2M_N	NA	NA	NC.
C4	GND	GND	Power	Ground.
C5	GND	GND	Power	Ground.
C6	DP0_M2C_P	NA	NA	NC.
C7	DP0_M2C_N	NA	NA	NC.
C8	GND	GND	Power	Ground.
C9	GND	GND	Power	Ground.
C10	LA06_P	PL_IO_L7P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 68th pin of SODIMM Connector (J7).
C11	LA06_N	PL_IO_L7N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 66th pin of SODIMM Connector (J7).
C12	GND	GND	Power	Ground.
C13	GND	GND	Power	Ground.
C14	LA10_P	PL_IO_L17P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 70th pin of SODIMM Connector (J7).
C15	LA10_N	PL_IO_L17N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 74th pin of SODIMM Connector (J7).
C16	GND	GND	Power	Ground.
C17	GND	GND	Power	Ground.
C18	LA14_P	PL_IO_L23P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 45th pin of SODIMM Connector (J7).
C19	LA14_N	PL_IO_L23N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 43rd pin of SODIMM Connector (J7).
C20	GND	GND	Power	Ground.
C21	GND	GND	Power	Ground.
C22	LA18_P_CC	PL_IO_L18P_T2_AD13P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 171st pin of SODIMM Connector (J7).
C23	LA18_N_CC	PL_IO_L18N_T2_AD13N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 165th pin of SODIMM Connector (J7).
C24	GND	GND	Power	Ground.
C25	GND	GND	Power	Ground.
C26	LA27_P	PL_IO_L1P_T0_AD0P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin This pin is connected from 174th pin of SODIMM Connector (J7).

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
C27	LA27_N	PL_IO_L1N_T0_AD0N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin This pin is connected from 189th pin of SODIMM Connector (J7).
C28	GND	GND	Power	Ground.
C29	GND	GND	Power	Ground.
C30	SCL	B_I2C0_SCL(PS_MIO46_501)	IO, 3.3V LVCMOS	HPC FMC I2C Clock Signal. This pin is connected from 116th pin of SODIMM Connector (J7).
C31	SDA	B_I2C0_SDA(PS_MIO47_501)	IO, 3.3V LVCMOS	HPC FMC I2C Data Signal. This pin is connected from 115th pin of SODIMM Connector (J7).
C32	GND	GND	Power	Ground.
C33	GND	GND	Power	Ground.
C34	GA0	-	10K PU	-
C35	12P0V	NC	NA	Default NC. *Note: Optionally 12V output can be supplied to this pin by changing the board assembly configuration. Please contact iWave for more information.*
C36	GND	GND	Power	Ground.
C37	12P0V	NC	NA	Default NC. *Note: Optionally 12V output can be supplied to this pin by changing the board assembly configuration. Please contact iWave for more information.*
C38	GND	GND	Power	Ground.
C39	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
C40	GND	GND	Power	Ground.
D1	PG_C2M	PG_C2M	I, 3.3V/ 10K PU	Power Good Signal from Carrier to FMC Module.
D2	GND	GND	Power	Ground.
D3	GND	GND	Power	Ground.
D4	NC	NA	NA	NC.
D5	NC	NA	NA	NC.
D6	GND	GND	Power	Ground.
D7	GND	GND	Power	Ground.
D8	LA01_P_CC	E_PL_IO_L14P_T2_AD4P_SRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 152nd pin of SODIMM Connector (J7).
D9	LA01_N_CC	E_PL_IO_L14N_T2_AD4N_SRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 159th pin of SODIMM Connector (J7).

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
D10	GND	GND	Power	Ground.
D11	LA05_P	PL_IO_L5P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 97th pin of SODIMM Connector (J7).
D12	LA05_N	PL_IO_L5N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 99th pin of SODIMM Connector (J7).
D13	GND	GND	Power	Ground.
D14	LA09_P	PL_IO_L16P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 102nd pin of SODIMM Connector (J7).
D15	LA09_N	PL_IO_L16N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 104th pin of SODIMM Connector (J7).
D16	GND	GND	Power	Ground.
D17	LA13_P	PL_IO_L22P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 94th pin of SODIMM Connector (J7).
D18	LA13_N	PL_IO_L22N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 96th pin of SODIMM Connector (J7).
D19	GND	GND	Power	Ground.
D20	LA17_P_CC	PL_IO_L14P_T2_SRCC_34	I, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 121st pin of SODIMM Connector (J7).
D21	LA17_N_CC	PL_IO_L14N_T2_SRCC_34	I, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 119th pin of SODIMM Connector (J7).
D22	GND	GND	Power	Ground.
D23	LA23_P	PL_IO_L4P_T0_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 176th pin of SODIMM Connector (J7).
D24	LA23_N	PL_IO_L4N_T0_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 178th pin of SODIMM Connector (J7).
D25	GND	GND	Power	Ground.
D26	LA26_P	E_PL_IO_L8P_T1_AD10P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 145th pin of SODIMM Connector (J7).
D27	LA26_N	E_PL_IO_L8N_T1_AD10N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 143rd pin of SODIMM Connector (J7).
D28	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
D29	TCK	JTAG_TCK	O, 3.3V LVCMOS	JTAG Test Clock.
D30	TDI	JTAG_TDI	I, 3.3V LVCMOS	JTAG Test Data Input
D31	TDO	JTAG_TDO	O, 3.3V LVCMOS	JTAG Test Data Output
D32	3P3VAUX	VCC_3V3	O, 3.3V Power	Auxiliary Supply Voltage
D33	TMS	JTAG_TMS	O, 3.3V LVCMOS	JTAG Test Mode Select
D34	TRST_L	NA	NA	NC.
D35	GA1	-	10K, PD	-
D36	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D37	GND	GND	Power	Ground.
D38	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
D39	GND	GND	Power	Ground.
D40	3P3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
E1	GND	GND	Power	Ground.
E2	HA01_P_CC	PL_IO_L12P_T1_MRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 26th pin of SODIMM Connector (J7).
E3	HA01_N_CC	PL_IO_L12N_T1_MRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 28th pin of SODIMM Connector (J7).
E4	GND	GND	Power	Ground.
E5	GND	GND	Power	Ground.
E6	HA05_P	PL_IO_L15P_T2_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 22nd pin of SODIMM Connector (J7).
E7	HA05_N	PL_IO_L15N_T2_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 24th pin of SODIMM Connector (J7).
E8	GND	GND	Power	Ground.
E9	HA09_P	PL_IO_L14P_T2_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 55th pin of SODIMM Connector (J7).
E10	HA09_N	PL_IO_L14N_T2_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 53rd pin of SODIMM Connector (J7).
E11	GND	GND	Power	Ground.
E12	HA13_P	NA	NA	NC. *Note: Optionally this pin is connected from 167th pin of SODIMM Connector (J7) through resistor and default not populated.*

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
E13	HA13_N	NA	NA	NC. *Note: Optionally this pin is connected from 7th pin of SODIMM Connector (J7) through resistor and default not populated.*
E14	GND	GND	Power	Ground.
E15	HA16_P	NA	NA	NC. *Note: Optionally this pin is connected from 156th pin of SODIMM Connector (J7) through resistor and default not populated.*
E16	HA16_N	NA	NA	NC. *Note: Optionally this pin is connected from 110th pin of SODIMM Connector (J7) through resistor and default not populated.*
E17	GND	GND	Power	Ground.
E18	HA20_P	NA	NA	NC.
E19	HA20_N	NA	NA	NC. *Note: Optionally this pin is connected from 10th pin of SODIMM Connector (J7) through resistor and default not populated.*
E20	GND	GND	Power	Ground.
E21	HB03_P	NA	NA	NC.
E22	HB03_N	NA	NA	NC.
E23	GND	GND	Power	Ground.
E24	HB05_P	NA	NA	NC.
E25	HB05_N	NA	NA	NC.
E26	GND	GND	Power	Ground.
E27	HB09_P	NA	NA	NC.
E28	HB09_N	NA	NA	NC.
E29	GND	GND	Power	Ground.
E30	HB13_P	NA	NA	NC.
E31	HB13_N	NA	NA	NC.
E32	GND	GND	Power	Ground.
E33	HB19_P	NA	NA	NC.
E34	HB19_N	NA	NA	NC.
E35	GND	GND	Power	Ground.
E36	HB21_P	NA	NA	NC.
E37	HB21_N	NA	NA	NC.
E38	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
E39	VADJ	VCC_3V3	O, 3.3V Power	FMC Adjustable Voltage.
E40	GND	GND	Power	Ground.
F1	PG_M2C	PG_M2C	O,3.3V/ 10K PU	Power Good Signal from FMC Module to Carrier.
F2	GND	GND	Power	Ground.
F3	GND	GND	Power	Ground.
F4	HA00_P_CC	PL_IO_L13P_T2_MRCC_13	I, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 54th pin of SODIMM Connector (J7).
F5	HA00_N_CC	PL_IO_L13N_T2_MRCC_13	I, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 52nd pin of SODIMM Connector (J7).
F6	GND	GND	Power	Ground.
F7	HA04_P	PL_IO_L17P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 50th pin of SODIMM Connector (J7).
F8	HA04_N	PL_IO_L17N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 48th pin of SODIMM Connector (J7).
F9	GND	GND	Power	Ground.
F10	HA08_P	PL_IO_L16P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 59th pin of SODIMM Connector (J7).
F11	HA08_N	PL_IO_L16N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 57th pin of SODIMM Connector (J7).
F12	GND	GND	Power	Ground.
F13	HA12_P	NA	NA	NC. *Note: Optionally this pin is connected from 73rd pin of SODIMM Connector (J7) through resistor and default not populated.*
F14	HA12_N	NA	NA	NC. *Note: Optionally this pin is connected from 173rd pin of SODIMM Connector (J7) through resistor and default not populated.*
F15	GND	GND	Power	Ground.
F16	HA15_P	NA	NA	NC. *Note: Optionally this pin is connected from 91st pin of SODIMM Connector (J7) through resistor and default not populated.*

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
F17	HA15_N	NA	NA	NC. *Note: Optionally this pin is connected from 123rd pin of SODIMM Connector (J7) through resistor and default not populated.*
F18	GND	GND	Power	Ground.
F19	HA19_P	NA	NA	NC.
F20	HA19_N	NA	NA	NC. *Note: Optionally this pin is connected from 168th pin of SODIMM Connector (J7) through resistor and default not populated.*
F21	GND	GND	Power	Ground.
F22	HB02_P	NA	NA	NC.
F23	HB02_N	NA	NA	NC.
F24	GND	GND	Power	Ground.
F25	HB04_P	NA	NA	NC.
F26	HB04_N	NA	NA	NC.
F27	GND	GND	Power	Ground.
F28	HB08_P	NA	NA	NC.
F29	HB08_N	NA	NA	NC.
F30	GND	GND	Power	Ground.
F31	HB12_P	NA	NA	NC.
F32	HB12_N	NA	NA	NC.
F33	GND	GND	Power	Ground.
F34	HB16_P	NA	NA	NC.
F35	HB16_N	NA	NA	NC.
F36	GND	GND	Power	Ground.
F37	HB20_P	NA	NA	NC.
F38	HB20_N	NA	NA	NC.
F39	GND	GND	Power	Ground.
F40	VADJ	VCC_3V3	O, 3.3V Power	FMC Adjustable Voltage.
G1	GND	GND	Power	Ground.
G2	CLK0_C2M_P	PL_IO_L11P_T1_SRCC_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 69th pin of SODIMM Connector (J7).
G3	CLK0_C2M_N	PL_IO_L11N_T1_SRCC_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 67th pin of SODIMM Connector (J7).
G4	GND	GND	Power	Ground.
G5	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
G6	LA00_P_CC	E_PL_IO_L10P_T1_AD11P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 154th pin of SODIMM Connector (J7).
G7	LA00_N_CC	E_PL_IO_L10N_T1_AD11N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 153rd pin of SODIMM Connector (J7).
G8	GND	GND	Power	Ground.
G9	LA03_P	PL_IO_L2P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 37th pin of SODIMM Connector (J7).
G10	LA03_N	PL_IO_L2N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 35th pin of SODIMM Connector (J7).
G11	GND	GND	Power	Ground.
G12	LA08_P	PL_IO_L10P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 39th pin of SODIMM Connector (J7).
G13	LA08_N	PL_IO_L10N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 38th pin of SODIMM Connector (J7).
G14	GND	GND	Power	Ground.
G15	LA12_P	PL_IO_L20P_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 101st pin of SODIMM Connector (J7).
G16	LA12_N	PL_IO_L20N_T3_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 103rd pin of SODIMM Connector (J7).
G17	GND	GND	Power	Ground.
G18	LA16_P	PL_IO_L15P_T2_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 122nd pin of SODIMM Connector (J7).
G19	LA16_N	PL_IO_L15N_T2_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 120th pin of SODIMM Connector (J7).
G20	GND	GND	Power	Ground.
G21	LA20_P	PL_IO_L21P_T3_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 98th pin of SODIMM Connector (J7).
G22	LA20_N	PL_IO_L21N_T3_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 100th pin of SODIMM Connector (J7).
G23	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
G24	LA22_P	E_PL_IO_L9P_T1_DQS_AD3P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 148th pin of SODIMM Connector (J7).
G25	LA22_N	E_PL_IO_L9N_T1_DQS_AD3N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 149th pin of SODIMM Connector (J7).
G26	GND	GND	Power	Ground.
G27	LA25_P	PL_IO_L17P_T2_AD5P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 162nd pin of SODIMM Connector (J7).
G28	LA25_N	PL_IO_L17N_T2_AD5N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 164th pin of SODIMM Connector (J7).
G29	GND	GND	Power	Ground.
G30	LA29_P	PL_IO_L3P_T0_DQS_AD1P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 181st pin of SODIMM Connector (J7).
G31	LA29_N	PL_IO_L3N_T0_DQS_AD1N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 177th pin of SODIMM Connector (J7).
G32	GND	GND	Power	Ground.
G33	LA31_P	PL_IO_L24P_T3_AD15P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 139th pin of SODIMM Connector (J7).
G34	LA31_N	PL_IO_L24N_T3_AD15N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 163rd pin of SODIMM Connector (J7).
G35	GND	GND	Power	Ground.
G36	LA33_P	PL_IO_L23P_T3_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 125th pin of SODIMM Connector (J7).
G37	LA33_N	PL_IO_L23N_T3_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 133rd pin of SODIMM Connector (J7).
G38	GND	GND	Power	Ground.
G39	VADJ	VCC_3V3	O, 3.3V Power	FMC Adjustable Voltage.
G40	GND	GND	Power	Ground.
H1	VREF_A_M2C	NA	NA	NC.
H2	PRSNT_M2C_L	PRSNT	I,3.3V/ 10K PU	Module Present Signal.
H3	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
H4	CLK0_M2C_P	PL_IO_L12P_T1_MRCC_34	I, 3.3V LVDS	Bank34 User I/O Single ended pin. This pin is connected from 90th pin of SODIMM Connector (J7).
H5	CLK0_M2C_N	PL_IO_L12N_T1_MRCC_34	I, 3.3V LVDS	Bank34 User I/O Single ended pin. This pin is connected from 92nd pin of SODIMM Connector (J7).
H6	GND	GND	Power	Ground.
H7	LA02_P	PL_IO_L1P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 36th pin of SODIMM Connector (J7).
H8	LA02_N	PL_IO_L1N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 34th pin of SODIMM Connector (J7).
H9	GND	GND	Power	Ground.
H10	LA04_P	PL_IO_L4P_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 64th pin of SODIMM Connector (J7).
H11	LA04_N	PL_IO_L4N_T0_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 62nd pin of SODIMM Connector (J7).
H12	GND	GND	Power	Ground.
H13	LA07_P	PL_IO_L8P_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 63rd pin of SODIMM Connector (J7).
H14	LA07_N	PL_IO_L8N_T1_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 61st pin of SODIMM Connector (J7).
H15	GND	GND	Power	Ground.
H16	LA11_P	PL_IO_L18P_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 44th pin of SODIMM Connector (J7).
H17	LA11_N	PL_IO_L18N_T2_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 42nd pin of SODIMM Connector (J7).
H18	GND	GND	Power	Ground.
H19	LA15_P	PL_IO_L9P_T1_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 86th pin of SODIMM Connector (J7).
H20	LA15_N	PL_IO_L9N_T1_DQS_34	IO, 3.3V LVCMOS	Bank34 User I/O Single ended pin. This pin is connected from 89th pin of SODIMM Connector (J7).
H21	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
H22	LA19_P	PL_IO_L22P_T3_AD7P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 138th pin of SODIMM Connector (J7).
H23	LA19_N	PL_IO_L22N_T3_AD7N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 132nd pin of SODIMM Connector (J7).
H24	GND	GND	Power	Ground.
H25	LA21_P	PL_IO_L21P_T3_DQS_AD14P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 126th pin of SODIMM Connector (J7).
H26	LA21_N	PL_IO_L21N_T3_DQS_AD14N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 140th pin of SODIMM Connector (J7).
H27	GND	GND	Power	Ground.
H28	LA24_P	PL_IO_L15P_T2_DQS_AD12P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 170th pin of SODIMM Connector (J7).
H29	LA24_N	PL_IO_L15N_T2_DQS_AD12N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 172nd pin of SODIMM Connector (J7).
H30	GND	GND	Power	Ground.
H31	LA28_P	PL_IO_L2P_T0_AD8P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 196th pin of SODIMM Connector (J7).
H32	LA28_N	PL_IO_L2N_T0_AD8N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 190th pin of SODIMM Connector (J7).
H33	GND	GND	Power	Ground.
H34	LA30_P	PL_IO_L20P_T3_AD6P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 134th pin of SODIMM Connector (J7).
H35	LA30_N	PL_IO_L20N_T3_AD6N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 166th pin of SODIMM Connector (J7).
H36	GND	GND	Power	Ground.
H37	LA32_P	PL_IO_L5P_T0_AD9P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 175th pin of SODIMM Connector (J7).
H38	LA32_N	PL_IO_L5N_T0_AD9N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 179th pin of SODIMM Connector (J7).
H39	GND	GND	Power	Ground.
H40	VADJ	VCC_3V3	O, 3.3V Power	FMC Adjustable Voltage.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
J1	GND	GND	Power	Ground.
J2	CLK1_C2M_P	PL_IO_L12P_T1_MRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 136th pin of SODIMM Connector (J7).
J3	CLK1_C2M_N	PL_IO_L12N_T1_MRCC_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 158th pin of SODIMM Connector (J7).
J4	GND	GND	Power	Ground.
J5	GND	GND	Power	Ground.
J6	HA03_P	PL_IO_L21P_T3_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 58th pin of SODIMM Connector (J7).
J7	HA03_N	PL_IO_L21N_T3_DQS_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 56th pin of SODIMM Connector (J7).
J8	GND	GND	Power	Ground.
J9	HA07_P	PL_IO_L18P_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 30th pin of SODIMM Connector (J7).
J10	HA07_N	PL_IO_L18N_T2_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 33rd pin of SODIMM Connector (J7).
J11	GND	GND	Power	Ground.
J12	HA11_P	E_PL_IO_L7P_T1_AD2P_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 146th pin of SODIMM Connector (J7).
J13	HA11_N	E_PL_IO_L7N_T1_AD2N_35	IO, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 147th pin of SODIMM Connector (J7).
J14	GND	GND	Power	Ground.
J15	HA14_P	NA	NA	NC. *Note: Optionally this pin is connected from 80th pin of SODIMM Connector (J7) through resistor and default not populated.*
J16	HA14_N	NA	NA	NC. *Note: Optionally this pin is connected from 47th pin of SODIMM Connector (J7) through resistor and default not populated.*
J17	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
J18	HA18_P	NA	NA	NC. *Note: Optionally this pin is connected from 161st pin of SODIMM Connector (J7) through resistor and default not populated.*
J19	HA18_N	NA	NA	NC. *Note: Optionally this pin is connected from 93rd pin of SODIMM Connector (J7) through resistor and default not populated.*
J20	GND	GND	Power	Ground.
J21	HA22_P	NA	NA	NC.
J22	HA22_N	NA	NA	NC.
J23	GND	GND	Power	Ground.
J24	HB01_P	NA	NA	NC.
J25	HB01_N	NA	NA	NC.
J26	GND	GND	Power	Ground.
J27	HB07_P	NA	NA	NC.
J28	HB07_N	NA	NA	NC.
J29	GND	GND	Power	Ground.
J30	HB11_P	NA	NA	NC.
J31	HB11_N	NA	NA	NC.
J32	GND	GND	Power	Ground.
J33	HB15_P	NA	NA	NC.
J34	HB15_N	NA	NA	NC.
J35	GND	GND	Power	Ground.
J36	HB18_P	NA	NA	NC.
J37	HB18_N	NA	NA	NC.
J38	GND	GND	Power	Ground.
J39	VIO_B_M2C	NA	NA	NC.
J40	GND	GND	Power	Ground.
K1	VREF_B_M2C	NA	NA	NC.
K2	GND	GND	Power	Ground.
K3	GND	GND	Power	Ground.
K4	CLK1_M2C_P	E_PL_IO_L11P_T1_SRCC_35	I, 3.3V LVCMOS	Bank35 Single ended Clock input pin. This pin is connected from 150th pin of SODIMM Connector (J7).
K5	CLK1_M2C_N	E_PL_IO_L11N_T1_SRCC_35	I, 3.3V LVCMOS	Bank35 User I/O Single ended pin. This pin is connected from 144th pin of SODIMM Connector (J7).
K6	GND	GND	Power	Ground.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
K7	HA02_P	PL_IO_L20P_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 29th pin of SODIMM Connector (J7).
K8	HA02_N	PL_IO_L20N_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 31st pin of SODIMM Connector (J7).
K9	GND	GND	Power	Ground.
K10	HA06_P	PL_IO_L22P_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 21st pin of SODIMM Connector (J7).
K11	HA06_N	PL_IO_L22N_T3_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 23rd pin of SODIMM Connector (J7).
K12	GND	GND	Power	Ground.
K13	HA10_P	PL_IO_L11P_T1_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 19th pin of SODIMM Connector (J7).
K14	HA10_N	PL_IO_L11N_T1_SRCC_13	IO, 3.3V LVCMOS	Bank13 User I/O Single ended pin. This pin is connected from 18th pin of SODIMM Connector (J7).
K15	GND	GND	Power	Ground.
K16	HA17_P_CC	NA	NA	NC. *Note: Optionally this pin is connected from 9th pin of SODIMM Connector (J7) through resistor and default not populated.*
K17	HA17_N_CC	NA	NA	NC. *Note: Optionally this pin is connected from 71st pin of SODIMM Connector (J7) through resistor and default not populated.*
K18	GND	GND	Power	Ground.
K19	HA21_P	NA	NA	NC.
K20	HA21_N	NA	NA	NC. *Note: Optionally this pin is connected from 155th pin of SODIMM Connector (J7) through resistor and default not populated.*
K21	GND	GND	Power	Ground.
K22	HA23_P	NA	NA	NC.
K23	HA23_N	NA	NA	NC.
K24	GND	GND	Power	Ground.
K25	HB00_P_CC	NA	NA	NC.

Pin No	FMC Connector Pin Name	Signal Name	Signal Type/ Termination	Description
K26	HB00_N_CC	NA	NA	NC.
K27	GND	GND	Power	Ground.
K28	HB06_P_CC	NA	NA	NC.
K29	HB06_N_CC	NA	NA	NC.
K30	GND	GND	Power	Ground.
K31	HB10_P	NA	NA	NC.
K32	HB10_N	NA	NA	NC.
K33	GND	GND	Power	Ground.
K34	HB14_P	NA	NA	NC.
K35	HB14_N	NA	NA	NC.
K36	GND	GND	Power	Ground.
K37	HB17_P_CC	NA	NA	NC.
K38	HB17_N_CC	NA	NA	NC.
K39	GND	GND	Power	Ground.
K40	VIO_B_M2C	NA	NA	NC.

2.6.2 Pmod Host Port Connectors

The Zynq-7000 SoC SODIMM Carrier board supports two 12pin Pmod host port connector for plugging Pmod modules. Pmod interface or Peripheral Module interface is a standard defined by Digilent Inc in the Digilent Pmod Interface Specification for peripherals used with FPGAs or microcontrollers.

Pmod provides multiple digital IO signals which can be configured as different standard serial protocols like SPI, UART, I2C etc. Pmod Host port conenctor1 (J3) and connector2 (J5) are physically located at the top of the board as shown below.

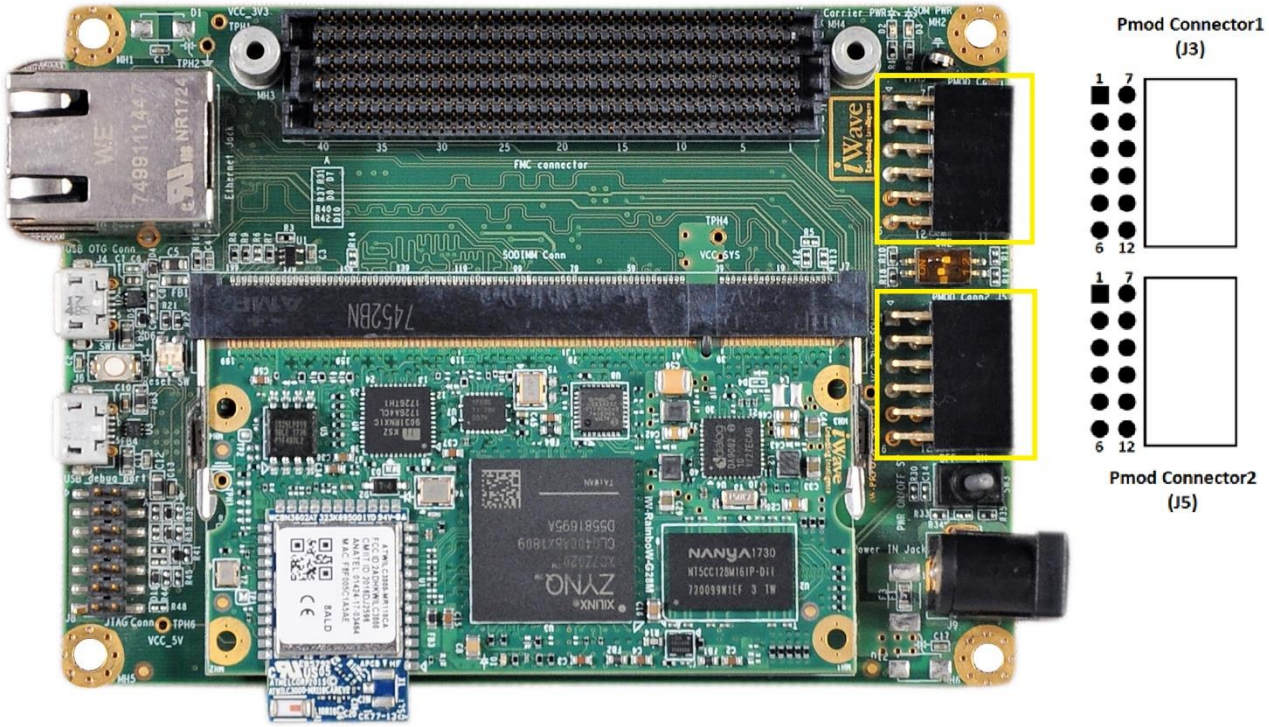

Figure 9: Pmod Host Port Connectors

Table 6: Pmod Connector1 Pin Out

Pin No	Signal Name	Signal Type/ Termination	Description
1	PL_IO_L6P_T0_35	IO, 3V3 LVCMOS	General purpose Input Output.
2	L_IO_L6N_T0_VREF_13	IO, 3V3 LVCMOS	General purpose Input Output.
3	PL_IO_L6N_T0_VREF_35	IO, 3V3 LVCMOS	General purpose Input Output.
4	PL_IO_L19N_T3_VREF_34	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	PL_IO_L19P_T3_35	IO, 3V3 LVCMOS	General purpose Input Output.
8	PL_IO_L19N_T3_VREF_35	IO, 3V3 LVCMOS	General purpose Input Output.
9	PL_IO_0_34	IO, 3V3 LVCMOS	General purpose Input Output.
10	PL_IO_L3N_T0_DQS_34	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

Note: If IO voltage of PL Bank34 and Bank35 is changed in Zynq-7000 SoC SODIMM SOM, then the IO voltage of corresponding PL Bank IOs in this Pmod connector1 will also change.

Note: In Zynq-7000 SoC, PL Bank13 is not available in Z-7007S & Z-7010 devices and so Bank13 IOs on Pmod Connector1 pin2 is NC in Z-7007S & Z-7010 SoC based SODIMM DevKit.

Table 7: Pmod Connector2 Pin Out

Pin No	Signal Name	Signal Type/ Termination	Description
1	PL_IO_L19P_T3_34	IO, 3V3 LVCMOS	General purpose Input Output.
2	PL_IO_L13N_T2_MRCC_34	IO, 3V3 LVCMOS	General purpose Input Output.
3	E_PL_IO_L16P_T2_35	IO, 3V3 LVCMOS	General purpose Input Output.
4	PL_IO_L16N_T2_35	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	PL_IO_25_34	IO, 3V3 LVCMOS	General purpose Input Output.
8	PL_IO_L24N_T3_34	IO, 3V3 LVCMOS	General purpose Input Output.
9	PL_IO_L6P_T0_34	IO, 3V3 LVCMOS	General purpose Input Output.
10	PL_IO_L6N_T0_VREF_34	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

Note: If IO voltage of PL Bank34 and Bank35 is changed in Zynq-7000 SoC SODIMM SOM, then the IO voltage of corresponding PL Bank IOs in this Pmod connector2 will also change.

2.7 Additional Features

2.7.1 JTAG Connector

A Standard Xilinx 14-pin JTAG Header is available in Zynq-7000 SoC SODIMM carrier board for debug purpose. JTAG signals from SODIMM connector is directly connected to JTAG Header (J8) and same JTAG signals are also connected to FMC connector. JTAG-HS2/ JTAG-HS3 programming cable can be plugged to this JTAG Header for programming and debugging purpose. This JTAG Header (J8) is physically located at the top of the board as shown below.

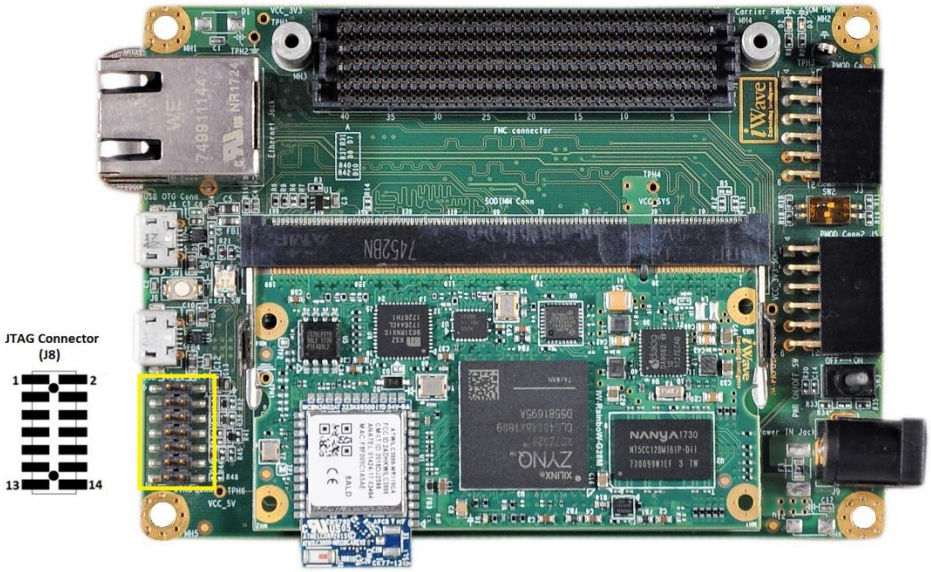

Figure 10: JTAG Connector

Table 8: JTAG Header Pin Out

Pin No	Signal Name	Signal Type/ Termination	Description
1	NC	-	Not Connected
2	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
3	GND	Power	Ground
4	JTAG_TMS	I, 3V3 CMOS	JTAG test mode select.
5	GND	Power	Ground
6	JTAG_TCK	I, 3V3 CMOS	JTAG test Clock
7	GND	Power	Ground
8	JTAG_TDO	O, 3V3 CMOS	JTAG test data output.
9	GND	Power	Ground
10	JTAG_TDI	I, 3V3 CMOS	JTAG test data input
11	GND	Power	Ground
12	NC	-	Not Connected
13	GND	Power	Ground
14	JTAG_TRSTB	-	Not connected from Zynq SOM

2.7.2 Power ON/OFF Switch

The Zynq-7000 SoC SODIMM carrier board has power ON/OFF switch (SW3) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

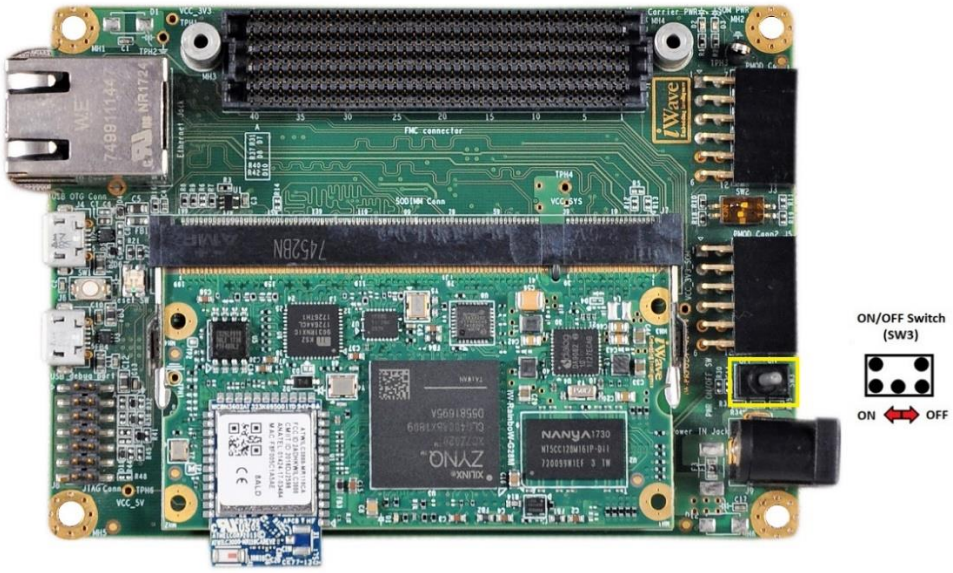

Figure 11: Power On/Off Switch

2.7.3 Reset Switch

The Zynq-7000 SoC SODIMM carrier board supports Push button switch (SW1) to reset the Zynq 7000 SoC CPU. Reset signal of SODIMM edge connector Pin 187 is directly connected from Reset Push button switch. This Reset Push button switch (SW1) is physically located at the top of the board as shown below.

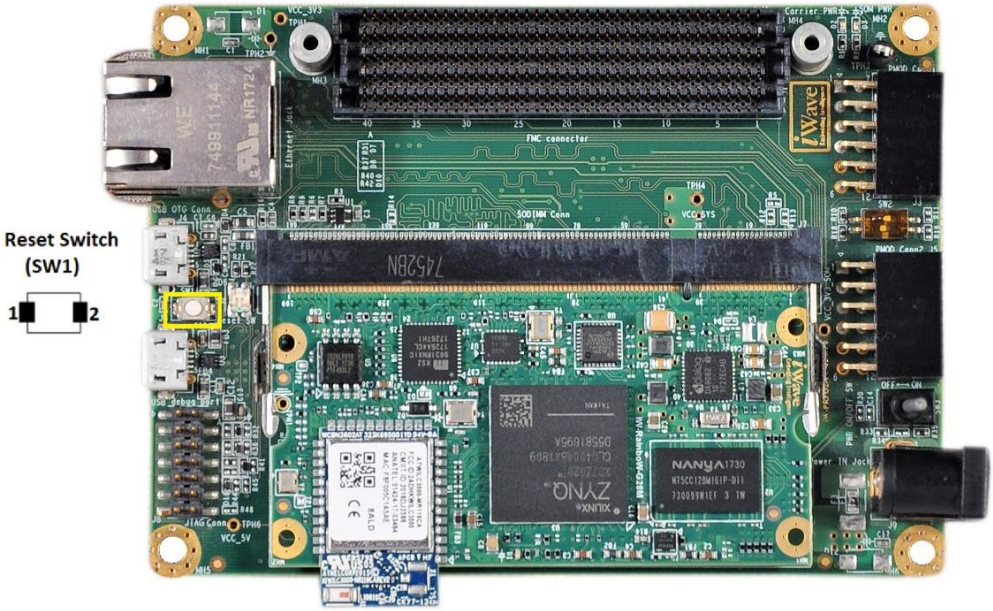

Figure 12: Reset Switch

2.7.4 DIP Switch

The Zynq-7000 SoC SODIMM carrier board has DIP switch (SW2) to access JTAG Boot Mode[0] functionality. This DIP switch is physically located at the top of the board as shown below.

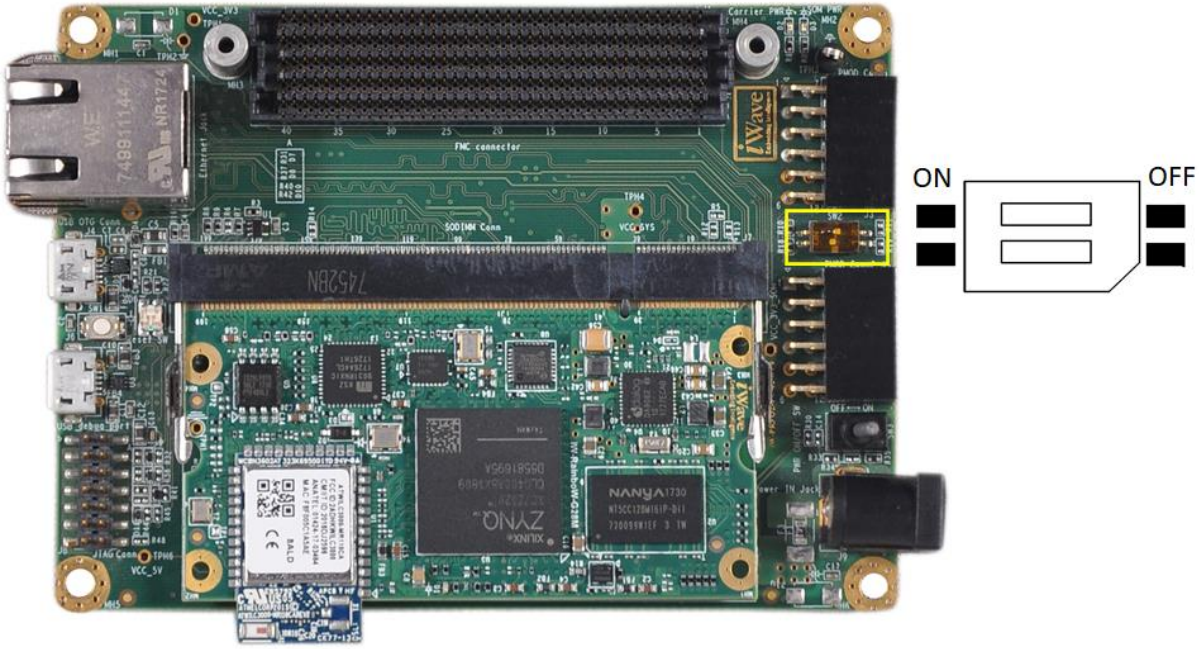

Figure 13: DIP Switch

Important Note: Make Sure that 2nd bit of SW2 DIP switch position in OFF state while booting the SOM from primary boot device.

2.7.5 RTC Coin Cell Holder

The Zynq-7000 SoC SODIMM carrier board supports Coin Cell Holder to connect “2032” series 3V coin cell. This coin cell voltage is connected to SODIMM SOM for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J12) is physically located at the bottom of the board as shown below.

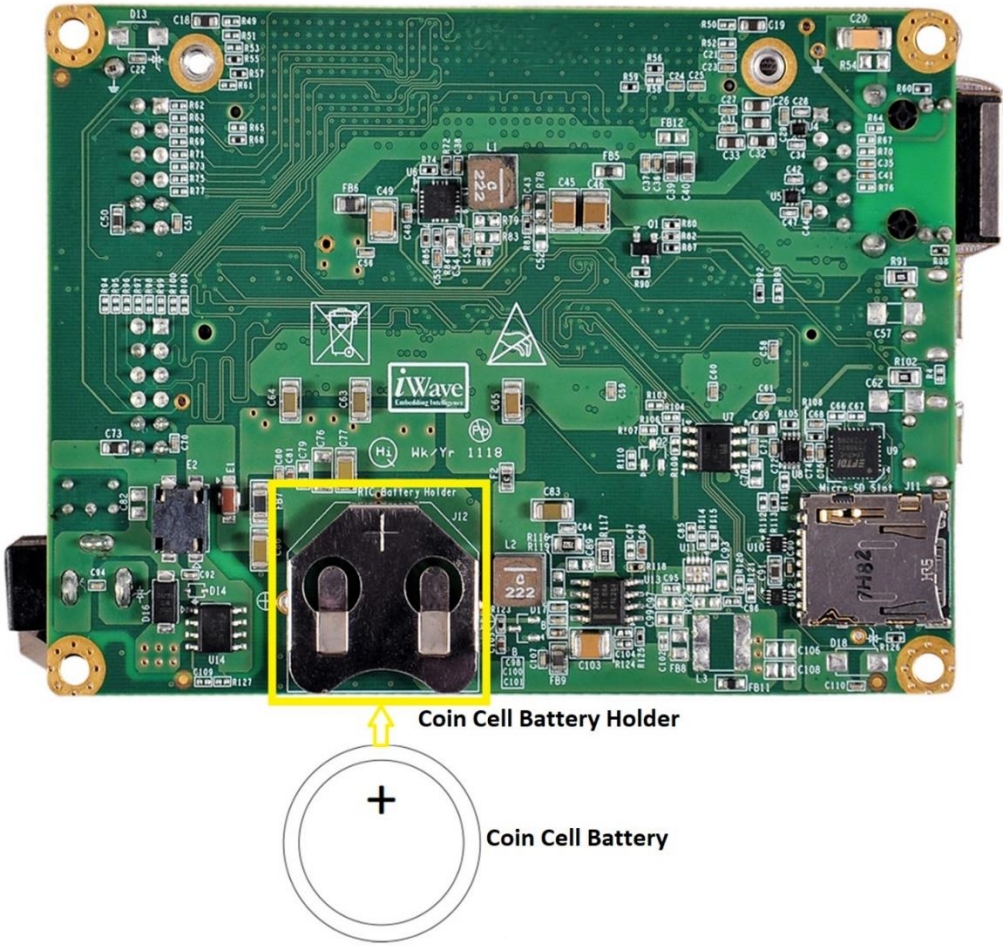

Figure 14: RTC Coin Cell Holder

3. TECHNICAL SPECIFICATION

This section provides detailed information about the Zynq-7000 SoC SODIMM Carrier Board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

3.1.1 Power Input Requirement

The Zynq-7000 SoC SODIMM Carrier Board is designed to work with 5V external power and uses on board voltage regulators for internal power management. 5V power input from an external power supply is connected to the Zynq-7000 SoC SODIMM Carrier Board through Power Jack (J9). This 1.3mm x 3.8mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 1.35mm and an outer dimension of 3.5mm. This connector is physically placed at the top of the board as shown below.

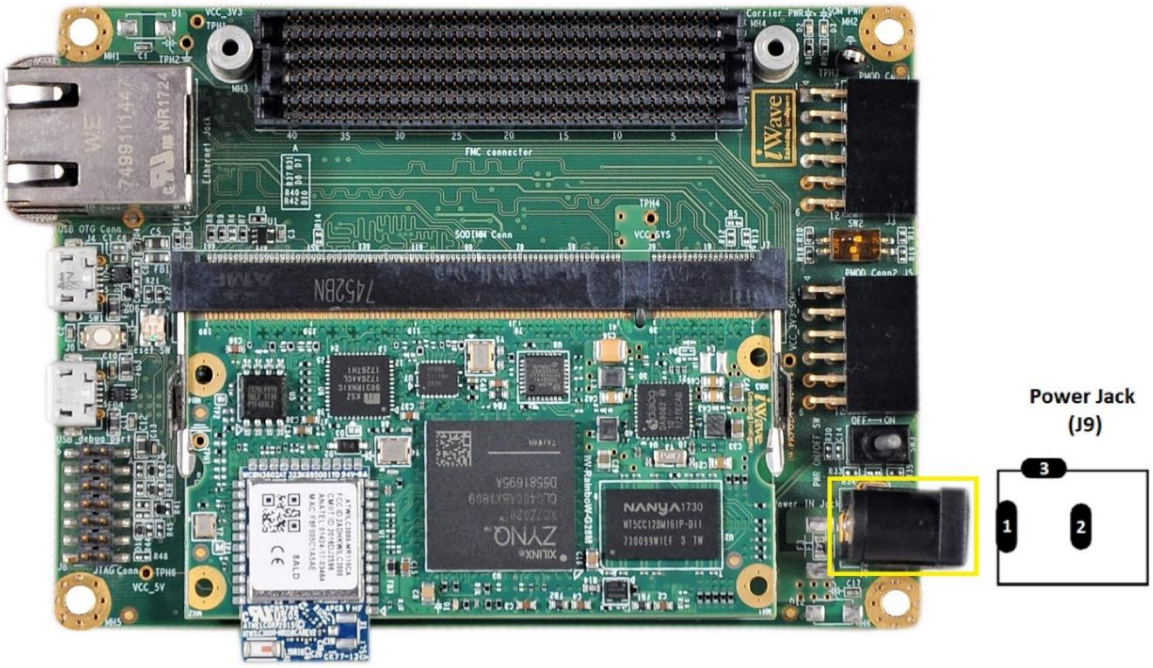

Figure 15: Power Jack

The below table provides the Power Input Requirement Zynq SODIMM Carrier Board.

Table 9: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V	4.75V	5V	5.25V	±50mV
2	VRTC_3V0[1]	0	3V	3.15	±20mV

[1] The Zynq-7000 SoC SODIMM DevKit uses this voltage as backup power source to RTC controller when VCC is off.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of Zynq-7000 SoC SODIMM Development platform.

Table 10: Environmental Specification

Parameters	Min	Max
Operating temperature range	0°C	70°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.2.2 RoHS Compliance

iWave's Zynq-7000 SoC SODIMM Development platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's Zynq-7000 SoC SODIMM Development platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 SODIMM Carrier Board Mechanical Dimensions

The SODIMM carrier board PCB form factor is 100mm x 72mm and Board mechanical dimension is shown below.

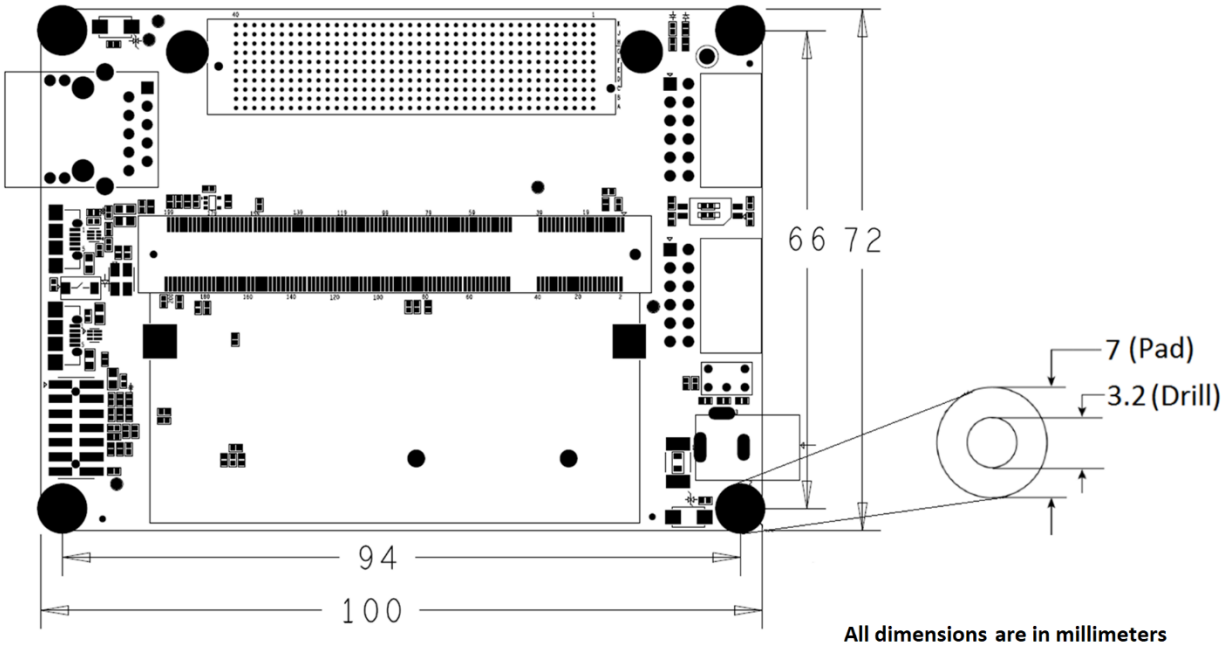

Figure 16: SODIMM carrier board Mechanical dimension – Top View

The SODIMM carrier board PCB thickness is 1.55mm±0.1mm, top side maximum height component is Ethernet Connector (13.55mm) and bottom side maximum height component is Inductor (4.50mm). Please refer the below figure for height details of the Zynq SODIMM carrier board.

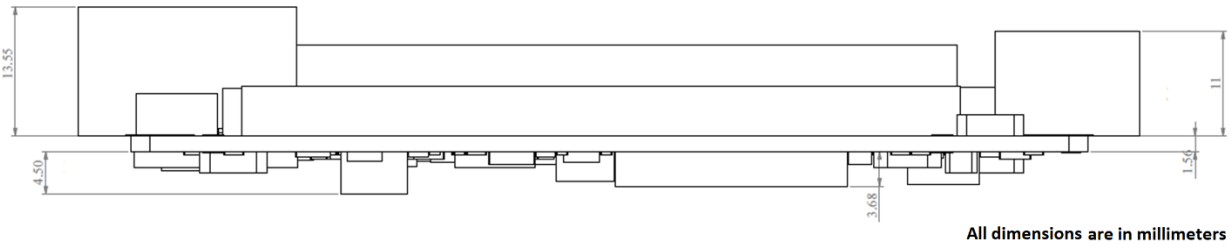

Figure 17: SODIMM carrier board Mechanical dimension – Side View

3.3.2 Guidelines to insert the Zynq-7000 SoC SODIMM SOM into Carrier Board

- Make sure that power is not provided to the SODIMM carrier board.
- Insert the SOM module into the socket at a slight angle (approximately 30 degrees) as shown in the below illustration (A). Note that the socket and module are both keyed, which means the module can be installed one way only.
- To seat the module into the socket, apply firm, even pressure to each end of the module until you feel it slip down into the SODIMM socket connector.
- With the module properly seated in the socket, rotate the module downward, as indicated in the illustration (B). Continue pressing the SOM module downward until the clips at each end of the socket lock into position.
- Once the SOM have been installed, Carrier board can be Powered ON with 5V power supply.

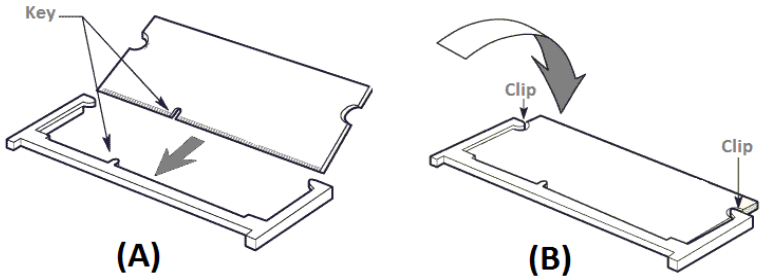

Figure 18: Zynq-7000 SoC SODIMM SOM Insertion procedure

3.3.3 Guidelines to remove the Zynq-7000 SoC SODIMM SOM from Carrier board

- Make sure that power is not provided to the Carrier board.
- When you remove the SOM module, pull away the retention clips (A) on each side of the SOM module.
- The module pops up. Grasp the edge of the module (B), and gently pull the module out of the connector

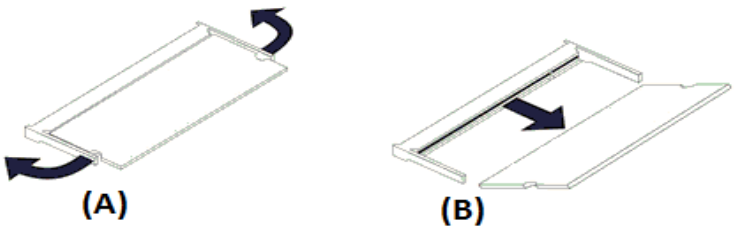

Figure 19: Zynq-7000 SoC SODIMM SOM removal procedure

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for Zynq-7000 SoC SODIMM Development platform which includes Zynq-7000 SoC SODIMM SOM and SODIMM carrier board.

Table 11: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G28D-SM20-3D512M-E008G-LCC	Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT kit with Linux	Commercial
iW-G28D-SM07-3D512M-E008G-LCC	Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, Wi-Fi/BT kit with Linux	Commercial
iW-G28D-SM20-3D512M-E008G-LCD	Zynq 7020 SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT kit with Linux	Commercial
iW-G28D-SM07-3D512M-E008G-LCD	Zynq 7007S SOC (-1), 512MB DDR3, 8GB eMMC Flash, without Wi-Fi/BT kit with Linux	

Important Note: Please contact iWave for orderable part number of higher density/ higher speed grade/ higher memory size supported Zynq-7000 SoC SODIMM SOM based DevKit.

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.


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