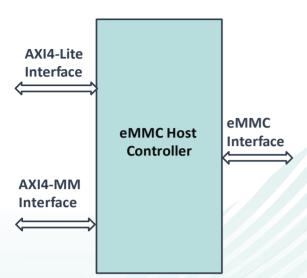


FPGA IP CORE

iW eMMC Host Controller IP



iW-eMMC 5.1 Controller interfaces MMC / eMMC card to any processor with a generic interface. The interface towards the eMMC is realized by the eMMC protocol implemented in the controller. The core supports AXI4-Lite interface for the control and status register access and AXI4-MM interface for data transfer through ADMA2 mode.

Applications

- SOC design integration with eMMC devices
- End applications includes Consumer, Industrial, Medical,
 Automotive, Computer & Storage, Test & Measurement

Highlights

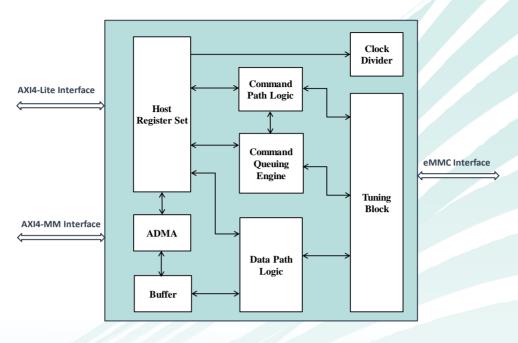
- Compliant with eMMC specification version 5.1
- Supports up to HS400
 Enhanced strobe modes
- Supports command queuing engine
- Supports auto CMD12 feature

Features

- Compliant with eMMC Specification Version 5.1
- Supports Default speed (26Mhz), High speed (52Mhz) mode, HS200,
 HS400 and HS400 Enhanced strobe modes
- Supports command queuing engine
- Supports 1-bit,4-bit and 8-bit eMMC modes
- Supports programmable clock frequency generation to the eMMC card
- Supports Tuning for HS200 mode
- Supports Interrupt and ADMA2 transfer mode of operation
- Individual 2Kbyte data buffer for read and write
- Cyclic Redundancy Check (CRC) for command and data
- Supports timeout monitoring for response, data, CRC token & busy
- Supports a maximum block length of 2K-byte
- Supports both single block and multi block data transfer
- Supports 32-bit AXI4 memory mapped interface towards host processor
- Supports 32-bit AXI4 lite interface towards host processor
- Supports auto CMD12 feature



iW eMMC Host Controller block diagram



Deliverables

- RTL source code or Netlist
- IP example design
- IP datasheet
- Integration Manual
- Linux driver reference

Licensing Options

- Non-Transferable: Single Project/Product Netlist License Single Site or Multi Site
- Non-Transferable: Multi Project /Product Netlist License Single Site or Multi Site
- Non-Transferable: Single Project/Product RTL Source Code License Single Site or Multi Site
- Non-Transferable: Multi Project/Product RTL Source Code License Single Site or Multi Site

Technical Support

iWave provides comprehensive support during your system integration & validation.

- The Client may open a new support incident by emailing to a technical support engineer
- iWave's response time shall be within 24 hours of the initial call, with the details of the action plan to resolve
- Support assistance shall be delivered by telephone, email and/or remote assistance via a web meeting
- iWave shall provide remote debugging support irrespective of the time zone/ region

iWave Systems, a leading FPGA design house enhances your design productivity by providing an extensive suite of proven, optimized and easy-to-use FPGA IP Cores along with reference designs to complement and quicken your applications development. Our extensive suite of IP Cores covers all key markets and applications. Along with the rich set of FPGA IP cores, iWave offers custom FPGA designs tailored to meet the client specifications which includes RTL Design, Integration of iWave's or 3rd Party IP Cores on our FPGA SOMs with Carrier Card/ Custom Hardware/ Off-the-Shelf Evaluation Kits to provide end-to-end solutions targeting Low-Power, High-Performance and Optimized Designs

iW eMMC controller FPGA IP

The IP can be ordered online from the iWave Website http://www.iwavesystems.com/product/emmc-host-controller/ Or from our Local Partners in your region http://www.iwavesystems.com/about-us/business-partner.html

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