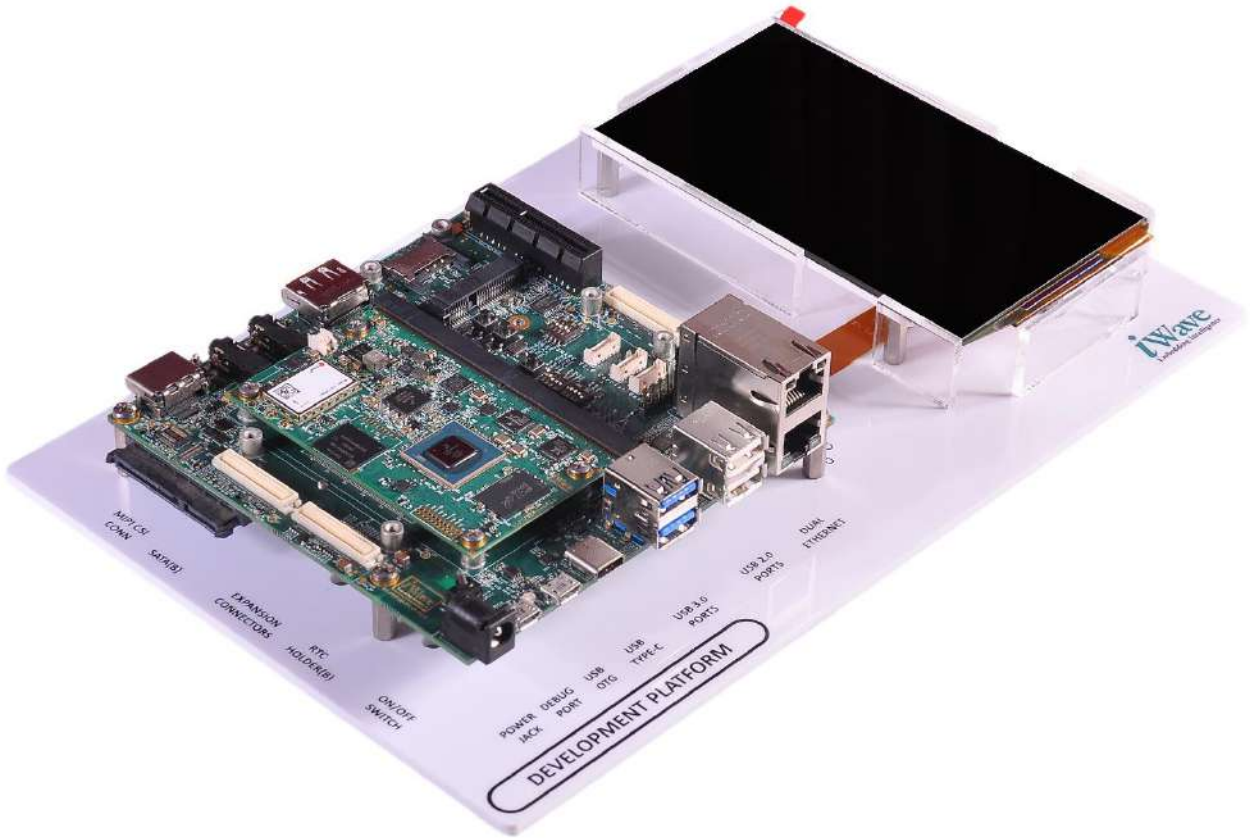
iW-RainboW-G33D
i.MX8M Quad/QuadLite/Dual SMARC Development Platform Hardware User Guide



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7/B, 29th Main, BTM Layout 2nd Stage,
Bangalore, Karnataka,
India – 560076

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1. INTRODUCTION

1.1 Purpose

The iW-RainboW-G33D i.MX8M SMARC SOM development platform incorporates i.MX8M Quad/QuadLite/Dual (Q/QL/D) CPU based SMARC SOM and generic SMARC Carrier board for complete validation of i.MX8M Q/QL/D CPU functionality. This document is the hardware user guide for the i.MX8M SMARC carrier board. This guide provides detailed information on the overall design and usage of the SMARC carrier board from a hardware systems perspective. Complete information about the i.MX8M SMARC SOM hardware is explained in another document "iW-RainboW-G33M-i.MX8M-SMARC-SOM-HardwareUserGuide".

1.2 Overview

iW-RainboW-G33D-i.MX8M development Platform comes with i.MX8M Q/QL/D based SMARC SOM, SMARC V2.0 Generic Carrier board along with 5.5-inch Capacitive Touch Display. The development board can be used for quick prototyping of various applications targeted by the i.MX8M Q/QL/D application processor. With the 120mmx120mm Nano ITX form factor, SMARC carrier board is highly packed with all the necessary on-board connectors to validate the features of i i.MX8M Q/QL/D SMARC SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
Hz	Hertz
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound Bu
IC	Integrated Circuit
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances

Acronyms	Abbreviations
RTC	Real Time Clock
SD	Secure Digital
SMARC SOM	Smart Mobility ARChitecture
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminlogy Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
TMDS	Transition Minimized Differential Signalling
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

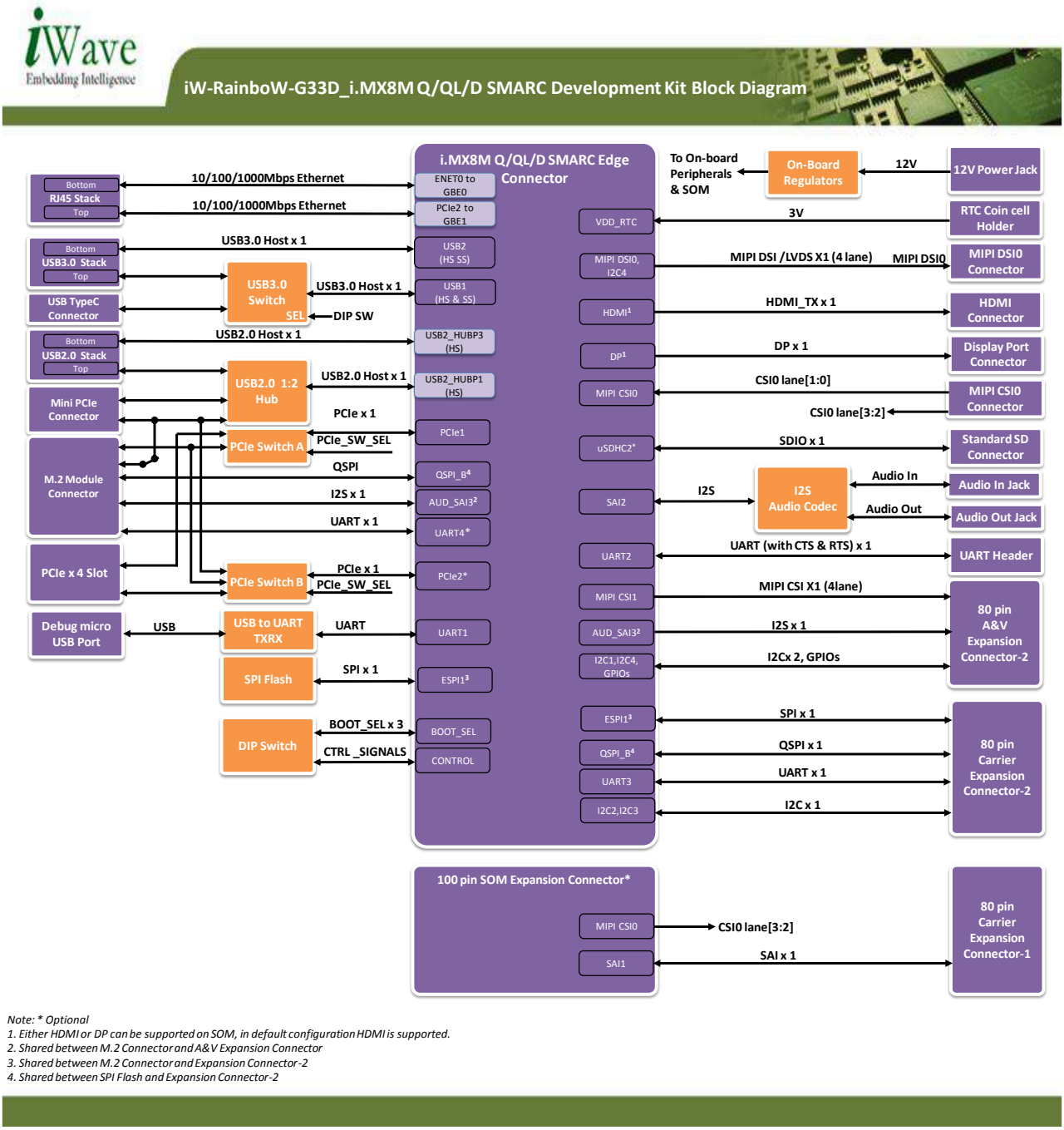
1.5 References

- IMX8MDQLQRM.pdf
- SMARC Specification V2.0

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX8M Q/QL/D SMARC SOM development platform carrier board features with high level block diagram and detailed information about each block.

2.1 i.MX8M Q/QL/D SMARC Development Platform Block Diagram



*Note: * Optional*
1. Either HDMI or DP can be supported on SOM, in default configuration HDMI is supported.
2. Shared between M.2 Connector and A&V Expansion Connector
3. Shared between M.2 Connector and Expansion Connector-2
4. Shared between SPI Flash and Expansion Connector-2

Figure 1: i.MX8M Q/QL/D SMARC Development Platform Block Diagram

2.2 i.MX8M Q/QL/D SMARC Development Platform Features

The i.MX8M Q/QL/D SMARC carrier board supports the following features to validate the NXP's i.MX8M Q/QL/D SMARC SOM Edge connector interfaces.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header

High Speed Interface Features

- PCIe x 1 Port through x4 connector or Mini-PCIe connector or M.2 Connector[1,2]
- USB 3.0 OTG as Device/Host x 1 Port through Type-C Connector (or Type A connector)[3]
- USB 3.0 Host x 1 Port through USB 3.0 Type A Connector

Communication Features

- Dual 10/100/1000Mbps Ethernet through dual stack RJ45MagJack
- USB 2.0 Host x 2 Ports through USB 2.0 dual stack USB Type A Connector
- SDHI (4bit) x 1 Port through Standard SD Connector (Optional)
- M.2 connector with USB, QSPI, UART & I2S interfaces

Audio & Video Features

- MIPI DSI 4lane Display connector with Capacitive touch
- MIPI CSI 2lane/4lane Camera Connector
- HDMI X 1 Port through Type A Connector
- I2S Audio codec with 3.5mm Audio IN and OUT Jack
- Display Port (Optional)

Additional Features

- RTC Coin Cell holder
- SPI Flash (Optional)

On Board Switches

- Power ON/OFF Switch
- Board Configuration DIP Switch
- Boot Selection DIP Switch
- Reset Switch
- Force Boot switch

A&V Expansion Connector

- MIPI CSI - 4 lanes x 1 Port
- I2S x 1 Port
- I2C x 2 Ports
- GPIOs

Carrier board Expansion Connectors

- SPI x 1 Port (Optional - Shared with SPI Flash)
- QSPI x 1 Port (Shared with M.2 connector)
- UART x 1 Port
- I2C x 2 Ports
- SAI x 1 Port
- GPIOs

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported: 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

[1]PCIe Channel A can be connected to either Mini PCIe or M.2 Connector or PETpO of PCIe X4 Connector by using on board configuration switch, Where PCIe channel B can be connected to either Mini PCIe or M.2 Connector or PETp1 of PCIe X4 Connector by using on board configuration switch

[2]At a time, do not set Both PCIe channel A & B neither to mini PCIe nor M.2 connector.

[3]Either USB Type C connector or USB 3.0 Type A top connector can be supported at a time. Anyone can be selected using on board configuration switch.

2.3 SMARC MXM Connector

The i.MX8M Q/QL/D SMARC carrier board supports 314Pin SMARC MXM Edge mating connector for SMARC SOM attachment. This standard 314-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This SMARC MXM Edge mating connector (J16) is physically located at the top of the board as shown below.

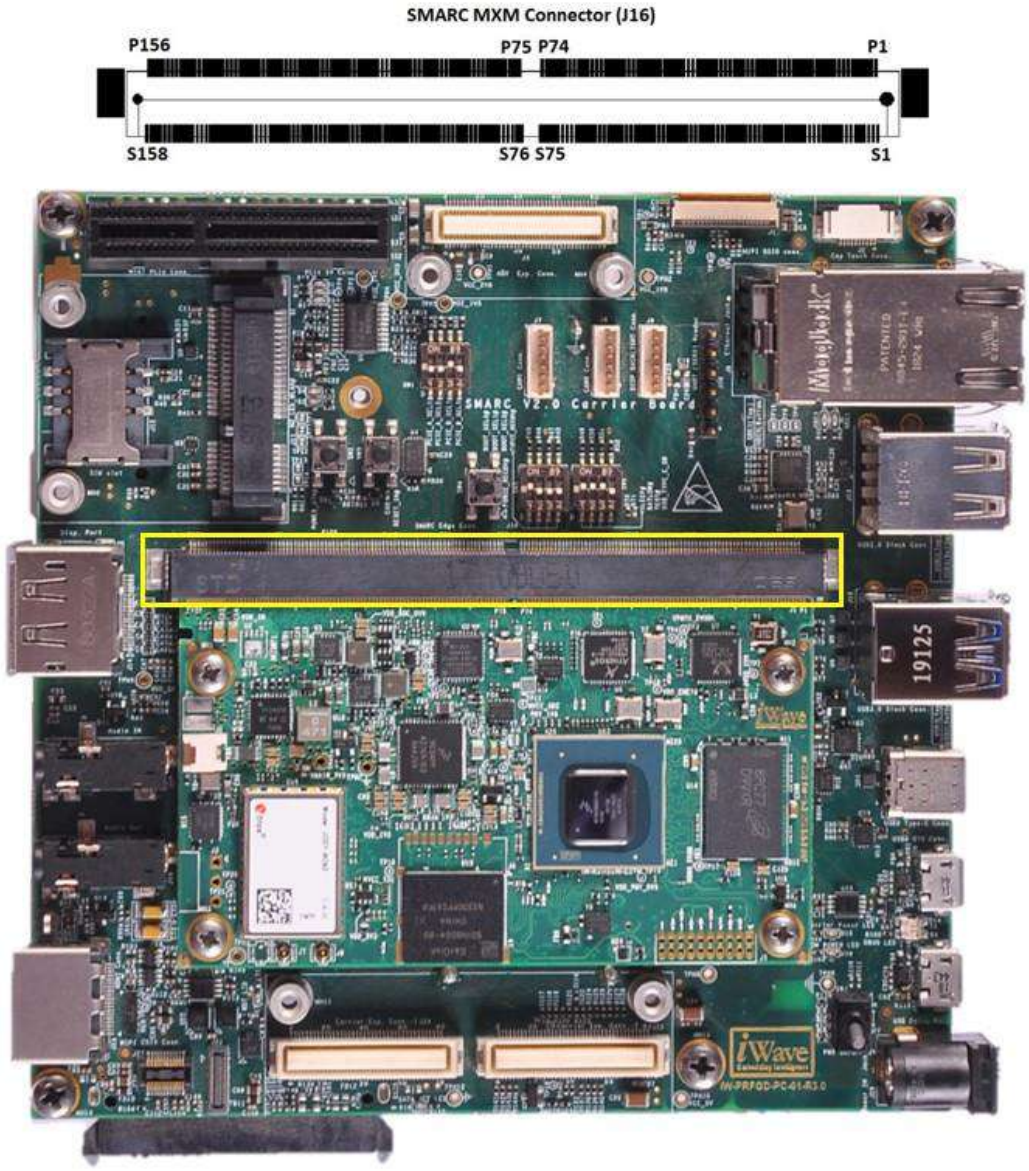


Figure 2: SMARC MXM Connector

2.3.1 SMARC MXM Connector Pin Assignment

Table 3: SMARC MXM Connector Pin Assignment

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
SMARC Primary Side					
P1	SMB_ALERT_1V8#	GPIO_SMB_ALERT(GPIO1_00)	GPIO1_IO00/ T6	I, 1.8V CMOS	SM Bus Alert# (interrupt) signal through GPIO.
P2	GND	GND	NA	Power	Ground.
P3	CSI1_CK+	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P/ B19	O, MIPI	MIPI CSI2 differential clock positive.
P4	CSI1_CK-	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N/ A19	O, MIPI	MIPI CSI2 differential clock negative.
P5	GBE1_SDP	NC	NA	NA	NC.
P6	GBE0_SDP	NC	NA	NA	NC.
P7	CSI1_RX0+	MIPI_CSI2_DATA0_ P	MIPI_CSI2_D0_P/ D20	O, MIPI	MIPI CSI2 differential data lane 0 positive.
P8	CSI1_RX0-	MIPI_CSI2_DATA0_ N	MIPI_CSI2_D0_N/ C20	O, MIPI	MIPI CSI2 differential data lane 0 negative.
P9	GND	GND	NA	Power	Ground.
P10	CSI1_RX1+	MIPI_CSI2_DATA1_ P	MIPI_CSI2_D1_P/ B20	O, MIPI	MIPI CSI2 differential data lane 1 positive.
P11	CSI1_RX1-	MIPI_CSI2_DATA1_ N	MIPI_CSI2_D1_N/ A20	O, MIPI	MIPI CSI2 differential data lane 1 negative.
P12	GND	GND	NA	Power	Ground.
P13	CSI1_RX2+	MIPI_CSI2_DATA2_ P	MIPI_CSI2_D2_P/ B21	O, MIPI	MIPI CSI2 differential data lane 2 positive.
P14	CSI1_RX2-	MIPI_CSI2_DATA2_ N	MIPI_CSI2_D2_N/ A21	O, MIPI	MIPI CSI2 differential data lane 2 negative.
P15	GND	GND	NA	Power	Ground.
P16	CSI1_RX3+	MIPI_CSI2_DATA3_ P	MIPI_CSI2_D3_P/ D19	O, MIPI	MIPI CSI2 differential data lane 3 positive.
P17	CSI1_RX3-	MIPI_CSI2_DATA3_ N	MIPI_CSI2_D3_N/ C19	O, MIPI	MIPI CSI2 differential data lane 3 negative.
P18	GND	GND	NA	Power	Ground.
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 3 negative to bottom port of Dual Magjack.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 3 positive to bottom port of Dual Magjack.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P21	GBE0_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	Ethernet0 100Mbps link status LED signal to bottom port of Dual Magjack.
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet0 link status LED signal.
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 2 negative to bottom port of Dual Magjack.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 2 positive to bottom port of Dual Magjack.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet0 activity status LED signal to bottom port of Dual Magjack.
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 1 negative to bottom port of Dual Magjack.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 1 positive to bottom port of Dual Magjack.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	I, 3.3V Power	CTREF Power for Ethernet0 to Centre Tap of bottom port of Dual Magjack.
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 0 negative to bottom port of Dual Magjack.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet0 MDI differential pair 0 positive to bottom port of Dual Magjack.
P31	SPI0_CS1#	NC	NA	-	NC.
P32	GND	GND	NA	Power	Ground.
P33	SDIO_WP	SD2_WP	SD2_WP/M21	O, 3.3V CMOS	SD Write Protect to Standard SD connector. *Note: This is optional feature in SOM.*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P34	SDIO_CMD	SD2_CMD	SD2_CMD/M22	IO, 1.8/3.3V CMOS	SD Command to Standard SD connector. *Note: This is optional feature in SOM.*
P35	SDIO_CD#	SD2_CD_B	SD2_CD_B/L21	O, 3.3V/CMOS	SD Card Detect to Standard SD connector. *Note: This is optional feature in SOM.*
P36	SDIO_CK	SD2_CLK	SD2_CLK/L22	I, 1.8/3.3V CMOS	SD Clock to Standard SD connector. *Note: This is optional feature in SOM.*
P37	SDIO_PWR_EN	GPIO_SDIO_PWR_EN(GPIO2_19)	SD2_RESET_B/R22	I, 3.3VCMOS	SD Power enable. *Note: This is optional feature in SOM.*
P38	GND	GND	NA	Power	Ground.
P39	SDIO_D0	SD2_DATA0	SD2_DATA0/N22	IO, 1.8/3.3V CMOS	SD Data0to Standard SD connector. *Note: This is optional feature in SOM.*
P40	SDIO_D1	SD2_DATA1	SD2_DATA1/N21	IO, 1.8/3.3V CMOS	SD Data1to Standard SD connector. *Note: This is optional feature in SOM.*
P41	SDIO_D2	SD2_DATA2	SD2_DATA2/P22	IO, 1.8/3.3V CMOS	SD Data2to Standard SD connector. *Note: This is optional feature in SOM.*
P42	SDIO_D3	SD2_DATA3	SD2_DATA3/P21	IO, 1.8/3.3V CMOS	SD Data3to Standard SD connector. *Note: This is optional feature in SOM.*
P43	SPI0_CS0#	eCSPI1_SS0	ECSPI1_SS0/D4	I, 1.8V CMOS	eCSPI1 Chip Select 0.
P44	SPI0_CK	eCSPI1_SCLK	ECSPI1_SCLK/D5	I, 1.8V CMOS	eCSPI1 Clock.
P45	SPI0_DIN	eCSPI1_MISO	ECSPI1_MISO/B4	O, 1.8V CMOS	eCSPI1 Master In Slave Out.
P46	SPI0_DO	eCSPI1_MOSI	ECSPI1_MOSI/A4	I, 1.8V CMOS	eCSPI1 Master Out Slave In.
P47	GND	GND	NA	Power	Ground.
P48	SATA_TX+	NC	NA	-	NC.
P49	SATA_TX-	NC	NA	-	NC.
P50	GND	GND	NA	Power	Ground.
P51	SATA_RX+	NC	NA	-	NC.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P52	SATA_RX-	NC	NA	-	NC.
P53	GND	GND	NA	Power	Ground.
P54	ESPI_CS0#	QSPIB_SS0_B(NAND_CE2_B)	NAND_CE2_B/F21	I, 1.8V CMOS	QSPIB Chip Select 0.
P55	ESPI_CS1#	QSPIB_SS1_B(NAND_CE3_B)	NAND_CE3_B/H20	I, 1.8V CMOS	QSPIB Chip Select 1.
P56	ESPI_CK	QSPI_B_SCLK(NAND_CLE)	NAND_CLE/H21	I, 1.8V CMOS	QSPIB Clock.
P57	ESPI_IO_0	QSPI_B_DATA0(NAND_DATA04)	NAND_DATA04/L20	IO, 1.8V CMOS	QSPIB DATA 0.
P58	ESPI_IO_1	QSPI_B_DATA1(NAND_DATA05)	NAND_DATA05/J22	IO, 1.8V CMOS	QSPIB DATA 1.
P59	GND	GND	NA	Power	Ground.
P60	USB0+	USB_OTG1_DP	USB1_DP/A14	IO, USB HS	USB Port0 Data Positive to USB2.0 OTG connector (J20). *Note: This is optional feature in SOM.*
P61	USB0-	USB_OTG1_DM	USB1_DN/B14	IO, USB HS	USB Port0 Data Negative to USB2.0 OTG connector (J20). *Note: This is optional feature in SOM.*
P62	USB0_EN_OC#	USB3_EN_OC(GPIO3_19)	SAI5_RXFS/N4	IO, 3.3V CMOS	USB Port0 Power Enable/ Over Current Indicator. *Note: This is optional feature in SOM.*
P63	USB0_VBUS_DET	VBUS_OTG	NA	O, 5V Power	USB Port0 OTG VBUS detection. *Note: This is optional feature in SOM.*
P64	USB0_OTG_ID	USB_OTG1_ID	USB1_ID/C14	O, 3.3V CMOS	USB Port0 OTG ID. This is *Note: This is optional feature in SOM.*
P65	USB1+	USB_HUB1OUT_DP	NA	IO, USB HS	USB Port2 HUB OUT1 Data Positive to 2 Port USB HUB.
P66	USB1-	USB_HUB1OUT_DM	NA	IO, USB HS	USB Port2 HUB OUT1 Data Negative to 2 Port USB HUB.
P67	USB1_EN_OC#	USB_HUB1_OC	NA	O, 3.3V CMOS	USB Port2 HUB OUT1 Over Current Indicator.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P68	GND	GND	NA	Power	Ground.
P69	USB2+	USB_HUB2OUT_DP	NA	IO, USB HS	USB Port2 HUB OUT2 Data Positive to bottom Port of USB2.0 TypeA connector(J15).
P70	USB2-	USB_HUB2OUT_DM	NA	IO, USB HS	USB Port2 HUB OUT2 Data Negative to bottom Port of USB2.0 TypeA connector(J15).
P71	USB2_EN_OC#	USB_HUB2_OC	GPIO1_IO05/P7	O, 3.3V CMOS	USB Port2 HUB OUT2 Over Current Indicator.
P72	RSVD4	NC	NA	-	NC.
P73	RSVD5	NC	NA	-	NC.
P74	USB3_EN_OC#	GPIO_USB3_EN_OC(GPIO3_19)	SAI5_RXFS/N4	O, 3.3V CMOS	USB Port1 Over Current Indicator.
KEY					
P75	PCIE_A_RST#	GPIO_PCIE_RST(GPIO5_4)	SPDIF_RX/G6	I, 3.3V CMOS	PCIe_A Reset.
P76	USB4_EN_OC#	USB_HUB3_OC	NA	O, 3.3V CMOS	USB Port2 HUB OUT3 Over Current Indicator.
P77	RSVD6	NC	NA	-	NC.
P78	RSVD7	NC	NA	-	NC.
P79	GND	GND	NA	Power	Ground.
P80	PCIE_C_REFCK+	NC	NA	-	NC.
P81	PCIE_C_REFCK-	NC	NA	-	NC.
P82	GND	GND	NA	Power	Ground.
P83	PCIE_A_REFCK+	PCIE1_REFCLK_P	NA	I, PCIe	PCIe1 Reference Clock Positive.
P84	PCIE_A_REFCK-	PCIE1_REFCLK_N	NA	I, PCIe	PCIe1 Reference Clock Negative.
P85	GND	GND	NA	Power	Ground.
P86	PCIE_A_RX+	PCIE1_RXP	PCIE1_RXN_P/H25	O, PCIe	PCIe1 Receive Positive.
P87	PCIE_A_RX-	PCIE1_RXN	PCIE1_RXN_N/H24	O, PCIe	PCIe1 Receive Negative.
P88	GND	GND	NA	Power	Ground.
P89	PCIE_A_TX+	PCIE1_TXP	PCIE1_TXN_P/J25	I, PCIe	PCIe1 Transmit Positive.
P90	PCIE_A_TX-	PCIE1_TXN	PCIE1_TXN_N/J24	I, PCIe	PCIe1 Transmit Negative.
P91	GND	GND	NA	Power	Ground.
P92	HDMI_D2+/ DP1_LANE0+	HDMI_TX_DATA2_P	HDMI_TX_P_LN_2/ N2	I, TMDS	HDMI Transceiver 2 Positive to HDMI Connector.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P93	HDMI_D2-/ DP1_LANE0-	HDMI_TX_DATA2_N	HDMI_TX_M_LN_2/ N1	I, TMDS	HDMI Transceiver 2 Negative to HDMI Connector.
P94	GND	GND	NA	Power	Ground.
P95	HDMI_D1+/ DP1_LANE1+	HDMI_TX_DATA1_P	HDMI_TX_P_LN_1/ U2	I, TMDS	HDMI Transceiver 1 Positive to HDMI Connector.
P96	HDMI_D1-/ DP1_LANE1-	HDMI_TX_DATA1_N	HDMI_TX_M_LN_1/ U1	I, TMDS	HDMI Transceiver 1 Negative to HDMI Connector.
P97	GND	GND	NA	Power	Ground.
P98	HDMI_D0+/ DP1_LANE2+	HDMI_TX_DATA0_P	HDMI_TX_P_LN_0/ T1	I, TMDS	HDMI Transceiver 0 Positive to HDMI Connector.
P99	HDMI_D0-/ DP1_LANE2-	HDMI_TX_DATA0_N	HDMI_TX_M_LN_0/ T2	I, TMDS	HDMI Transceiver 0 Negative to HDMI Connector.
P100	GND	GND	NA	Power	Ground.
P101	HDMI_CK+/ DP1_LANE3+	HDMI_CLK_P	HDMI_TX_P_LN_3/ M1	I, TMDS	HDMI Transceiver CLK Positive to HDMI Connector.
P102	HDMI_CK-/ DP1_LANE3-	HDMI_CLK_N	HDMI_TX_M_LN_3/ M2	I, TMDS	HDMI Transceiver CLK Negative to HDMI Connector.
P103	GND	GND	NA	Power	Ground.
P104	HDMI_HPD/ DP1_HPD	HDMI_HPD	HDMI_HPD/W2	O, 1.8V CMOS	HDMI Hot Plug Detect from HDMI Connector.
P105	HDMI_CTRL_CK/ DP1_AUX+	HDMI_CTRL_SCL	HDMI_DDC_SCL/R3	I, 1.8V CMOS	HDMI DDC Clock to HDMI Connector through Voltage Level translator.
P106	HDMI_CTRL_DAT/ DP1_AUX-	HDMI_CTRL_SDA	HDMI_DDC_SDA/P3	IO, 1.8V CMOS	HDMI DDC DATA to HDMI Connector through Voltage Level translator.
P107	DP1_AUX_SEL	HDMI_CEC	HDMI_CEC/W3	O, 1.8V CMOS	NC.
P108	GPIO0/ CAM0_PWR#	SMARC_GPIO_0(GPIO3_16)	GPIO3_16(NAND_READY_B)/K20	IO, 1.8V CMOS	General Purpose Input/ Output 0.
P109	GPIO1/ CAM1_PWR#	SMARC_GPIO_1(GPIO1_12)	GPIO1_IO12/L7	IO, 1.8V CMOS	General Purpose Input/ Output 1.
P110	GPIO2/ CAM0_RST#	SMARC_GPIO_2(GPIO1_15)	GPIO1_IO15/J6	IO, 1.8V CMOS	General Purpose Input/ Output 2. Used for Camera RESET.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P111	GPIO3/ CAM1_RST#	SMARC_GPIO_3(GPIO1_11)	GPIO1_IO11/L6	IO, 1.8V CMOS	General Purpose Input/ Output 3. Connected to A&V Expansion connector.
P112	GPIO4/HDA_RST#	SMARC_GPIO_4(GPIO1_10)	GPIO1_IO10/M7	IO, 1.8V CMOS	General Purpose Input/ Output 4. USB Type C Port selection.
P113	GPIO5/PWM_OUT	SMARC_GPIO_5(GPIO1_01)	GPIO1_IO01/T7	IO, 1.8V CMOS	General Purpose Input/ Output 5. Connected to M.2 Reset.
P114	GPIO6/TACHIN	SMARC_GPIO_6(GPIO1_09)	GPIO1_IO09/M6	IO, 1.8V CMOS	General Purpose Input/ Output 6. Connected to USB Type C Controller interrupt.
P115	GPIO7	SMARC_GPIO_7(GPIO1_06)	GPIO1_IO06/N5	IO, 1.8V CMOS	General Purpose Input/ Output 7. Connected to Touch interrupt.
P116	GPIO8	SMARC_GPIO_8(GPIO1_08)	GPIO1_IO08/N7	IO, 1.8V CMOS	General Purpose Input/ Output 8. Connected to Headphone Detect.
P117	GPIO9	SMARC_GPIO_9(GPIO1_03)	GPIO1_IO03/P4	IO, 1.8V CMOS	General Purpose Input/ Output 9. Connected to MIPI Display RESET.
P118	GPIO10	SMARC_GPIO_10(GPIO1_07)	GPIO1_IO07/N6	IO, 1.8V CMOS	General Purpose Input/ Output 10. Connected to PCIe connector for Wireless disable (active low).
P119	GPIO11	SMARC_GPIO_11(GPIO1_04)	GPIO1_IO04/P5	IO, 1.8V CMOS	General Purpose Input/ Output 11. Connected to MIC Detect.
P120	GND	GND	NA	Power	Ground.
P121	I2C_PM_CK	I2C1_SCL	I2C1_SCL/E7	I, 1.8V CMOS	I2C1 Clock. *Note: This is optional feature in SOM.*
P122	I2C_PM_DAT	I2C1_SDA	I2C1_SDA/E8	IO, 1.8V CMOS	I2C1 Data. *Note: This is optional feature in SOM.*
P123	BOOT_SEL0#	BOOT_SEL0#	NA	O, 1.8V CMOS	Boot Media Select bit 0 from 4bit DIP Switch (SW5).

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P124	BOOT_SEL1#	BOOT_SEL1#	NA	O, 1.8V CMOS	Boot Media Select bit 1 from 4bit DIP Switch (SW5).
P125	BOOT_SEL2#	BOOT_SEL2#	NA	O, 1.8V CMOS	Boot Media Select bit 2 from 4bit DIP Switch (SW5).
P126	RESET_OUT#	GPIO_RESET_OUT(GPIO3_25)	SAI5_MCLK/K4	I, 1.8V CMOS	Reset out from CPU GPIO to all other peripherals.
P127	RESET_IN#	RESET_IN#	NA	O, 1.8V CMOS	Hard RESET Input to SOM from Reset Push Button Switch (SW3).
P128	POWER_BTN#	POWER_BUTTON	ONOFF/W21	O, 1.8V CMOS	Power ON /OFF Input to SOM from Power Push Button Switch (SW2).
P129	SER0_TX	UART2_TXD	UART2_TXD/D6	I, 1.8V CMOS	UART2 Transmitter to Data UART Header (J10) through Voltage Level translator.
P130	SER0_RX	UART2_RXD	UART2_RXD/B6	O, 1.8V CMOS	UART2 Receiver to Data UART Header (J10) through Voltage Level translator.
P131	SER0_RTS#	UART2_CTS_B(UART4_TXD)	UART4_RXD/C6	0, 1.8V CMOS	UART2 Clear to Send Data UART Header (J10) through Voltage Level translator.
P132	SER0_CTS#	UART2_RTS_B(UART4_RXD)	UART4_TXD/D7	I, 1.8V CMOS	UART2 Request to Send to Data UART Header (J10) through Voltage Level translator.
P133	GND	GND	NA	Power	Ground.
P134	SER1_TX	UART3_TXD	UART3_TXD/B7	O, 1.8V CMOS	UART3 Transmitter to Carrier Expansion Connector2.
P135	SER1_RX	UART3_RXD	UART3_RXD/A6	I,1.8V CMOS	UART3 Receiver to Carrier Expansion Connector2.
P136	SER2_TX	UART4_TX	ECSPI2_MOSI/E5	O, 1.8V CMOS	UART4 Transmitter to M.2 Connector. *Note: This is optional feature in SOM.*
P137	SER2_RX	UART4_RX	ECSPI2_SCLK/C5	I, 1.8V CMOS	UART4 Receiver to M.2 Connector. *Note: This is optional feature in SOM.*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P138	SER2_RTS#	UART4_CTS_B	ECSPI2_MISO/B5	O, 1.8V CMOS	UART4 Clear to Send to M.2 Connector. *Note: This is optional feature in SOM.*
P139	SER2_CTS#	UART4_RTS_B	ECSPI2_SS0/A5	I, 1.8V CMOS	UART4 Request to Send to M.2 Connector. *Note: This is optional feature in SOM.*
P140	SER3_TX	UART1_TXD	UART1_TXD/A7	I, 1.8V CMOS	UART1 Transmitter to Debug UART.
P141	SER3_RX	UART1_RXD	UART1_RXD/C7	O, 1.8V CMOS	UART1 Receiver to Debug UART.
P142	GND	GND	NA	Power	Ground.
P143	CAN0_TX	NC	NA	-	NC.
P144	CAN0_RX	NC	NA	-	NC.
P145	CAN1_TX	NC	NA	-	NC.
P146	CAN1_RX	NC	NA	-	NC.
P147	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P148	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P149	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P150	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P151	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P152	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P153	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P154	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P155	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
P156	VDD_IN	VDD_IN	NA	O, 5V Power	Supply Voltage.
SMARC Secondary Side					
S1	CSI1_TX+/ I2C_CAM1_CK	I2C1_SCL	I2C1_SCL/E7	I, 1.8V CMOS	I2C1 Clock.
S2	CSI1_TX-/ I2C_CAM1_DAT	I2C1_SDA	I2C1_SDA/E8	IO, 1.8V CMOS	I2C1 Data.
S3	GND	GND	NA	Power	Ground.
S4	RSVD1	NC	NA	-	NC.
S5	CSI0_TX-/ I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/G8	I, 1.8V CMOS	I2C3 Clock.
S6	CAM_MCK	MCLK	SAI1_MCLK/A3	O, 1.8V CMOS	Master Clock for Camera.
S7	CSI0_TX+/ I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/E9	IO, 1.8V CMOS	I2C3 Data.
S8	CSI0_CK+	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ B22	O, MIPI	MIPI CSI1 differential Clock positive.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S9	CSI0_CK-	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ A22	O, MIPI	MIPI CSI1 differential Clock negative.
S10	GND	GND	NA	Power	Ground.
S11	CSI0_RX0+	MIPI_CSI1_DATA0_P	MIPI_CSI1_D0_P/ B23	O, MIPI	MIPI CSI1 differential data lane 0 positive.
S12	CSI0_RX0-	MIPI_CSI1_DATA0_N	MIPI_CSI1_D0_N/ A23	O, MIPI	MIPI CSI1 differential data lane 0 negative.
S13	GND	GND	NA	Power	Ground.
S14	CSI0_RX1+	MIPI_CSI1_DATA1_P	MIPI_CSI1_D1_P/ D22	O, MIPI	MIPI CSI1 differential data lane 1 positive.
S15	CSI0_RX1-	MIPI_CSI1_DATA1_N	MIPI_CSI1_D1_N/ C22	O, MIPI	MIPI CSI1 differential data lane 1 negative.
S16	GND	GND	NA	Power	Ground.
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 0 positive to top port of Dual Magjack.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 0 negative to top port of Dual Magjack.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	I, 3.3V CMOS	Ethernet1 100Mbps link status LED signal to top port of Dual Magjack.
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 1 positive to top port of Dual Magjack.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 1 negative to top port of Dual Magjack.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	I, 3.3V CMOS	Ethernet1 1000Mbps link status LED signal.
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 2 positive to top port of Dual Magjack.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair2 negative

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					to top port of Dual Magjack.
S25	GND	GND	NA	Power	Ground.
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 3 positive to top port of Dual Magjack.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE	Gigabit Ethernet1 MDI differential pair 3 negative to top port of Dual Magjack.
S28	GBE1_CTREF	NC	NA	-	NC.
S29	PCIE_D_TX+	NC	NA	-	NC.
S30	PCIE_D_TX-	NC	NA	-	NC.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet1 activity status LED signal to top port of Dual Magjack.
S32	PCIE_D_RX+	NC	NA	-	NC.
S33	PCIE_D_RX-	NC	NA	-	NC.
S34	GND	GND	NA	Power	Ground.
S35	USB4+	USB_HUB3OUT_DP	NA	IO, USB HS	USB Port2 HUB OUT3 Data Positive to bottom Port of Dual Stack USB2.0 TypeA Connector (J13).
S36	USB4-	USB_HUB3OUT_DM	NA	IO, USB HS	USB Port2 HUB OUT3 Data Negative to bottom Port of Dual Stack USB2.0 TypeA Connector (J13).
S37	USB3_VBUS_DET	VBUS_OTG	NA	5V, Power	USB Port1 VBUS detection.
S38	AUDIO_MCK	SAI2_MCLK	SAI2_MCLK/H5	I, 1.8V CMOS	Master Clock for Audio codec.
S39	I2S0_LRCK	SAI2_TXFS	SAI2_TXFS/H4	O, 1.8V CMOS	Serial Audio Interface 2 Frame Sync to I2S Audio Codec.
S40	I2S0_SDOUT	SAI2_TXD0	SAI2_TXD0/G5	O, 1.8V CMOS	Serial Audio Interface 2 Data Transmitter to I2S Audio Codec.
S41	I2S0_SDIN	SAI2_RXD0	SAI2_RXD0/H6	I, 1.8V CMOS	Serial Audio Interface 2 Data Receiver to I2S Audio Codec.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S42	I2S0_CK	SAI2_TXC	SAI2_TXC/J5	O, 1.8V CMOS	Serial Audio Interface 2 Clock to I2S Audio Codec.
S43	ESPI_ALERT0#	NC	NA	-	NC.
S44	ESPI_ALERT1#	NC	NA	-	NC.
S45	RSVD2	NC	NA	-	NC.
S46	RSVD3	NC	NA	-	NC.
S47	GND	GND	NA	Power	Ground.
S48	I2C_GP_CK	I2C2_SCL	I2C2_SCL/G7	I, 1.8V CMOS	I2C2 Clock.
S49	I2C_GP_DAT	I2C2_SDA	I2C2_SDA/F7	IO, 1.8V CMOS	I2C2 Data.
S50	HDA_SYNC/ I2S2_LRCK	SAI3_TXFS	SAI3_TXFS/G3	I, 1.8V CMOS	Serial Audio Interface 3 Frame Sync.
S51	HDA_SDO/ I2S2_SDOUT	SAI3_TXD0	SAI3_TXD/C3	I, 1.8V CMOS	Serial Audio Interface 3 Data Transmitter.
S52	HDA_SD/ I2S2_SDIN	SAI3_RXD0	SAI3_RXD/F3	O, 1.8V CMOS	Serial Audio Interface 3 Data Receiver.
S53	HDA_CK/ I2S2_CK	SAI3_TXC	SAI3_TXC/C4	I, 1.8V CMOS	Serial Audio Interface 3 Clock.
S54	SATA_ACT#	NC	NA	-	NC.
S55	USB5_EN_OC#	USB_HUB4_OC	NA	O, 3.3V CMOS	USB Port2 HUB OUT4 Over Current Indicator.
S56	ESPI_IO_2	QSPI_B_DATA2(NAND_DATA06)	NAND_DATA06/L19	IO, 1.8V CMOS	QSPIB Data2.
S57	ESPI_IO_3	QSPI_B_DATA3(NAND_DATA07)	NAND_DATA07/M19	IO, 1.8V CMOS	QSPIB Data3.
S58	ESPI_RESET#	QSPI_B_DQS(NAND_RE_B)	NAND_RE_B/K19	O, 1.8V CMOS	QSPIB RESET.
S59	USB5+	USB_HUB4OUT_DP	NA	IO, USB HS	USB Port2 HUB OUT4 Data Positive to M.2 Connector.
S60	USB5-	USB_HUB4OUT_DM	NA	IO, USB HS	USB Port2 HUB OUT4 Data Negative to M.2 Connector.
S61	GND	GND	NA	Power	Ground.
S62	USB3_SSTX+	USB1_TX_P	USB1_TX_P/A13	I, USB SS	USB Port1 Super Speed Transmit Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).
S63	USB3_SSTX-	USB1_TX_N	USB1_TX_N/ B13	I, USB SS	USB Port1 Super Speed Transmit Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S64	GND	GND	NA	Power	Ground.
S65	USB3_SSRX+	USB1_RX_P	USB1_RX_P/ A12	O, USB SS	USB Port1 Super Speed Receive Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).
S66	USB3_SSRX-	USB1_RX_N	USB1_RX_N/ B12	O, USB SS	USB Port1 Super Speed Receive Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).
S67	GND	GND	NA	Power	Ground.
S68	USB3+	USB_OTG1_DP	USB1_DP/A14	IO, USB HS	USB Port1 High Speed Data Positive to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).
S69	USB3-	USB_OTG1_DM	USB1_DN/B14	IO, USB HS	USB Port1 High Speed Data Negative to Top Port of Dual Stack USB3.0 TypeA Connector (J15) or TypeC Connector (J18).
S70	GND	GND	NA	Power	Ground.
S71	USB2_SSTX+	USB2_TX_P	USB2_TX_P/A9	I, USB SS	USB Port2 Super Speed Transmit Positive to bottom Port of Dual Stack USB3.0 TypeA Connector (J15).
S72	USB2_SSTX-	USB2_TX_N	USB2_TX_N/B9	I, USB SS	USB Port2 Super Speed Transmit Negative to bottom Port of Dual Stack USB3.0 TypeA Connector (J15).
S73	GND	GND	NA	Power	Ground.
S74	USB2_SSRX+	USB2_RX_P	USB2_RX_P/A8	O, USB SS	USB Port2 Super Speed Receive Positive to bottom Port of Dual Stack USB3.0 TypeA Connector (J15).
S75	USB2_SSRX-	USB2_RX_N	USB2_RX_N/B8	O, USB SS	USB Port2 Super Speed Receive Negative to bottom Port of Dual Stack

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					USB3.0 TypeA Connector (J15).
			KEY		
S76	PCIE_B_RST#	GBE_PERST_N(GPIO5_4)	SPDIF_RX/G6	I, 3.3V CMOS	PCIe_B RESET. *Note: This is optional feature in SOM.*
S77	PCIE_C_RST#	NC	NA	-	NC.
S78	PCIE_C_RX+	NC	NA	-	NC.
S79	PCIE_C_RX-	NC	NA	-	NC.
S80	GND	GND	NA	Power	Ground.
S81	PCIE_C_TX+	NC	NA	-	NC.
S82	PCIE_C_TX-	NC	NA	-	NC.
S83	GND	GND	NA	Power	Ground.
S84	PCIE_B_REFCK+	PCIE2_REFCLK_P	NA	I, PCIe	PCIe2 Reference Clock Positive. *Note: This is optional feature in SOM.*
S85	PCIE_B_REFCK-	PCIE2_REFCLK_N	NA	I, PCIe	PCIe2 Reference Clock Negative. *Note: This is optional feature in SOM.*
S86	GND	GND	NA	Power	Ground.
S87	PCIE_B_RX+	PCIE2_RXP	PCIE2_RXN_P/D25	O, PCIe	PCIe2 Receiver Positive. *Note: This is optional feature in SOM.*
S88	PCIE_B_RX-	PCIE2_RXN	PCIE2_RXN_N/D24	O, PCIe	PCIe2 Receiver Negative. *Note: This is optional feature in SOM.*
S89	GND	GND	NA	Power	Ground.
S90	PCIE_B_TX+	PCIE2_TXP	PCIE2_TXN_P/E25	I, PCIe	PCIe2 Transmitter Positive. *Note: This is optional feature in SOM.*
S91	PCIE_B_TX-	PCIE2_TXN	PCIE2_TXN_N/E24	I, PCIe	PCIe2 Transmitter Negative. *Note: This is optional feature in SOM.*
S92	GND	GND	NA	Power	Ground.
S93	DP0_LANE0+	HDMI_TX_DATA0_P	HDMI_TX_P_LN_0/T1	I, TMDS	DP Transmitter Data0 Positive to DP connector. *Note: This is optional feature in SOM.*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S94	DP0_LANE0-	HDMI_TX_DATA0_N	HDMI_TX_M_LN_0/ T2	I, TMDS	DP Transmitter Data0 Negative to DP connector. *Note: This is optional feature in SOM.*
S95	DP0_AUX_SEL	NC	NA	-	NC.
S96	DP0_LANE1+	HDMI_TX_DATA1_P	HDMI_TX_P_LN_1/ U2	I, TMDS	DP Transmitter Data1 Positive to DP connector. *Note: This is optional feature in SOM.*
S97	DP0_LANE1-	HDMI_TX_DATA1_N	HDMI_TX_M_LN_1/ U1	I, TMDS	DP Transmitter Data1 Negative to DP connector. *Note: This is optional feature in SOM.*
S98	DP0_HPD	HDMI_HPD	HDMI_HPD/ W2	I, 1.8V CMOS	Hot plug Detect from DP Connector *Note: This is optional feature in SOM.*
S99	DP0_LANE2+	HDMI_TX_DATA2_P	HDMI_TX_P_LN_2/ N2	I, TMDS	DP Transmitter Data2 Positive to DP connector. *Note: This is optional feature in SOM.*
S100	DP0_LANE2-	HDMI_TX_DATA2_N	HDMI_TX_M_LN_2/ N1	I, TMDS	DP Transmitter Data2 Negative to DP connector. *Note: This is optional feature in SOM.*
S101	GND	GND	NA	Power	Ground.
S102	DP0_LANE3+	HDMI_CLK_P	HDMI_TX_P_LN_3/ M1	I, TMDS	DP Clock Positive to DP *Note: This is optional feature in SOM.*
S103	DP0_LANE3-	HDMI_CLK_N	HDMI_TX_M_LN_3/ M2	I, TMDS	DP Clock Negative to DP *Note: This is optional feature in SOM.*
S104	USB3_OTG_ID	USB_OTG1_ID	USB1_ID/C14	-	NC.
S105	DP0_AUX+	HDMI_AUX_P	HDMI_AUX_P/V1	I, DIFF	DP AUX Positive to DP connector. *Note: This is optional feature in SOM.*
S106	DP0_AUX-	HDMI_AUX_N	HDMI_AUX_N/V2	I, DIFF	DP AUX Negative to DP connector. *Note: This is optional feature in SOM.*

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S107	LCD1_BKLT_EN	NC	NA	-	NC.
S108	LVDS1_CK+/ eDP1_AUX+/ DSI1_CLK+	NC	NA	-	NC.
S109	LVDS1_CK-/ eDP1_AUX-/ DSI1_CLK-	NC	NA	-	NC.
S110	GND	GND	NA	Power	Ground.
S111	LVDS1_0+/ eDP1_TX0+/ DSI1_D0+	NC	NA	-	NC.
S112	LVDS1_0-/ eDP1_TX0-/ DSI1_D0-	NC	NA	-	NC.
S113	eDP1_HPD	NC	NA	-	NC.
S114	LVDS1_1+/ eDP1_TX1+/ DSI1_D1+	NC	NA	-	NC.
S115	LVDS1_1-/ eDP1_TX1-/ DSI1_D1-	NC	NA	-	NC.
S116	LCD1_VDD_EN	NC	NA	-	NC.
S117	LVDS1_2+/ eDP1_TX2+/ DSI1_D2+	NC	NA	-	NC.
S118	LVDS1_2-/ eDP1_TX2-/ DSI1_D2-	NC	NA	-	NC.
S119	GND	GND	NA	Power	Ground.
S120	LVDS1_3+/ eDP1_TX3+/ DSI1_D3+	NC	NA	-	NC.
S121	LVDS1_3-/ eDP1_TX3-/ DSI1_D3-	NC	NA	-	NC.
S122	LCD1_BKLT_PWM	NC	NA	-	NC.
S123	RSVD8	NC	NA	-	NC.
S124	GND	GND	NA	Power	Ground.
S125	LVDS0_0+/ eDP0_TX0+/ DSI0_D0+	MIPI_DSI_DATA0_P	MIPI_DSI_D0_P/B17	I, MIPI	MIPI DSI Differential Data Lane 0 Positive to 5.5” AMOLED display.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S126	LVDS0_0-/ eDP0_TX0-/ DSI0_D0-	MIPI_DSI_DATA0_N	MIPI_DSI_D0_N/A17	I, MIPI	MIPI DSI Differential Data Lane 0 Negative to 5.5" AMOLED display.
S127	LCD0_BKLT_EN	GPIO_LCD0_1_EN(GPIO3_17)	GPIO3_17(NAND_WE_B)/K22	I, 1.8V CMOS	Display Backlight Enable.
S128	LVDS0_1+/ eDP0_TX1+/ DSI0_D1+	MIPI_DSI_DATA1_P	MIPI_DSI_D1_P/B16	I, MIPI	MIPI DSI Differential Data Lane 1 Positive to 5.5" AMOLED display.
S129	LVDS0_1-/ eDP0_TX1-/ DSI0_D1-	MIPI_DSI_DATA1_N	MIPI_DSI_D1_N/A16	I, MIPI	MIPI DSI Differential Data Lane 1 Negative to 5.5" AMOLED display.
S130	GND	GND	NA	Power	Ground.
S131	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSI_DATA2_P	MIPI_DSI_D2_P/B18	I, MIPI	MIPI DSI Differential Data Lane 2 Positive to 5.5" AMOLED display.
S132	LVDS0_2-/ eDP0_TX2-/ DSI0_D2-	MIPI_DSI_DATA2_N	MIPI_DSI_D2_N/A18	I, MIPI	MIPI DSI Differential Data Lane 2 Negative to 5.5" AMOLED display.
S133	LCD0_VDD_EN	GPIO_LCD0_VDD_EN(GPIO3_18)	GPIO3_18(NAND_WP_B)/K21	I, 1.8V CMOS	Display Power Enable.
S134	LVDS0_CK+/ eDP0_AUX+/ DSI0_CLK+	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P/ D16	I, MIPI	MIPI DSI Differential Clock Positive to 5.5" AMOLED display.
S135	LVDS0_CK-/ eDP0_AUX-/ DSI0_CLK-	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N/ C16	I, MIPI	MIPI DSI Differential Clock Negative to 5.5" AMOLED display.
S136	GND	GND	NA	Power	Ground.
S137	LVDS0_3+/ eDP0_TX3+/ DSI0_D3+	MIPI_DSI_DATA3_P	MIPI_DSI_D3_P/ B15	I, MIPI	MIPI DSI Differential Data Lane 3 Positive to 5.5" AMOLED display.
S138	LVDS0_3-/ eDP0_TX3-/ DSI0_D3-	MIPI_DSI_DATA3_N	MIPI_DSI_D3_N/ A15	I, MIPI	MIPI DSI Differential Data Lane 3 Negative to 5.5" AMOLED display.
S139	I2C_LCD_CK	I2C4_SCL	I2C4_SCL/F8	I, 1.8V CMOS	I2C4 Clock.
S140	I2C_LCD_DAT	I2C4_SDA	I2C4_SDA/F9	IO, 1.8V CMOS	I2C4 Data.
S141	LCD0_BKLT_PWM	GPIO_LCD0_BL_PWM(GPIO1_14)	GPIO1_IO14/K7	I, 1.8V CMOS	Display Back Light Brightness control PWM.
S142	RSVD9	NC	NA	-	NC.
S143	GND	GND	NA	Power	Ground.
S144	eDP0_HPD	GPIO_WDT_OUT(GPIO1_02)	NA	-	NC.

Pin No.	SMARC MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S145	WDT_TIME_OUT#	GPIO_WDT_OUT(GPIO1_02)	GPIO1_IO02/R4	I, 1.8V CMOS	Watchdog Time Out Interrupt.
S146	PCIE_WAKE#	GPIO_PCIe_Wake(GPIO5_5)	SPDIF_EXT_CLK/E6	O, 3.3V CMOS	PCIe wake up interrupt to host.
S147	VDD_RTC	VDD_RTC	NA	O, 3V Power	RTC backup power. Connected to RTC battery holder.
S148	LID#	NC	NA	-	NC.
S149	SLEEP#	NC	NA	-	NC.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	O, 5V CMOS	Power bad indication.
S151	CHARGING#	NC	NA	-	NC.
S152	CHARGER_PRSNT#	NC	NA	-	NC.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	I, 1.8V CMOS	Carrier Standby
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	I, 1.8V CMOS	Carrier power enable.
S155	FORCE_RECOV#	FORCE_RECOV#	NA	O, 1.8V CMOS	Force Recovery.
S156	BATLOW#	NC	NA	-	NC.
S157	TEST#	TEST#	NA	I, 1.8V CMOS	Connected to 4bit DIP switch (SW6).
S158	GND	GND	NA	Power	Ground.

2.4 Serial Interface Features

2.4.1 Debug UART Port

The i.MX8M Q/QL/D SMARC carrier board supports debug interface through i.MX8M CPU's UART1 interface. This UART1 signals from SMARC MXM connector SER3 port is connected to UART to USB Convertor "FT232RQ" via 1.8V to 3.3V level Translator and to USB Micro AB Connector (J22). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

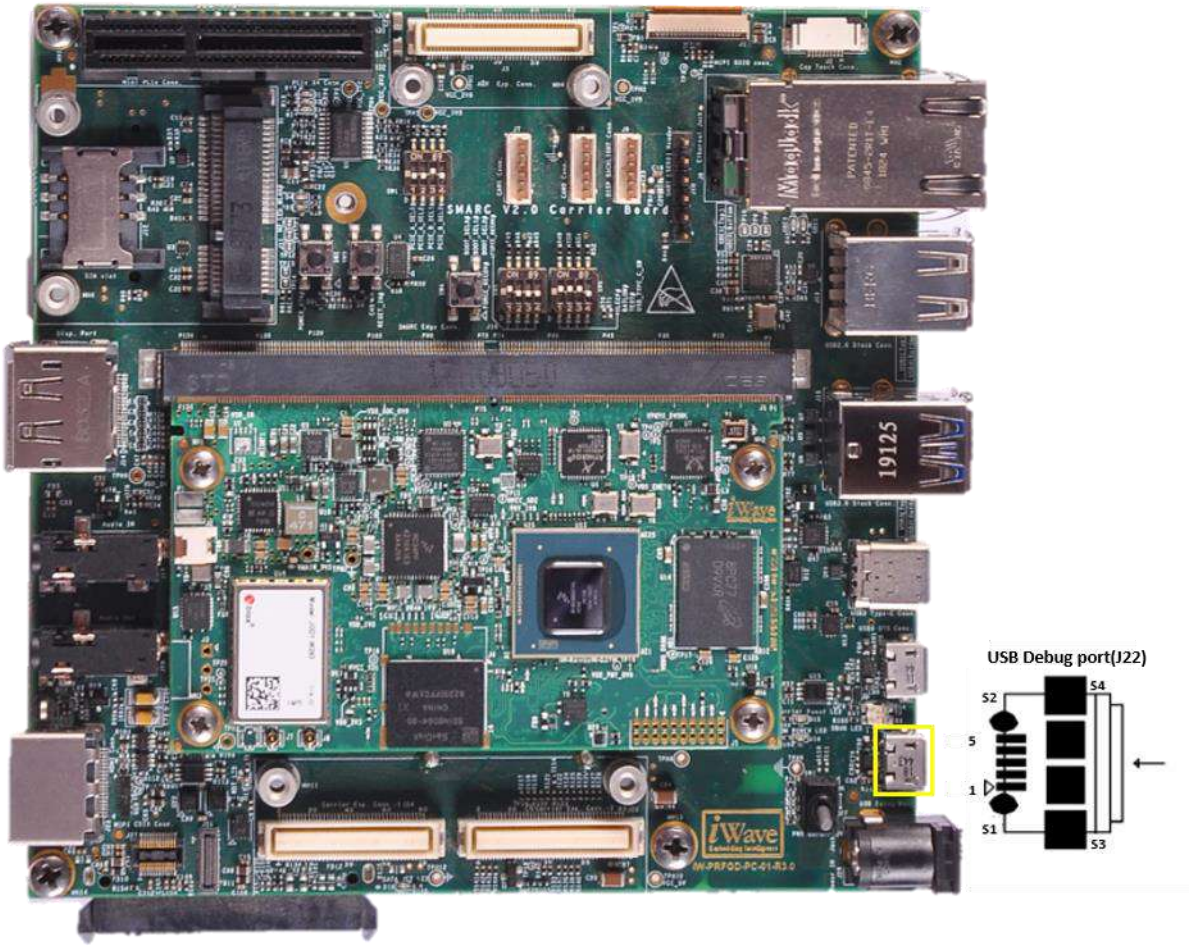


Figure 3: Debug UART

2.4.2 Data UART Header

The i.MX8M Q/QL/D SMARC carrier board supports full functional Data UART interface through i.MX8M CPU's UART2 interface. This UART2 signals from SMARC MXM connector is connected to 6pin Header (J10) via 1.8 to 3.3V volatge level translator. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

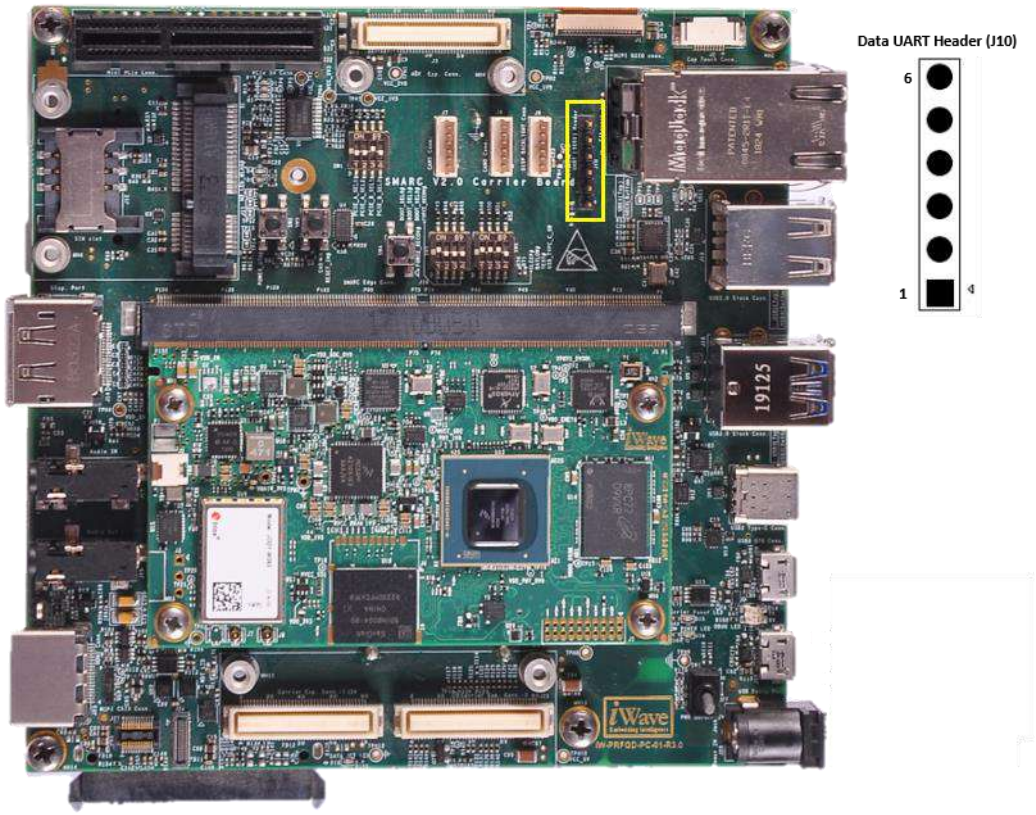


Figure 4: Data UART Header

Table 4: Data UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	UART2_CTS_B(UART4_RXD)	O, 3.3V CMOS	UART2 interface Clear to Send signal.
3	VCC_3V3	NC	O, 3.3V Power	NC. *Note: VCC_3V3 Optionally connected to this pin*
4	UART_RXD	UART2_RXD	I, 3.3V CMOS	UART2 interface Receive signal.
5	UART_TXD	UART2_TXD	O, 3.3V CMOS	UART2 interface Transmit signal.
6	UART_RTS#	UART2_RTS_B(UART4_TXD)	I, 3.3V CMOS	UART2 interface Ready to Send signal.

2.5 High Speed Interface Features

2.5.1 PCIe Port

The i.MX8M Q/QL/D SMARC Development platform by default supports one PCIe lane through i.MX8M CPU's PCIe1 interface and optionally supports one PCIe lane through i.MX8M CPU's PCIe2 interface, which are connected from PCIe Link A and Link B port respectively of SMARC MXM connector. Both PCIe Link A & B signals of SMARC MXM connector connected to separate 1:3 Multiplexer/Demultiplexer switch and the output of the Multiplexer/Demultiplexer switch are connected to PCIex4 connector, Mini PCIe connector and M.2 connector. The selection between the connector can be done by setting the 4-bit Board configuration switch (SW1) to appropriate position. PCIe Link B port can be used if PCIe2 interface supported i.MX8M SOM is used. By default, PCIe2 interface is used for on-SOM PCIe to Ethernet PHY/Controller.

PCIe A reference clock from SMARC MXM connector is connected to 1:2 output clock buffer and then connected to PCIex4 connector, Mini PCIe connector and M.2 connector for clock reference. Whereas PCIe B reference clock is optionally connected to M.2 Connector.

Refer Dip Switch (SW1) Settings in "Table 10: Board Configuration Switch" for more details on selecting PCIe connector. **PCIex4 Connector:** PCIeX4 connector (J4) is physically located at the top of the board as shown below

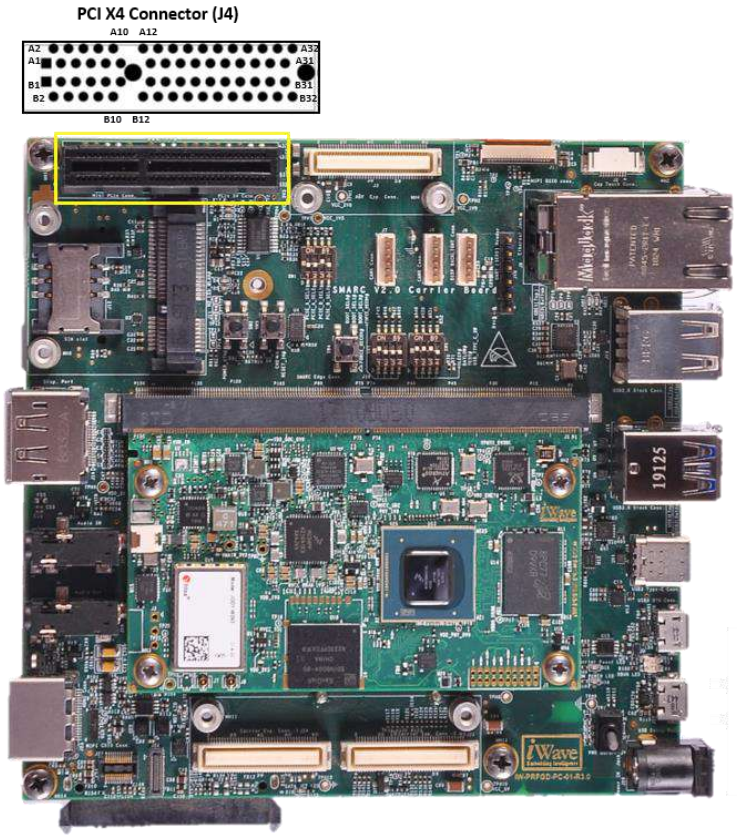


Figure 5: PCIex4 Connector

Table 5: PCIex4 Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	-	NC.
B5	SMCLK	I2C2_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	I2C2_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	GPIO_PCIE_RST(GPIO5_4)	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	GPIO_PCIe_Wake(GPIO5_5)	O, 3.3V CMOS	PCIe WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	REFCLK+	PCIe0_CLK+	O, PCIe	PCIe Clock positive.
B13	GND	GND	Power	Ground.
A14	REFCLK-	PCIe0_CLK-	O, PCIe	PCIe Clock negative.
B14	PETp0	PCIE1_TXP	O, PCIe	PCIe Port 0 Transmit pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE0_TX.*
A15	GND	GND	Power	Ground.
B15	PETn0	PCIE1_TXN	O, PCIe	PCIe Port 0 Transmit pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE0_TX.*
A16	PERp0	PCIE1_RXP	I, PCIe	PCIe Port 0 Receive pair positive. PCIe Port 0 Receive pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE0_RX.*
B16	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A17	PERn0	PCIE1_RXN	I, PCIe	PCIe Port 0 Receive pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE0_RX.*
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PETp1	PCIE2_TXP	O, PCIe	Optional, PCIe Port 1 Transmit pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE1_TX.*
A20	GND	GND	Power	Ground.
B20	PETn1	PCIE2_TXN	O, PCIe	Optional, PCIe Port 1 Transmit pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1_TX.*
A21	PERp1	PCIE2_RXP	I, PCIe	Optional, PCIe Port 1 Receive pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE1_RX.*
B21	GND	GND	Power	Ground.
A22	PERn1	PCIE2_RXN	I, PCIe	Optional, PCIe Port 1 Receive pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1_RX.*
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PETp2	NC	-	NC.
A24	GND	GND	Power	Ground.
B24	PETn2	NC	-	NC.
A25	PERp2	NC	-	NC.
B25	GND	GND	Power	Ground.
A26	PERn2	NC	-	NC.
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PETp3	NC	-	NC.
A28	GND	GND	Power	Ground.
B28	PETn3	NC	-	NC.
A29	PERp3	NC	-	NC.
B29	GND	GND	Power	Ground.
A30	PERn3	NC	-	NC.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSNT2#	NC	-	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A32	RSVD	NC	-	NC, Reserved Pin.
B32	GND	GND	Power	Ground.

Mini PCIe Connector: The i.MX8 SMARC carrier board supports Mini PCIe connector (J11) which is physically located at the top of the board as shown below.

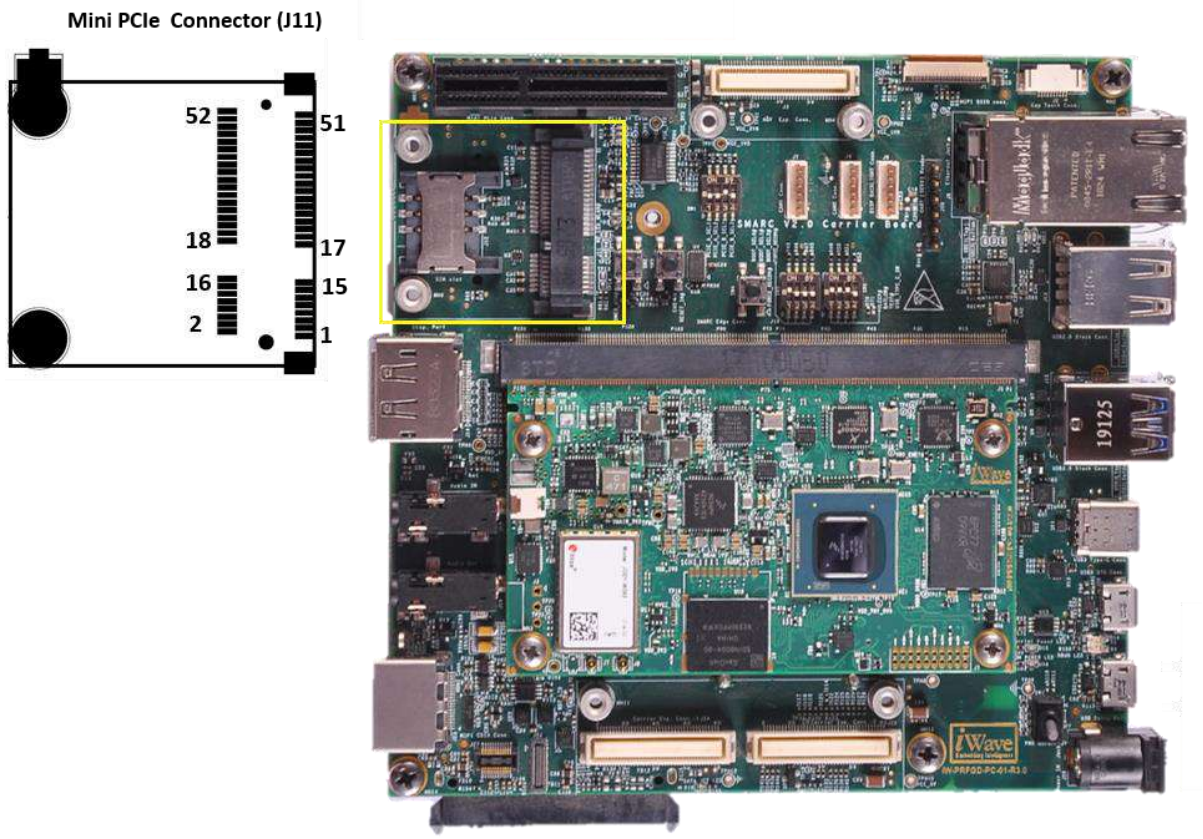


Figure 6: Mini PCIe Connector

Table 6: Mini-PCIe Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	WAKE#	GPIO_PCIe_Wake(GPIO5_5)	O, 3.3V CMOS	PCIe WAKE#.
2	+3.3V_aux	VCC_3V3	I, 3.3V Power	3.3V Supply Voltage.
3	COEX1	NC.	-	NC.
4	GND	GND	Power	Ground.
5	COEX2	NC.	-	NC.
6	1.5V	VCC_1V5_3G	I, 1.5V Power	1.5V Supply Voltage.
7	CLK_REQ#	CLK_REQ#	O, 3.3V CMOS	Used to enable Clock.
8	UIM_PWR	VSIM_3V	O,3V Power	3V SIM Supply Voltage.
9	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
10	UIM_DATA	UICC_DATA	IO, UIM	SIM Card data.
11	REFCLK-	PCIe1_CLK+	O, PCIe	PCIe Clock positive.
12	UIM_CLK	UICC_CLK	O, UIM	SIM Card clock.
13	REFCLK+	PCIe1_CLK-	O, PCIe	PCIe Clock negative.
14	UIM_RESET	UICC_RESET	O, UIM	Reset out for SIM
15	GND	GND	Power	Ground.
16	UIM_VPP	VPP_SIM	O, UIM	UIM Supply Voltage.
17	RESERVED	NC.	-	NC.
18	GND	GND	Power	Ground.
19	RESERVED	NC.	-	NC.
20	W_DISABLE#	SMARC_GPIO_10(GPIO1_07)	O, 3.3V CMOS	Wireless Disable.
21	GND	GND	Power	Ground.
22	PERST#	GPIO_PCIE_RST(GPIO5_4)	O, 3.3V CMOS	PCIe Reset.
23	PCIE0_RX-	PCIE1_RXN/PCIE2_RXN	I, PCIe	PCIe Port0 Receive pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_RXN.*
24	+3.3V_aux	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
25	PCIE0_RX+	PCIE1_RXP/PCIE2_RXP	I, PCIe	PCIe Port0 Receive pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_RXN.*
26	GND	GND	Power	Ground.
27	GND	GND	Power	Ground.
28	1.5V	VCC_1V5_3G	O, 1.5V Power	1.5V Supply Voltage.
29	GND	GND	Power	Ground.
30	SMB_CLK	I2C2_SCL	O, 3.3V CMOS	SMB Clock.
31	PCIE0_TX-	PCIE1_TXN/PCIE2_TXN	O, PCIe	PCIe Port0 Transmit pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_TXN.*
32	SMB_DATA	I2C2_SDA	IO, 3.3V CMOS	SMB DATA.
33	PCIE0_TX+	PCIE1_TXP/PCIE2_TXP	O, PCIe	PCIe Port0 Transmit pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_TXP.*
34	GND	GND	Power	Ground.
35	GND	GND	Power	Ground.
36	USB_D-	USB_HUBOUT2_DM	IO, USB HS	USB Data negative
37	GND	GND	Power	Ground.
38	USB_D+	USB_HUBOUT2_DP.	IO, USB HS	USB Data Positive
39	+3.3V_aux	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
40	GND	GND	Power	Ground.
41	+3.3V_aux	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
42	LED_WWAN#	LED_WWAN#	O, 3.3V CMOS	Connected to D4 Green LED cathode.
43	GND	GND	Power	Ground.
44	LED_WLAN#	LED_WLAN#	O, 3.3V CMOS	Connected to D5 Green LED cathode.
45	RESERVED	NC.	-	NC.
46	LED_WPAN#	LED_WPAN#	O, 3.3V CMOS	Connected to D3 Green LED cathode.
47	RESERVED	NC.	-	NC.
48	1.5V	VCC_1V5_SIM	O, 1.5V Power	1.5V Supply Voltage.
49	RESERVED	NC.	-	NC.
50	GND	GND	Power	Ground.
51	RESERVED	NC.	-	NC.
52	+3.3V_aux	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.

M.2 Connector: The i.MX8 SMARC carrier board supports M.2 Key-E Connector (J31) and is placed at the bottom side of the board. SPI, SDIO, PCIe, I2S, I2C, and UART interface are optionally supported over M.2 Connector.

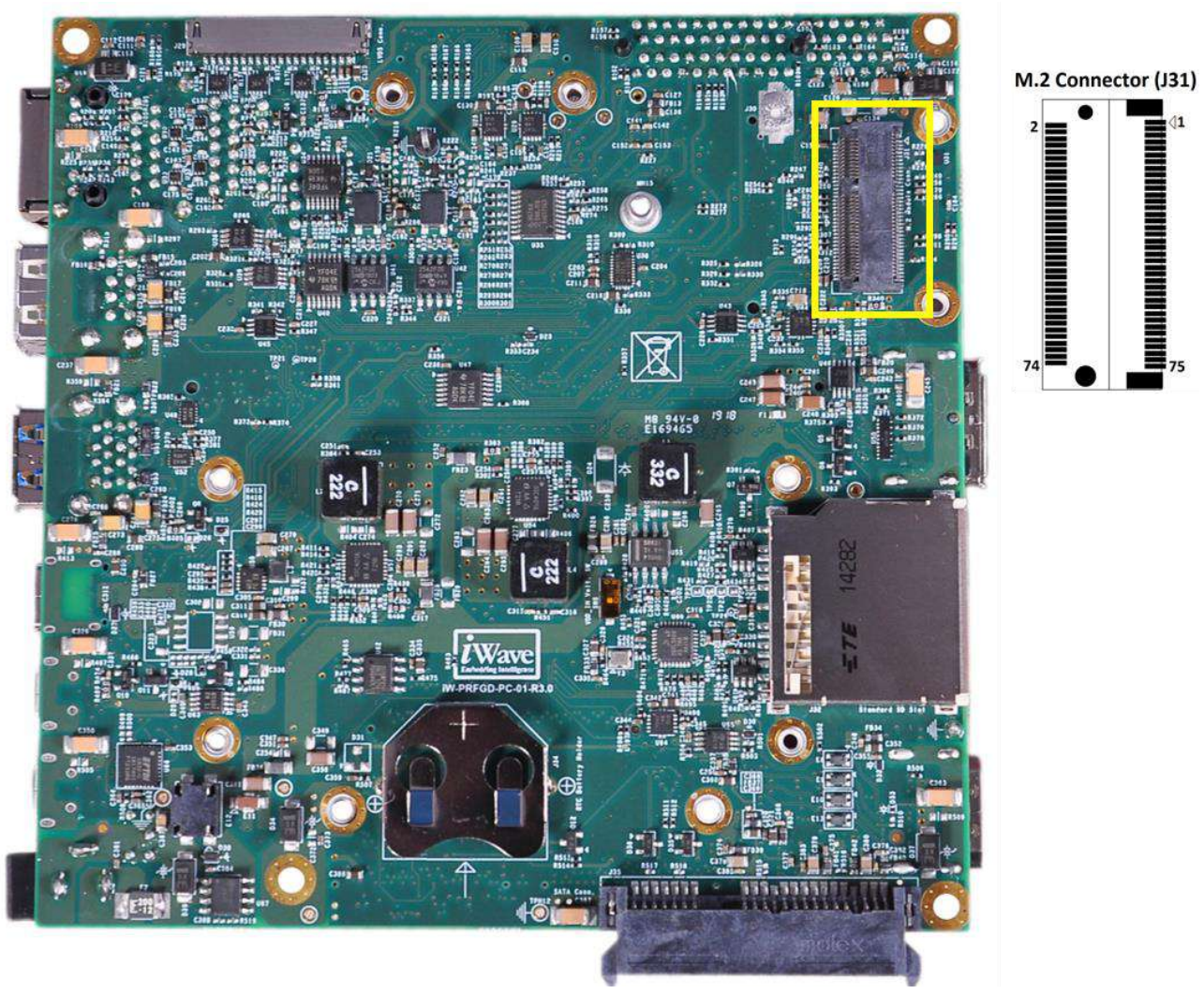


Figure 7: M.2 Connector

Refer below table for M.2 connector pinout details.

Table 7: M.2 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	USB_DP	USB_HUB4OUT_DP	NA	USB Data Positive
4	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
5	USB_DM	USB_HUB4OUT_DM	NA	USB Data Negative
6	LED_WLAN#	M2_LED_WLAN#	O, 3.3V CMOS	Connected to D5 Green LED cathode.
7	GND	GND	Power	Ground.
8	I2S SCK	M2_MI2S_2_SCK	O, 1.8V CMOS	M.2 Module I2S Clock *Note: This pin is connected from SMARC Edge connector S53rd pin for I2S2_CK. This pin is also connected to A&V Expansion Conn connector (J3) 30th pin through resistor.*
9	SDIO CLK	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
10	I2S WS	M2_MI2S_2_WS	O, 1.8V CMOS	M.2 Module I2S Word Select. *Note: This pin is connected from SMARC Edge connector S50th pin for I2S2_LRCK. This pin is also connected to A&V Expansion Conn connector (J3) 36th pin through resistor.*
11	SDIO CMD	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
12	I2S SD_IN	M2_MI2S_2_D0	IO, 1.8V CMOS	M.2 Module I2S SD_IN *Note: This pin is connected from SMARC Edge connector S51st pin for I2S2_SDOUT. This pin is also connected to A&V Expansion Conn connector (J3) 32nd pin through resistor.*
13	SDIO DATA0	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
14	I2S SD_OUT	M2_MI2S_2_D1	IO, 1.8V CMOS	M.2 Module I2S SD_OUT *Note: This pin is connected from SMARC Edge connector S52nd pin for I2S2_SDIN. This pin is also connected to A&V*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Expansion Conn connector (J3) 34th pin through resistor.
15	SDIO DATA1	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
16	LED_BT#	M2_LED_BT#	O, 3.3V CMOS	Connected to D4 Green LED cathode.
17	SDIO DATA2	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
18	GND	GND	Power	Ground.
19	SDIO DATA3	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
20	CB_PWR_ON	NC	NA	NC
21	SDIO WAKE#	NC	NA	NC. *Note: To support SD interface refer* ***Note-1***
22	UART0 RXD	SER2_RX	I, 1.8V CMOS	NC. *Note: M.2 UART Receive Signal. This signal is Connected to SMARC Edge P137th pin for SER2_RX. SER2 is optional in default SOM Configuration.*
23	SDIO RESET#	SDIO_RST#	O, 1.8V CMOS	M.2 SDIO Reset.
24	NC1	NA	NA	NC.
25	NC2	NA	NA	NC.
26	NC3	NA	NA	NC.
27	NC4	NA	NA	NC.
28	NC5	NA	NA	NC.
29	NC6	NA	NA	NC.
30	NC7	NA	NA	NC.
31	NC8	NA	NA	NC.
32	UART0 TXD	SER2_TX	O, 1.8V CMOS	NC. *Note: M.2 UART Transmit Signal. This signal is Connected to SMARC Edge P136th pin for SER2_TX. SER2 is optional in default SOM Configuration.*
33	GND	GND	Power	Ground.
34	UART0 CTS	SER2_CTS#	I, 1.8V CMOS	NC. *Note: M.2 UART Clear to Send signal. This signal is Connected to SMARC Edge P139th pin for SER2_CTS#. SER2 is optional in default SOM Configuration.*
35	PETp0	PCIE1_TXP/PCIE2_TXP	O, PCIe	PCIe Port 0/1 Transmit pair positive.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Note: Refer SW1 setting from Table 10 to support PCIE1/2_TXP
36	UART0 RTS	SER2_RTS#	O, 1.8V CMOS	NC. *Note: M.2 UART Ready to Send signal. This signal is Connected to SMARC Edge P138th pin for SER2_RTS#. SER2 is optional in default SOM Configuration.*
37	PETn0	PCIE1_TXN/PCIE2_TXN	O, PCIe	PCIe Port 0/1 Transmit pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_TXN*
38	GPIO0	NA	IO, 3.3V CMOS	NC.
39	GND	GND	Power	Ground.
40	GPIO1	NA	IO, 3.3V CMOS	NC.
41	PERp0	PCIE1_RXP/PCIE2_RXP	I, PCIe	PCIe Port 0/1 Receive pair positive. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_RXP*
42	GPIO2	NA	IO, 3.3V CMOS	NC.
43	PERn0	PCIE1_RXN/PCIE2_RXN	I, PCIe	PCIe Port 0/1 Receive pair negative. *Note: Refer SW1 setting from Table 10 to support PCIE1/2_RXN*
44	COEX3(LTE_ACTIVE)	TP7	NA	Connected to Test Point.
45	GND	GND	Power	Ground.
46	COEX2(LTE_PRI)	TP12	NA	Connected to Test Point.
47	REFCLK+	REFCLK+	I, DIFF	100MHz Reference Clock for PCIe.
48	COEX2(LTEE_SYNC)	TP11	NA	Connected to Test Point
49	REFCLK-	REFCLK-	I DIFF	100MHz Reference Clock for PCIe.
50	SUSCLK(32KHz)	NA	NA	NC
51	GND	GND	Power	Ground.
52	PERST#	PCIe_A_RST#	O, 3.3V CMOS	M.2 PCIe Reset.
53	CLKREQ#	CLKREQ#	O, 3.3V CMOS	PCIe Reference Clock Request *Note: This pin should have Pull Down on Module to enable to CLK.*
54	BT_DISABLE#	SMARC_GPIO_10(GPIO1_07)	O, 3.3V CMOS	BT_DISABLE# *Note: This Pin is Connected to SMARC Edge P118th pin* SMARC_GPIO_10*. Also shared with W_DISABLE#*
55	PEWAKE#	PEWAKE#	O, 3.3V CMOS	NC Note: by default, connected to Mini PCIe connector
56	W_DISABLE#	SMARC_GPIO_10(GPIO1_07)	O, 3.3V CMOS	W_DISABLE. *This Pin is Connected to SMARC Edge P118th pin* SMARC_GPIO_10*.*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				Also shared with BT_DISABLE#
57	GND	GND	Power	Ground.
58	I2C_DATA	I2C2_SDA	IO, 3.3V CMOS	I2C Data Signal. *Note: This Pin is Connected to SMARC Edge S49th pin I2C_GP_DAT via voltage level Translator.*
59	ADC4/ GPIO14	NA	NA	NC
60	I2C_CLK	I2C2_SCL	O, 3.3V CMOS	I2C Clock Signal. *Note: This Pin is Connected to SMARC Edge S48th pin I2C_GP_CK via voltage level Translator.*
61	ADC5 / GPIO15	NA	NA	NC.
62	SPI0_MOSI	ESPI_IO_0_3V3	O, 3.3V CMOS	SPI Master Out Slave In. *Note: This Pin is Connected to SMARC Edge P58th pin ESPI_IO_0 via voltage level Translator.*
63	GND	GND	Power	Ground.
64	SPI0_MISO	ESPI_IO_1_3V3	I, 3.3V CMOS	SPI Master in Slave Out. *Note: This Pin is Connected to SMARC Edge P57th pin ESPI_IO_1 via voltage level Translator.*
65	VBAT	NC	O, 3.3V Power	NC. *Note: Optionally connected to VDD_RTC*
66	SPI0_CLK	ESPI_CK_3V3	I, 3.3V CMOS	SPI Clock. *Note: This Pin is Connected to SMARC Edge P56th pin ESPI_CK via voltage level Translator*
67	Backup#	NC	I, 3.3V CMOS	NC
68	SPI0_CS0#	ESPI_CS0_N_3V3	O, 3.3V CMOS	SPI Chip Select0. *Note: This Pin is Connected to SMARC Edge P54th pin ESPI_CS0# via voltage level Translator*
69	GND	GND	Power	Ground.
70	SPI0_CS1#	ESPI_CS1_N_3V3	O, 3.3V CMOS	SPI Chip Select1. *Note: This Pin is Connected to SMARC Edge P55th pin ESPI_CS1# via voltage level Translator*
71	RESET_IN#	PCIe_A_RST#	I, 3.3V CMOS	Reset Input. *Note: This pin is connected to SMARC Edge P75th pin for PCIe_A_RST#*
72	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
73	Wake#	NA	NA	NC
74	VCC	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
75	GND	GND	Power	Ground.

Note-1: *SMARC SDIO interface is directly connected to Standard SD and optionally connected to M.2 Connector. SMARC SDIO interface optional in default SOM Configuration. To Support SDIO interface at M.2 connector contact iWave Support team.*

2.5.2 USB3.0 OTG as Device/Host Port

The i.MX8M Q/QL/D SMARC carrier board supports one USB3.0 OTG through i.MX8M CPU's USB1 interface which is connected from USB3 port of SMARC MXM connector. USB3.0 signals of USB3 port of SMARC MXM connector is connected to 1:2 data switch and then one output is connected to USB Type C connector (J18) for OTG as Device or Host support & other one to top port of dual stack USB3.0 TypeA connector (J15) for OTG as Host only support.

The selection between USB Type C connector and top port of dual stack USB3.0 TypeA connector can be done by setting the 4th bit of Board configuration switch (SW6) to appropriate position. If the 4th bit of Board configuration switch (SW6) is set to OFF position, then USB3 port of SMARC MXM connector is connected to USB Type C connector. If the 4th bit of Board configuration switch (SW6) is set to ON position, then USB3 port of SMARC MXM connector is connected to top port of dual stack USB3.0 TypeA connector. Also USB2.0 signals of USB3 Port of SMARC MXM connector is connected to both these connectors.

To support double-way plug in on USB TypeC connector, USB3 signals are connected to FUSB340TMX USB3.0 switch and then connected to USB Type C connector. This USB3.0 switch port connection to Type C connector top or bottom is controlled through GPIO4 (P112nd pin) of the SMARC MXM connector.

The VBUS power of USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin (P74th) of SMARC MXM connector USB3 port. This USB3.0 connector is physically located at the top of the board as shown below.

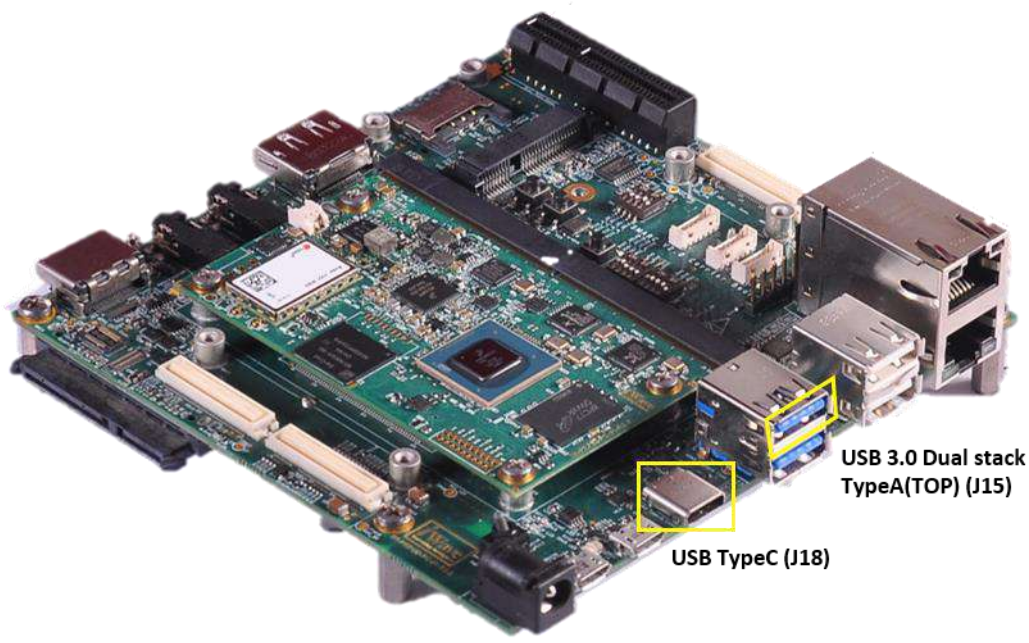


Figure 8: USB3.0 OTG Port

2.5.3 USB3.0 Host Port

The i.MX8M Q/QL/D SMARC carrier board supports one USB3.0 Host through i.MX8M CPU's USB2 interface which is connected from USB2 port of SMARC MXM connector. USB3.0 signals of USB2 port of SMARC MXM connector is directly connected to bottom port of dual stack USB3.0 TypeA connector (J15). Also USB2.0 signals of USB2 Port of SMARC MXM connector is connected to this connector.

The VBUS power of this USB3.0 host connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin (P71st) of SMARC MXM connector USB2 port. This USB3.0 connector is physically located at the top of the board as shown below.

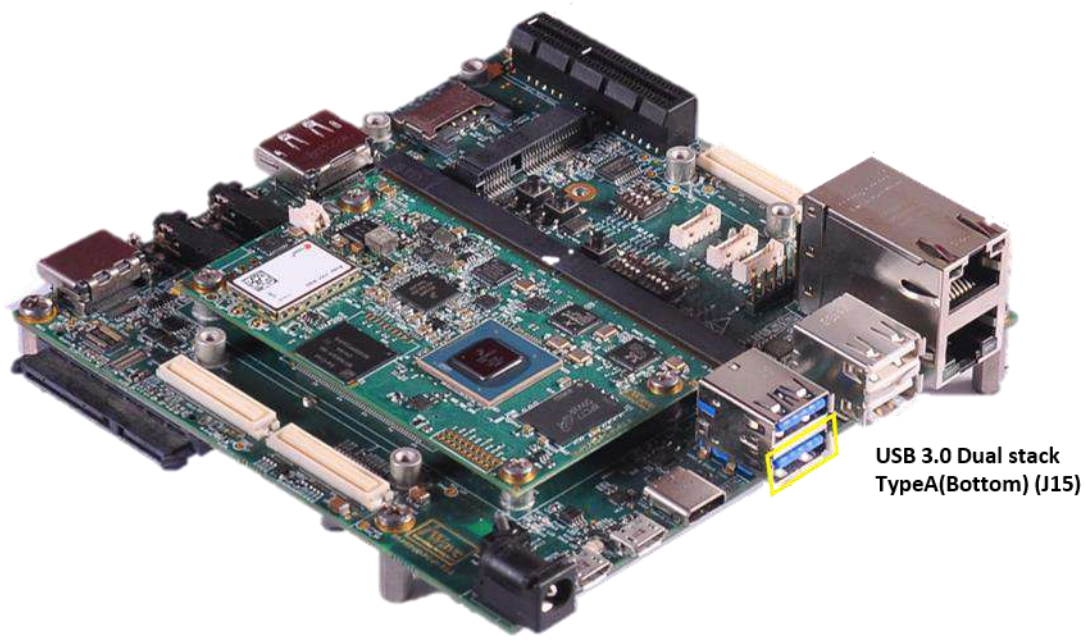


Figure 9: USB3.0 Host Port

2.6 Communication Interface Features

2.6.1 Dual Gigabit Ethernet Ports

The i.MX8M Q/QL/D SMARC carrier board supports Dual Ethernet Ports through GBE0 and GBE1 ports of SMARC MXM connector which supports 10/100/1000Mbps Ethernet. The GBE0 and GBE1 signals from SMARC MXM connector are directly connected to Dual Stack RJ45 Magjack (J6) Top & Bottom connector respectively. Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

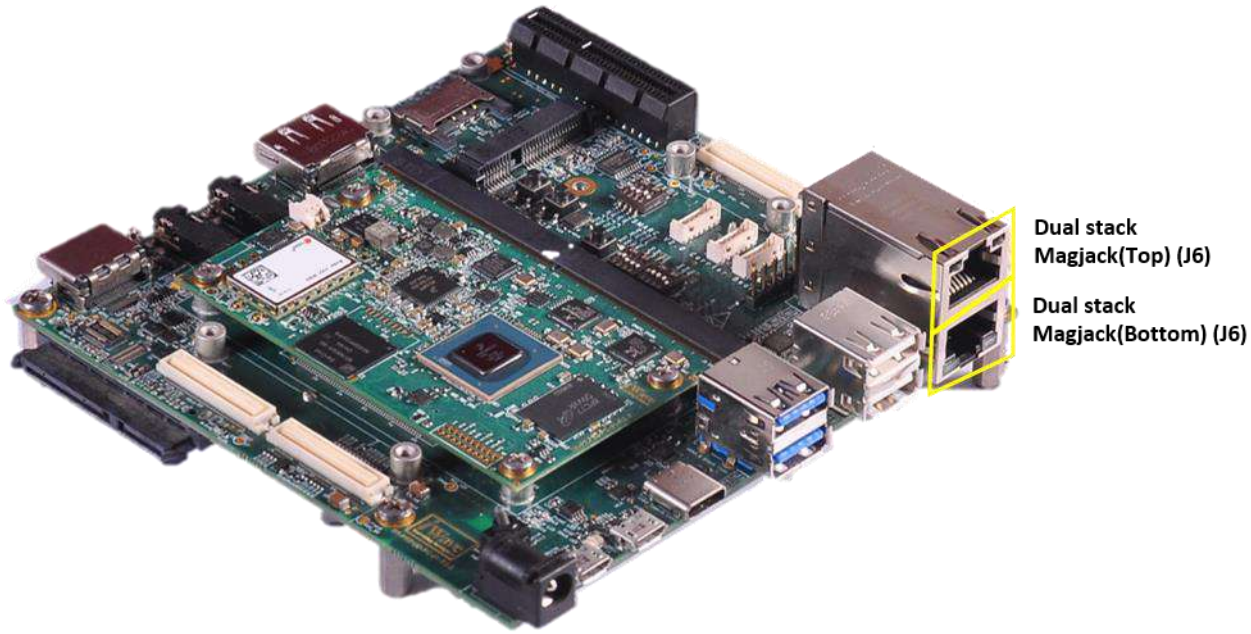


Figure 10: Dual Stack RJ45 Magjack

2.6.2 USB2.0 Host Port

The i.MX8M Q/QL/D SMARC carrier board supports additional two USB2.0 Host interface through USB1 and USB4 ports of SMARC MXM connector. USB1 signals from the SMARC MXM connector is connected to 2 port USB Hub in carrier board and one port is directly connected to bottom port of dual stack USB2.0 TypeA connector (J13) and other port is connected to Mini-PCIe connector. USB4 signals from the SMARC MXM connector is directly connected to top port of dual stack USB2.0 TypeA connector (J13).

The VBUS power of these USB2.0 connectors are connected through current limit power switch and limit is set as 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pins P67th & P76th of USB1 and USB4 ports respectively of SMARC MXM connector. This dual stack USB2.0 TypeA connector is physically located at the top of the board as shown below.

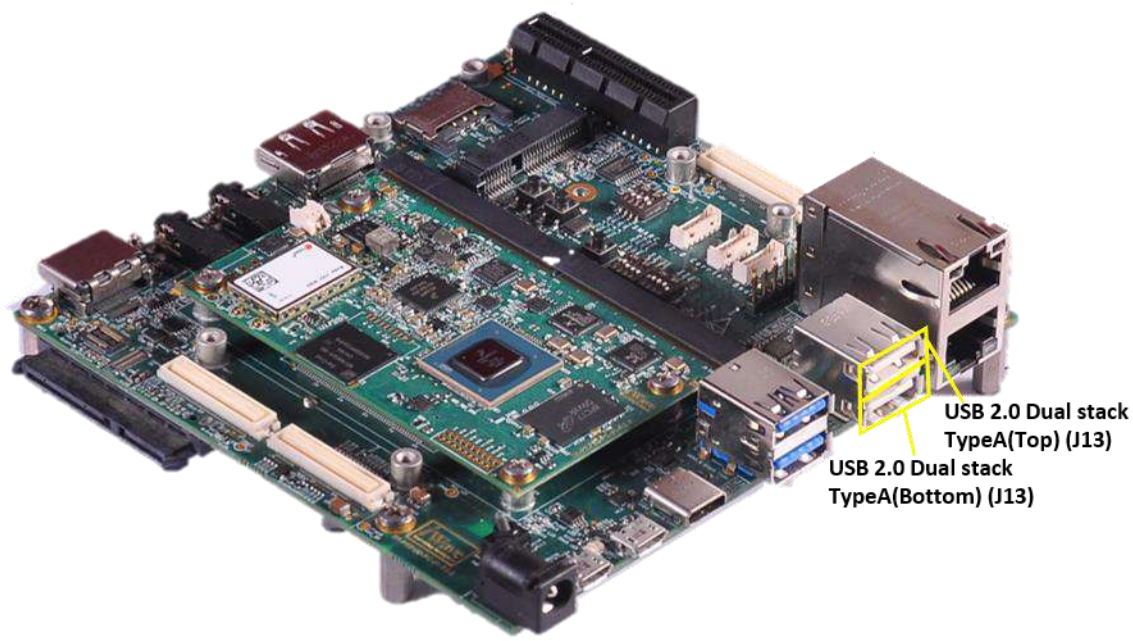


Figure 11: USB2.0 Host Port

2.6.3 SDIO Port (Optional)

The i.MX8M Q/QL/D SMARC carrier board supports SDIO interface through CPU's uSDHC2 interface. This uSDHC2 signals from SMARC MXM connector is connected to SD connector (J32) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR_EN pin (P37th) of SMARC MXM connector. This SD connector (J32) is physically located at the bottom of the board as shown below.

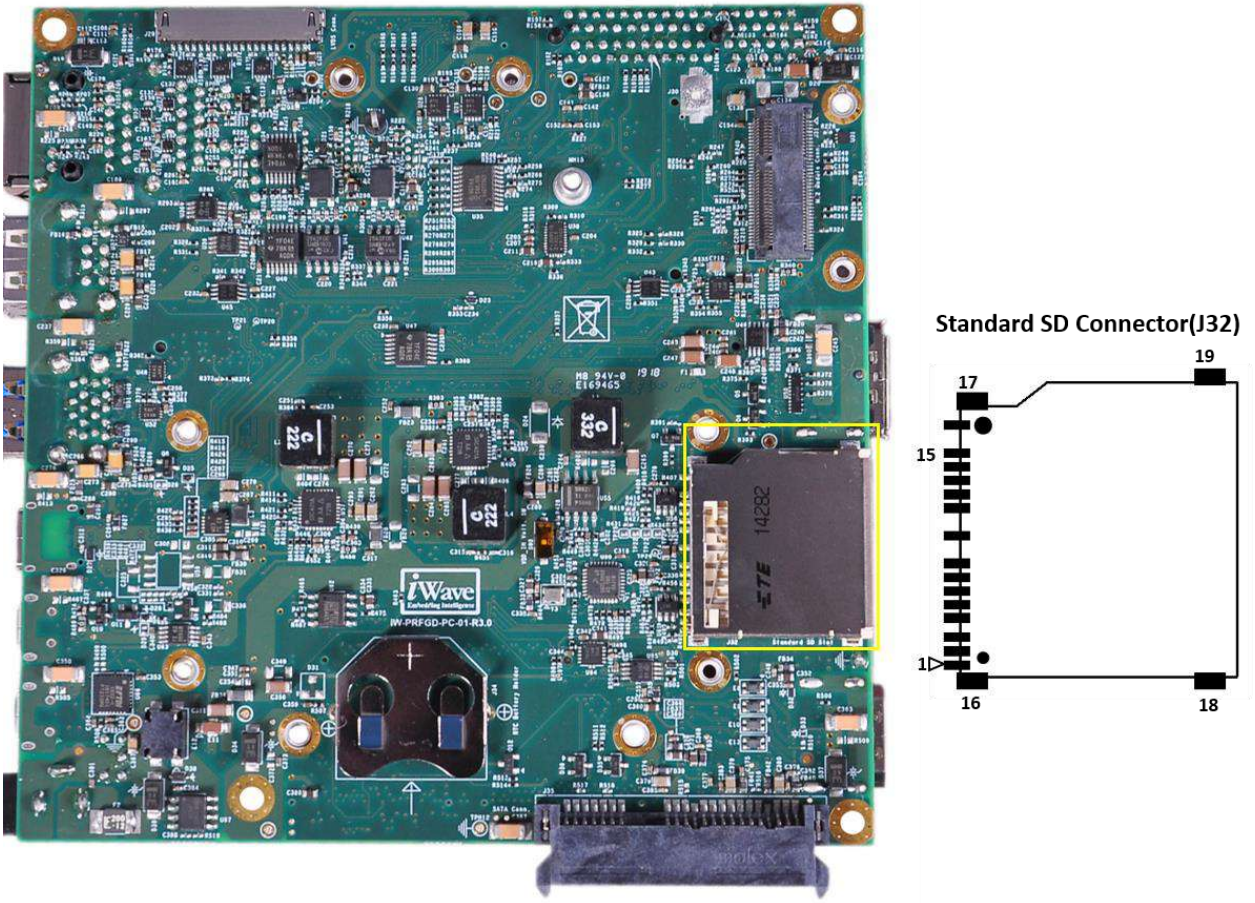


Figure 12: SDIO Port

2.7 Audio & Video Features

2.7.1 Audio In and Out Ports

The i.MX8M Q/QL/D SMARC carrier board supports Audio In and Out through CPU's SAI2 interface which can support I2S format. This four wire I2S signals from SMARC MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input through 3.5mm audio Jack J19 and J17 correspondingly. Also Headphone detect and Mic detect is supported through GPIO8 (P116th) & GPIO11 (P119th) pin of SMARC MXM connector correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

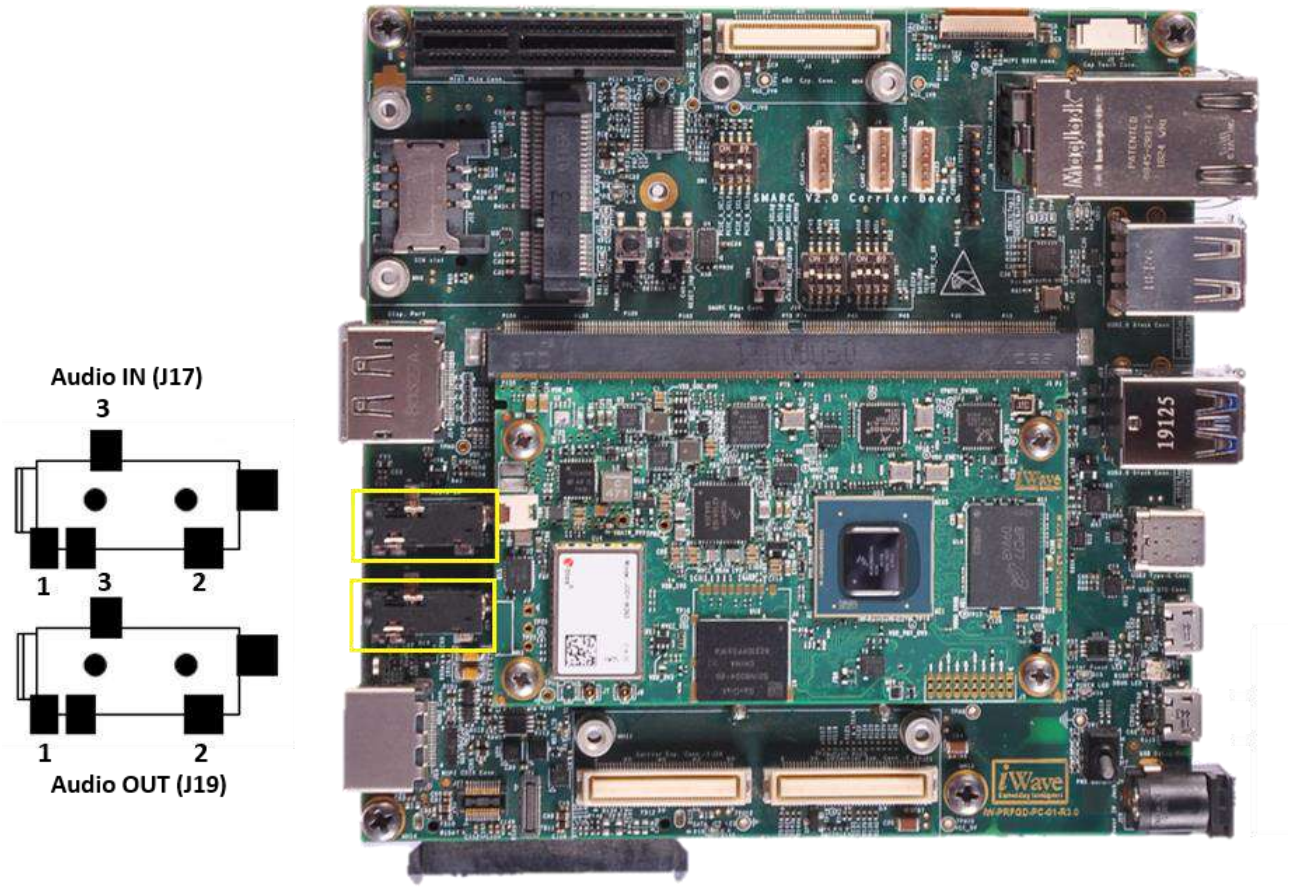


Figure 13: Audio In and Out Ports

2.7.2 MIPI DSI Display

The i.MX8M Q/QL/D SMARC carrier board supports MIPI DSI display connector to support 5.5inch, 1080X1920 resolution supported AMOLED Display G1548FH107GG" (from i-excellence) with Capacitive touch panel. i.MX8M CPU's MIPI DSI0 4 lane interface is used for display interface and connected to this display connector.

Also i.MX8M CPU's I2C4 interface is connected to this connector for touch interface and its touch interrupt output is connected to GPIO7 pin (P115th) of SMARC MXM connector. The main power to this display connector is 3.3V and its on/off is controlled using LCD0_VDD_EN pin (S133rd) of SMARC MXM connector. This MIPI DSI display connector (J1) is physically located at the top of board as shown below.

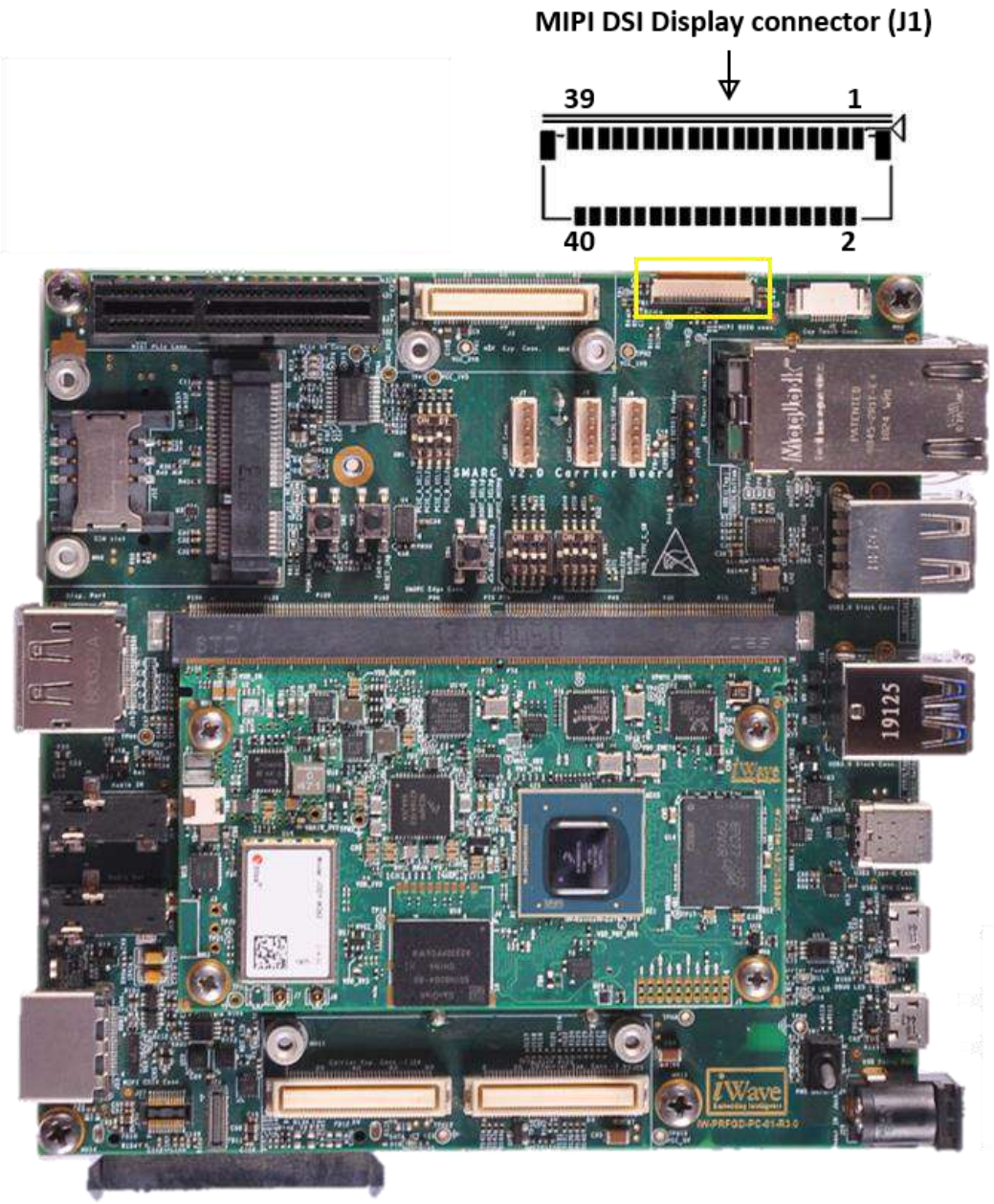


Figure 14: MIPI DSI Display Connector

Table 8: MIPI DSI Display Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND	GND	Power	Ground.
2	GND	GND	Power	Ground.
3	GND	GND	Power	Ground.
4	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	VBAT	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
9	GND	GND	Power	Ground.
10	OTPV	NC	NA	NA.
11	NC1	NC	NA	NA.
12	GND	GND	Power	Ground.
13	D3P	MIPI_DSI_DATA3_P	O, MIPI	MIPI_DSI DATA Lane3 Positive
14	D3N	MIPI_DSI_DATA3_N	O, MIPI	MIPI_DSI DATA Lane3 Negative
15	GND	GND	Power	Ground.
16	D0P	MIPI_DSI_DATA0_P	O, MIPI	MIPI_DSI DATA Lane0 Positive
17	D0N	MIPI_DSI_DATA0_N	O, MIPI	MIPI_DSI DATA Lane0 Negative
18	GND	GND	Power	Ground.
19	DKP	MIPI_DSI_CLK_P	O, MIPI	MIPI_DSI Clock Positive
20	DKN	MIPI_DSI_CLK_N	O, MIPI	MIPI_DSI Clock Negative
21	GND	GND	Power	Ground.
22	D1P	MIPI_DSI_DATA1_P	O, MIPI	MIPI_DSI DATA Lane1 Positive
23	D1N	MIPI_DSI_DATA1_N	O, MIPI	MIPI_DSI DATA Lane1 Negative
24	GND	GND	Power	Ground.
25	D2P	MIPI_DSI_DATA2_P	O, MIPI	MIPI_DSI DATA Lane2 Positive
26	D2N	MIPI_DSI_DATA2_N	O, MIPI	MIPI_DSI DATA Lane2 Negative
27	GND	GND	Power	Ground.
28	RESX	SMARC_GPIO_9(GPIO1_03)	O, 1.8V CMOS	RESET
29	VDDIO	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Display IO Circuit.
30	VCI	VCI_1	O, 3.3V Power	3.3V Supply voltage for Display Circuit.
31	NC2	NC	NA	NA.
32	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
33	TP_AVDD_3P3V	VCC_3V3_TFT0	O, 3.3V Power	3.3V Supply voltage for Touch driver Circuit.
34	TP_DVDD_1P8V	VCC_1V8	O, 1.8V Power	1.8V Supply voltage for Touch IO Circuit.
35	TP_SDA	I2C4_SDA	IO, 1.8V CMOS	I2C Data for Capacitive Touch
36	TP_SCL	I2C4_SCL	O, 1,8V CMOS	I2C Clock for Capacitive Touch
37	TP_RESET	GPIO_RESET_OUT(GPIO3_25)	O, 1.8V CMOS	RESET for Capacitive Touch
38	TP_INT	SMARC_GPIO_7(GPIO1_06)	I, 1.8V CMOS	Interrupt from Capacitive Touch
39	GND	GND	Power	Ground.

2.7.3 HDMI/DP Port

The i.MX8M Q/QL/D SMARC carrier board supports HDMI audio/video out through i.MX8M CPU's HDMI 2.0a interface. HDMI interface signals from the SMARC MXM connector is connected to standard HDMI connector and supports up to 600Mhz pixel clock and up to 4k2k at 60Hz resolution. This HDMI output connector (J23) is physically located on top of the board as shown below.

The i.MX8M Q/QL/D SMARC carrier board supports Display Port (DP) through i.MX8M CPU's Display Port 1.3 interface. DP interface signals from the SMARC MXM connector is connected to standard Display Port connector and can be used if Display Port interface supported i.MX8M SOM is used. Since HDMI and Display Port are multiplexed on the same pins in i.MX8M CPU, either one interface only can be used at a time. Display Port connector (J14) is physically located on top of the board as shown below.

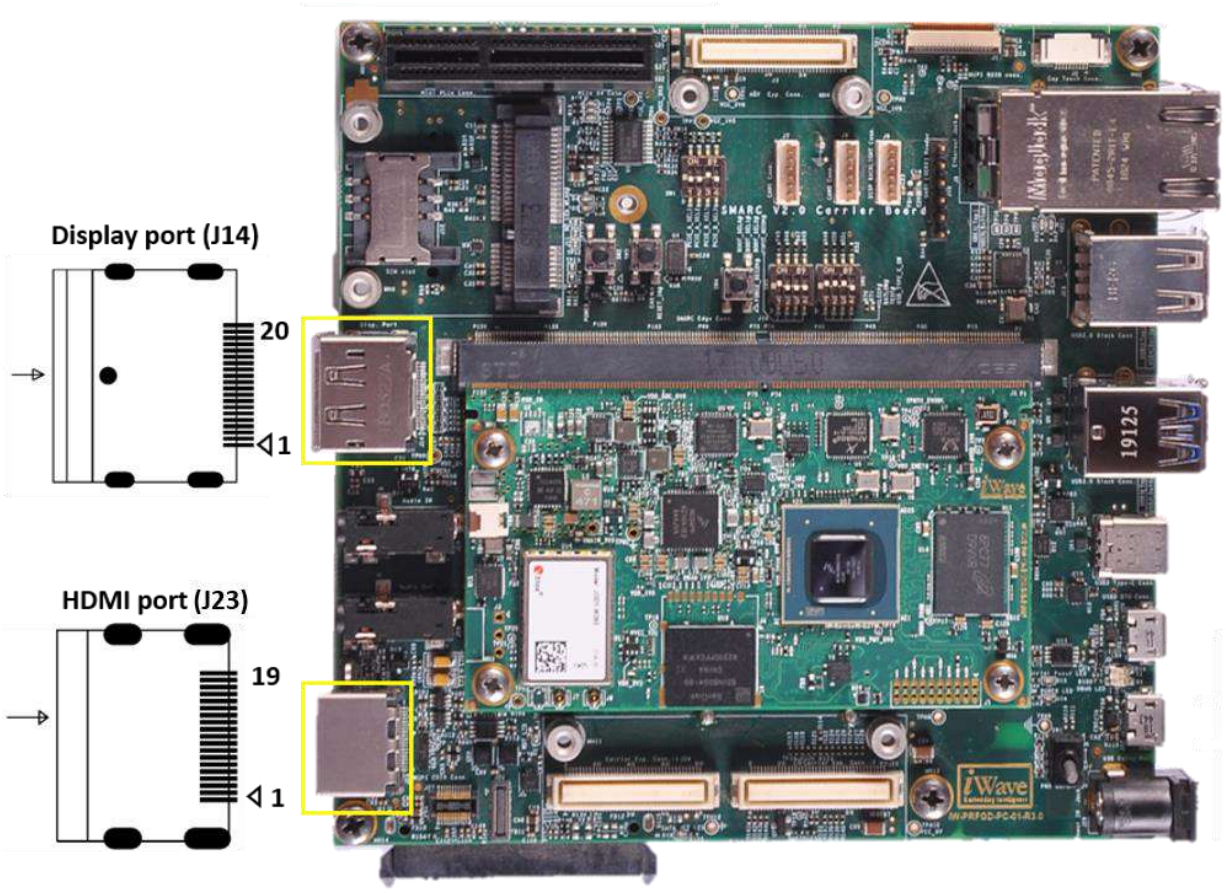


Figure 15: HDMI/DP Port

2.7.4 MIPI CSI Camera

The i.MX8M Q/QL/D SMARC carrier board supports OV5640 sensor based MIPI CSI camera which supports 5MP of resolution. i.MX8M Q/QL/D CPU's dual lane MIPI CSI0 interface from SMARC MXM connector is used for this Camera interface. This MIPI CSI camera connector (J27) is physically located on top of the board as shown below.

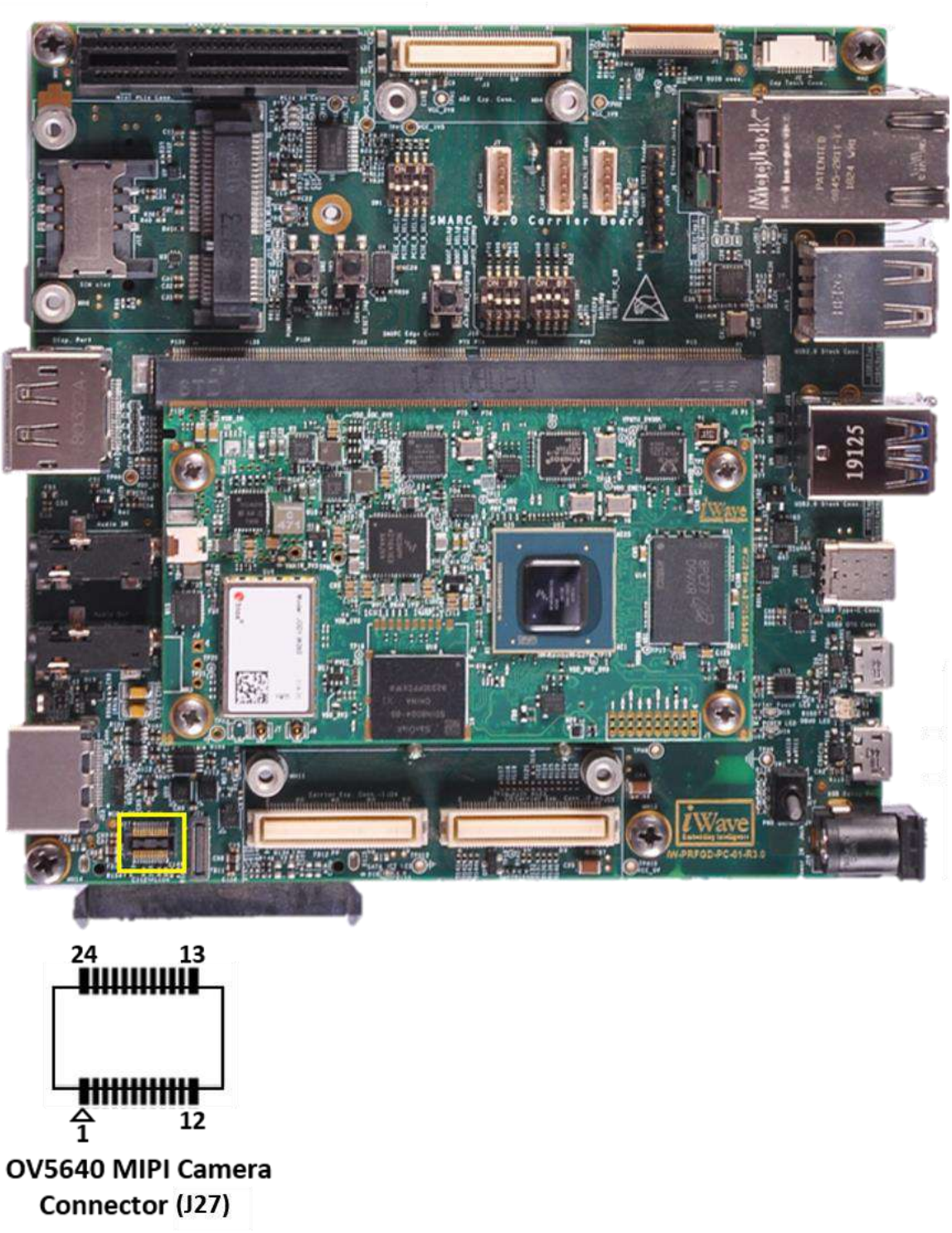


Figure 16: MIPI Camera Connector

Table 9: MIPI Camera Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	Strobe	NC	NA	NA
2	AGND	AGND	Power	Analog Ground.
3	SDA	I2C3_SDA	IO, 1.8V OD/ 4.7K PU	I2C3 Data for Camera
4	AVDD	AVDD	O, Power	2.8V Supply voltage
5	SCL	I2C3_SCL	O, 1.8V OD/ 4.7K PU	I2C3 Clock for Camera
6	RESET	SMARC_GPIO_2(GPIO1_15)	O, 1.8V CMOS	Reset Output from CPU GPIO.
7	NC	NC	NA	NA
8	PWDN	PWDN	O, 1.8V CMOS	Power Down Output
9	NC	NC	NA	NA
10	DVDD	DVDD	O, Power	1.2V Supply voltage
11	DOVDD	DOVDD	O, Power	1.8V Supply voltage
12	MDP1	MIPI_CSI1_DATA1_P	I, MIPI	MIPI_CSI DATA Lane1 Positive
13	XCLK	XCLK	O, CMOS	Reference Clock to Camera Module
14	MDN1	MIPI_CSI1_DATA1_N	O, MIPI	MIPI_CSI DATA Lane1 Negative
15	DGND	GND	Power	Ground.
16	MCP	MIPI_CSI1_CLK_P	I, MIPI	MIPI_CSI Clock Positive
17	NC	NC	NA	NA
18	MCN	MIPI_CSI1_CLK_N	I, MIPI	MIPI_CSI Clock Negative
19	NC	NC	NA	NA
20	MDP0	MIPI_CSI1_DATA0_P	I, MIPI	MIPI_CSI DATA Lane0 Positive
21	NC	NC	NA	NA
22	MDN0	MIPI_CSI1_DATA0_N	I, MIPI	MIPI_CSI DATA Lane0 Negative
23	AF-VCC	AF-VCC	O, Power	2.8V Supply voltage
24	AF-AGND	AF-AGND	Power	AF Ground.

2.8 Additional Features

2.8.1 RTC Coin Cell Holder

The i.MX8M Q/QL/D SMARC carrier board supports Coin Cell Holder to connect “2032” series coin cell. This coin cell voltage is connected to SMARC MXM connector VDD_RTC pin (S147th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J34) is physically located on bottom of the board as shown below.

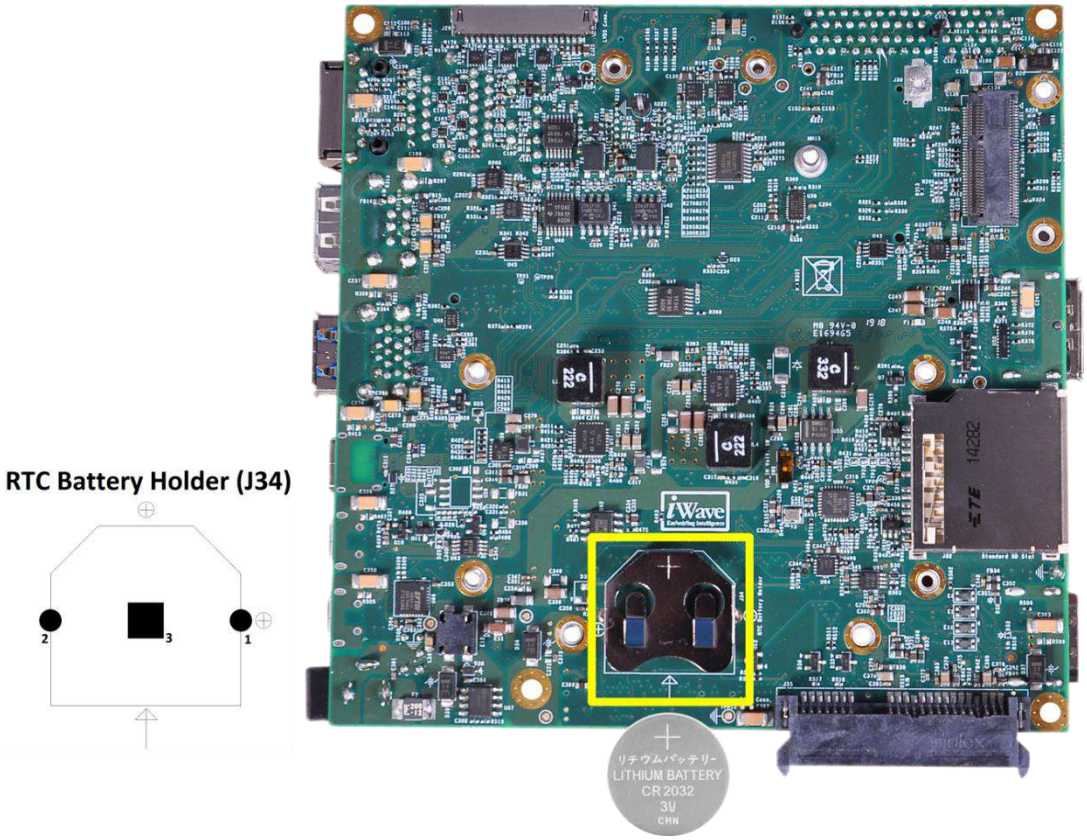


Figure 17: RTC Coin Cell Holder

2.8.2 SPI Flash (Optional)

The i.MX8M Q/QL/D SMARC carrier board supports SPI Flash through i.MX8M CPU’s eCSPI1 interface which is connected from SPI0 port of SMARC MXM connector. This SPI interface signals from SMARC MXM connector is connected to SPI Flash “IS25WPO16D-JNLE” and operating at 1.8V Level.

2.9 On Board Switches

The i.MX8M Q/QL/D SMARC carrier board has seven Switches on Top side of carrier card to support generic SMARC features. All the seven switches location is highlight in below image and the switch description is given in the following table.

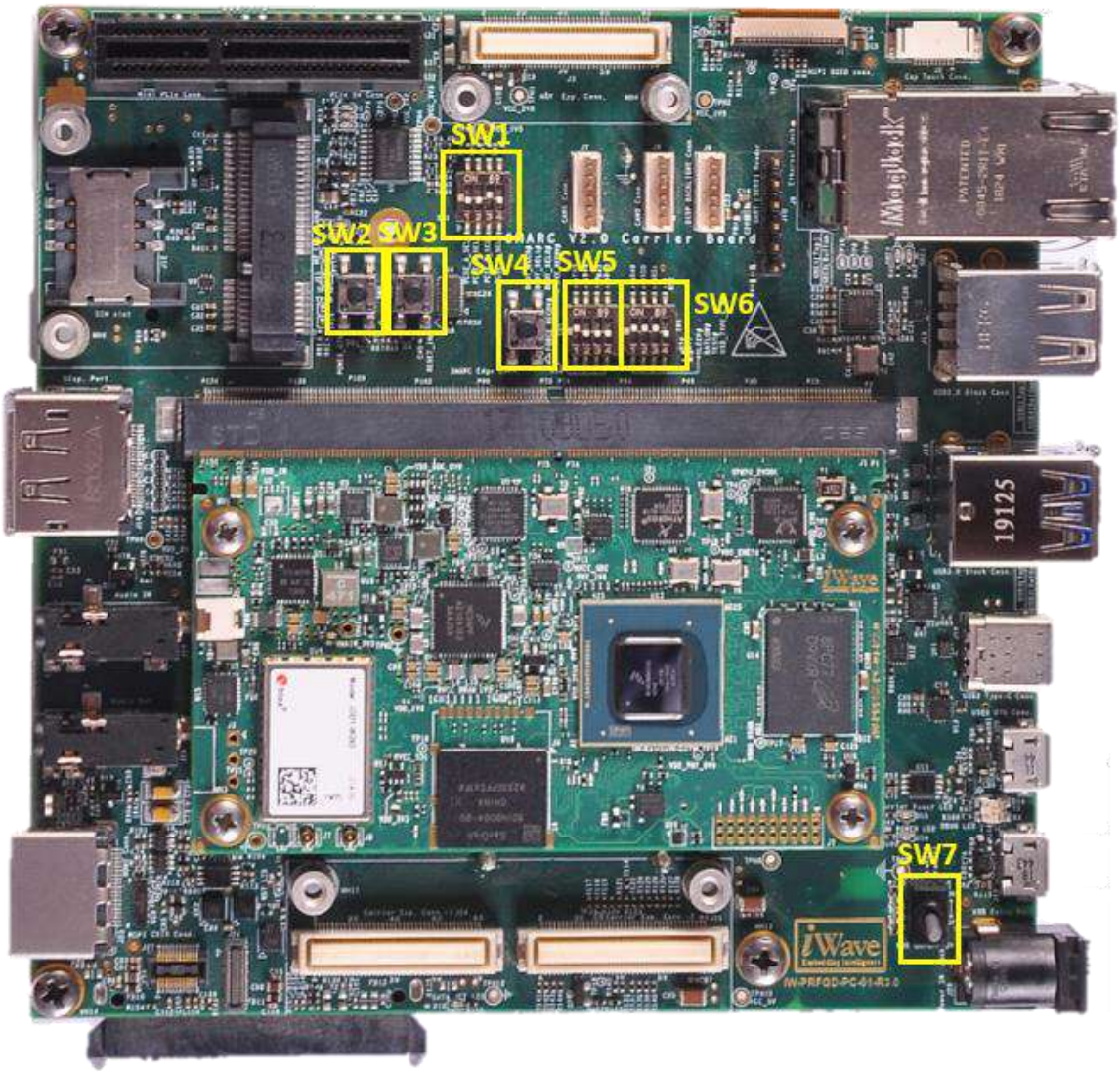
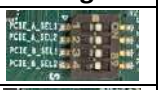
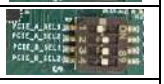


Figure 18: SMARC On Board Switches

Table 10: Board Configuration Switch

<table>
<tr><th>SW Identifier/ (SW Type)</th><th>No. of Bits</th><th>Bit Name</th><th colspan="2">Description</th><th>Remark</th></tr>
<tr><th></th><th></th><th></th><th>ON/Push</th><th>OFF/Release</th><th></th></tr>
<tr><td rowspan="4">SW1 (DIP SW)</td><td>1</td><td>PCIe_A_SEL1</td><td colspan="2" rowspan="2"><u>PCIe Channel 0 Connection:</u>
<table><tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr><tr><td>00</td><td>Hi-Z</td><td>  </td></tr><tr><td>01</td><td>MINI PCIe</td><td>  </td></tr><tr><td>10</td><td>M.2</td><td>  </td></tr><tr><td>11</td><td>PCIe x4(Lane0)</td><td>  </td></tr></table></td><td rowspan="4">1-Switch OFF (Pulled High)
0 -Switch ON (GND)

Note: At a time, do not set Both the PCIe Channel A & B neither to mini PCIe nor to M.2 connector</td></tr>
<tr><td>2</td><td>PCIe_A_SEL2</td></tr>
<tr><td>3</td><td>PCIe_B_SEL1</td><td colspan="2" rowspan="2"><u>PCIe Channel 1 Connection:</u>
<table><tr><th>State [SEL2,SEL1]</th><th>Select</th><th>Reference image</th></tr><tr><td>00</td><td>Hi-Z</td><td>  </td></tr><tr><td>01</td><td>MINI PCIe</td><td>  </td></tr><tr><td>10</td><td>M.2</td><td>  </td></tr><tr><td>11</td><td>PCIe x4(Lane1)</td><td>  </td></tr></table></td></tr>
<tr><td>4</td><td>PCIe_B_SEL2</td></tr>
<tr><td>SW2 (Push button)</td><td>1</td><td>POWER_BTN#</td><td colspan="2">SOM Power ON - One Press and release
SOM Power OFF - Long Press (above 5sec)</td><td>SOM Power ON/OFF Switch</td></tr>
<tr><td>SW3 (Push button)</td><td>1</td><td>RESET_IN#</td><td colspan="2">SOM Reset – While Pressing
SOM Out of reset – When release</td><td>SOM Reset Switch</td></tr>
<tr><td>SW4 (Push button)</td><td>1</td><td>FORCE_RECOV#</td><td>-</td><td>-</td><td>Not Supported
Note: Same signal is also connected to SW5 4th bit</td></tr>
<tr><td rowspan="3">SW5 (DIP SW)</td><td>1</td><td>BOOT_SEL0#</td><td colspan="2" rowspan="3"><u>BOOT_SEL[2:0]#</u>
110- Boot from SOM eMMC (Default)
110- Boot from SOM microSD (Optional)
001- Boot from Carrier Board SD(Optional)</td><td rowspan="3">0-Switch OFF (Floating)

1 -Switch ON (GND)</td></tr>
<tr><td>2</td><td>BOOT_SEL1#</td></tr>
<tr><td>3</td><td>BOOT_SEL2#</td></tr>
</table>

SW Identifier/ (SW Type)	No. of Bits	Bit Name	Description		Remark
			ON/Push	OFF/Release	
	4	FORCE_RECOV#	CPU USB Serial Mode (For programming the SOM boot media)	CPU Normal Boot Mode	*Note: Same signal is also connected to SW4*
SW6 (DIP SW)	**1**	LID#/SLEEP#*	-	-	Not Supported
	2	BATLOW#/CHARGING#*	-	-	Not Supported
	3	TEST#/CHARGER_PRSNT#*	-	-	Not Supported
	4	USB_TYPE_C_SW	USB3 port is connected to USB Type A (J15, Top) connector.	USB3 port is connected to USB Type C (J18) connector.	
SW7 (Toggle SW)	**1**	Carrier Power ON/ OFF Switch	Carrier Board Power is ON	Carrier board Power is OFF	Carrier Board Main 12V Power On/Off Switch.

2.10 Audio & Video Expansion Connector

The i.MX8M Q/QL/D SMARC Carrier board supports 80pin Audio & Video Expansion Connector. The Audio & Video interface signals which are not supported on carrier board are connected to this expansion connector from SMARC MXM connector. This connector can be used for expanding Audio/Video feature by designing an add-on module to it. This Audio & Video Expansion connector (J3) is physically located at the top of board as shown below.

Connectors Part number : DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector : DF17(2.0)-80DP-0.5V(57) from Hirose

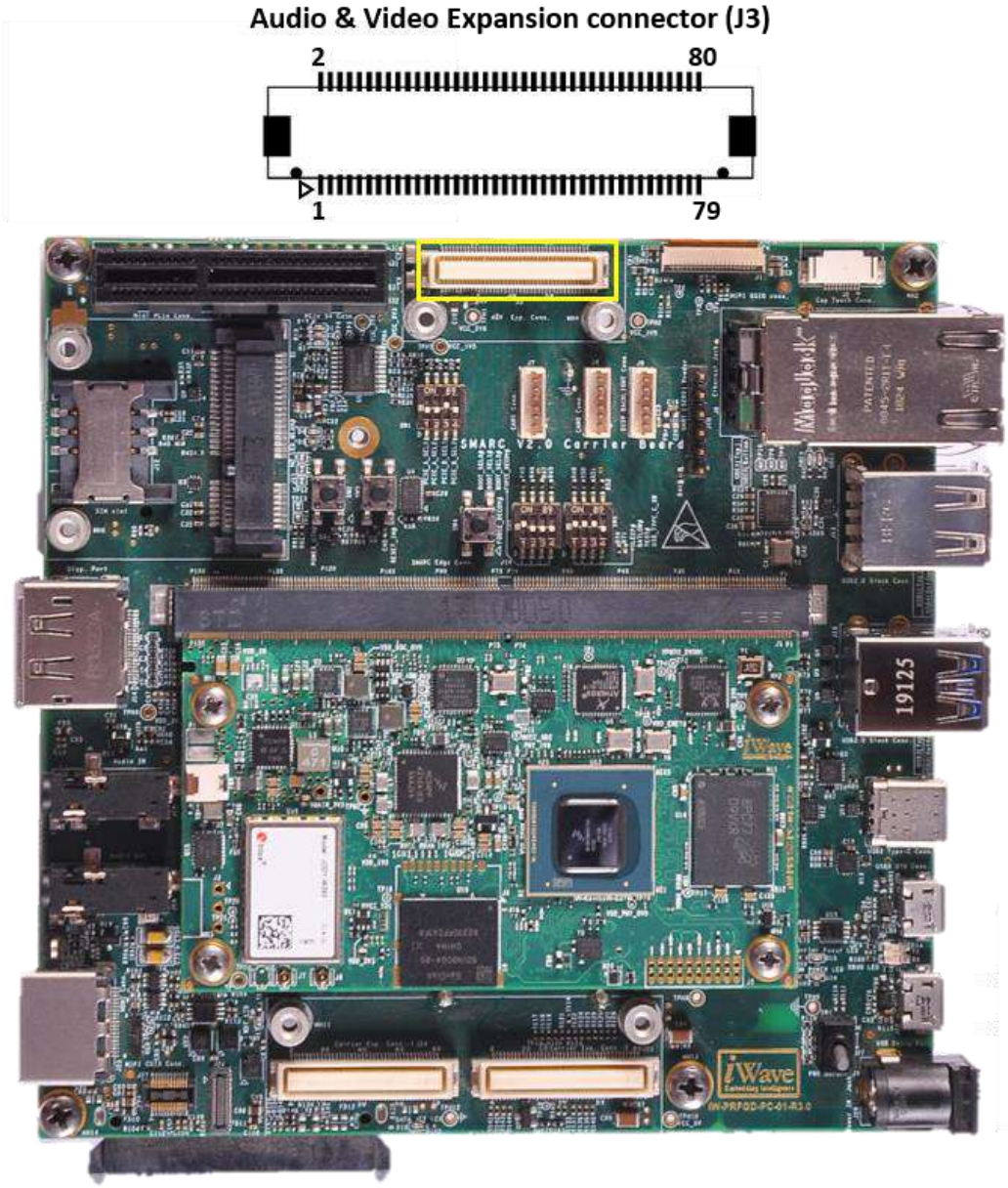


Figure 19: Audio & Video Expansion Connector

Table 11: Audio & Video Expansion Connector Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	VCC_5V	O, 5V Power	5V Supply voltage.
2	VCC_12V	O, 5V 12V Power	12V Supply voltage.
3	VCC_5V	O, Power	5V Supply voltage.
4	VCC_12V	O, 12V Power	12V Supply voltage.
5	GND	Power	Ground.
6	GND	Power	Ground.
7	VCC_2V8	O, 2.8V Power	2.8V Supply voltage.
8	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
9	VCC_2V8	O, 2.8V Power	2.8V Supply voltage.
10	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
13	VCC_1V5	O, 1.5V Power	1.5V Supply voltage.
14	GND	Power	Ground.
15	VCC_1V5	O, 1.5V Power	1.5V Supply voltage.
16	VCC_1V8	O, 1.8V Power	1.8V Supply voltage.
17	GND	Power	Ground.
18	VCC_1V8	O, 1.8V Power	1.8V Supply voltage.
19	GND	Power	Ground.
20	VCC_1V8	O, 1.8V Power	1.8V Supply voltage.
21	GND	Power	Ground.
22	GND	Power	Ground.
23	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S121st pin.*
24	VCC_1V2	O, 1.2V Power	1.2V Supply voltage.
25	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S120th pin.*
26	VCC_1V2	O, 1.2V Power	1.2V Supply voltage
27	GND	Power	Ground.
28	GND	Power	Ground.
29	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S118th pin.*
30	SAI3_TXC	O, 1.8V CMOS	SAI3 Clock. This pin is also connected to M.2 connector (J31) 08th pin for I2S Clock. *Note: This pin is connected from SMARC Edge connector S53rd pin.*

Pin No	Signal Name	Signal Type / Termination	Description
31	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S117th pin.*
32	SAI3_TXD0	O, 1.8V CMOS	SAI3 Data out. This pin is also connected to M.2 connector (J31) 12th pin for I2S Data Out. *Note: This pin is connected from SMARC Edge connector S51st pin.*
33	GND	Power	Ground
34	SAI3_RXD0	I, 1.8V CMOS	SAI3 Data IN. This pin is also connected to M.2 connector (J31) 14th pin for I2S Data In. *Note: This pin is connected from SMARC Edge connector S52nd pin.*
35	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S115th pin.*
36	SAI3_TXFS	O, 1.8V CMOS	SAI3 Left Right Synchronise clock. This pin is also connected to M.2 connector (J31) 10th pin for I2S WS. *Note: This pin is connected from SMARC Edge connector S50th pin.*
37	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S114th pin*
38	GND	Power	Ground.
39	GND	Power	Ground.
40	RSVD6	-	NC. *Note: This pin is connected from SMARC Edge connector P77th pin*
41	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S112rd pin.*
42	RSVD7	-	NC. *Note: This pin is connected from SMARC Edge connector P78th pin.*
43	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S111st pin*
44	GND	Power	Ground.
45	GND	Power	Ground.

Pin No	Signal Name	Signal Type / Termination	Description
46	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S116th pin.*
47	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S109th pin.*
48	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S107th pin.*
49	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S108th pin.*
50	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S122rd pin.*
51	GND	Power	Ground.
52	GND	Power	Ground.
53	MIPI_CSI2_DATA3_N	I, MIPI	MIPI CSI1 differential data lane 3 negative. *Note: This pin is connected from SMARC Edge connector P17th pin.*
54	GPIO_RESET_OUT(GPIO3_25)	O, 1.8V CMOS	Reset Out from CPU GPIO. *Note: This pin is connected from SMARC Edge connector P126th pin.*
55	MIPI_CSI2_DATA3_P	I, MIPI	MIPI CSI1 differential data lane 3 Positive. *Note: This pin is connected from SMARC Edge connector P16th pin.*
56	SMARC_GPIO_9(GPIO1_03)	IO, 1.8V CMOS	General Purpose Input / Output. This pin is connected to MIPI Display reset. *Note: This pin is connected from SMARC Edge connector P117th pin.*
57	GND	Power	Ground.
58	GND	Power	Ground.
59	MIPI_CSI2_DATA2_N	I, MIPI	MIPI CSI1 differential data lane 2 negative. *Note: This pin is connected from SMARC Edge connector P14th pin.*
60	RSVD8	-	NC. *Note: This pin is connected from SMARC Edge connector S123rd pin.*
61	MIPI_CSI2_DATA2_P	I, MIPI	MIPI CSI1 differential data lane 2 Positive *Note: This pin is connected from SMARC Edge connector P13rd pin.*

Pin No	Signal Name	Signal Type / Termination	Description
62	RSVD9	-	NC. *Note: This pin is connected from SMARC Edge connector S142nd pin.*
63	GND	Power	Ground
64	RSVD5	-	NC. *Note: This pin is connected from SMARC Edge connector P73rd pin.*
65	MIPI_CSI2_DATA1_N	I, MIPI	MIPI CSI1 differential data lane 1 negative. *Note: This pin is connected from SMARC Edge connector P11st pin.*
66	RSVD4	-	NC. *Note: This pin is connected from SMARC Edge connector P72rd pin.*
67	MIPI_CSI2_DATA1_P	I, MIPI	MIPI CSI1 differential data lane 1 Positive *Note: This pin is connected from SMARC Edge connector P10th pin.*
68	I2C4_SDA	IO, 1.8V CMOS	I2C4 data. This pin is also connected to MIPI DSI connector (J1) 35th pin. *Note: This pin is connected from SMARC Edge connector S140th pin.*
69	GND	Power	Ground.
70	I2C4_SCL	O, 1.8V CMOS	I2C4 Clock. This pin is also connected to MIPI DSI connector (J1) 36th pin. *Note: This pin is connected from SMARC Edge connector S139th pin.*
71	MIPI_CSI2_DATA0_N	I, MIPI	MIPI CSI1 differential data lane 0 negative. *Note: This pin is connected from SMARC Edge connector P8th pin.*
72	GND	Power	Ground.
73	MIPI_CSI2_DATA0_P	I, MIPI	MIPI CSI1 differential data lane 0 Positive. *Note: This pin is connected from SMARC Edge connector P7th pin.*
74	I2C1_SDA	IO, 1.8V CMOS	I2C1 data for camera. *Note: This pin is connected from SMARC Edge connector S2nd pin.*
75	GND	Power	Ground.
76	I2C1_SCL	O, 1.8V CMOS	I2C1 Clock for camera. *Note: This pin is connected from SMARC Edge connector S1st pin.*

Pin No	Signal Name	Signal Type / Termination	Description
77	MIPI_CSI2_CLK_N	I, MIPI	MIPI CSI1 differential Clock negative. *Note: This pin is connected from SMARC Edge connector P4th pin.*
78	SMARC_GPIO_3(GPIO1_11)	IO, 1.8V CMOS	General Purpose Input / Output. *Note: This pin is connected from SMARC Edge connector P111st pin.*
79	MIPI_CSI2_CLK_P	I, MIPI	MIPI CSI1 differential Clock Positive. *Note: This pin is connected from SMARC Edge connector P3rd pin.*
80	GND	Power	Ground.

2.11 SOM Expansion Connector(Optional)

The i.MX8M Q/QL/D SMARC Carrier board has one 100pin SOM Expansion Connector for mating with i.MX8M Q/QL/D SMARC SOM. This SOM Expansion connector (J22) pins are directly connected to Carrier board Expansion connector 1 & 2 (J25 & J26) in .MX8M Q/QL/D SMARC Carrier board. This Expansion connector (J22) is physically located at the top of board as shown below.

Connectors Part number : FX8C-100P-SV(91) from Hirose

Mating Connector : FX8C-100S-SV(91) from Hirose

Note: For this connector pinout, refer the i.MX8M Q/QL/D SMARC SOM Hardware User Guide.

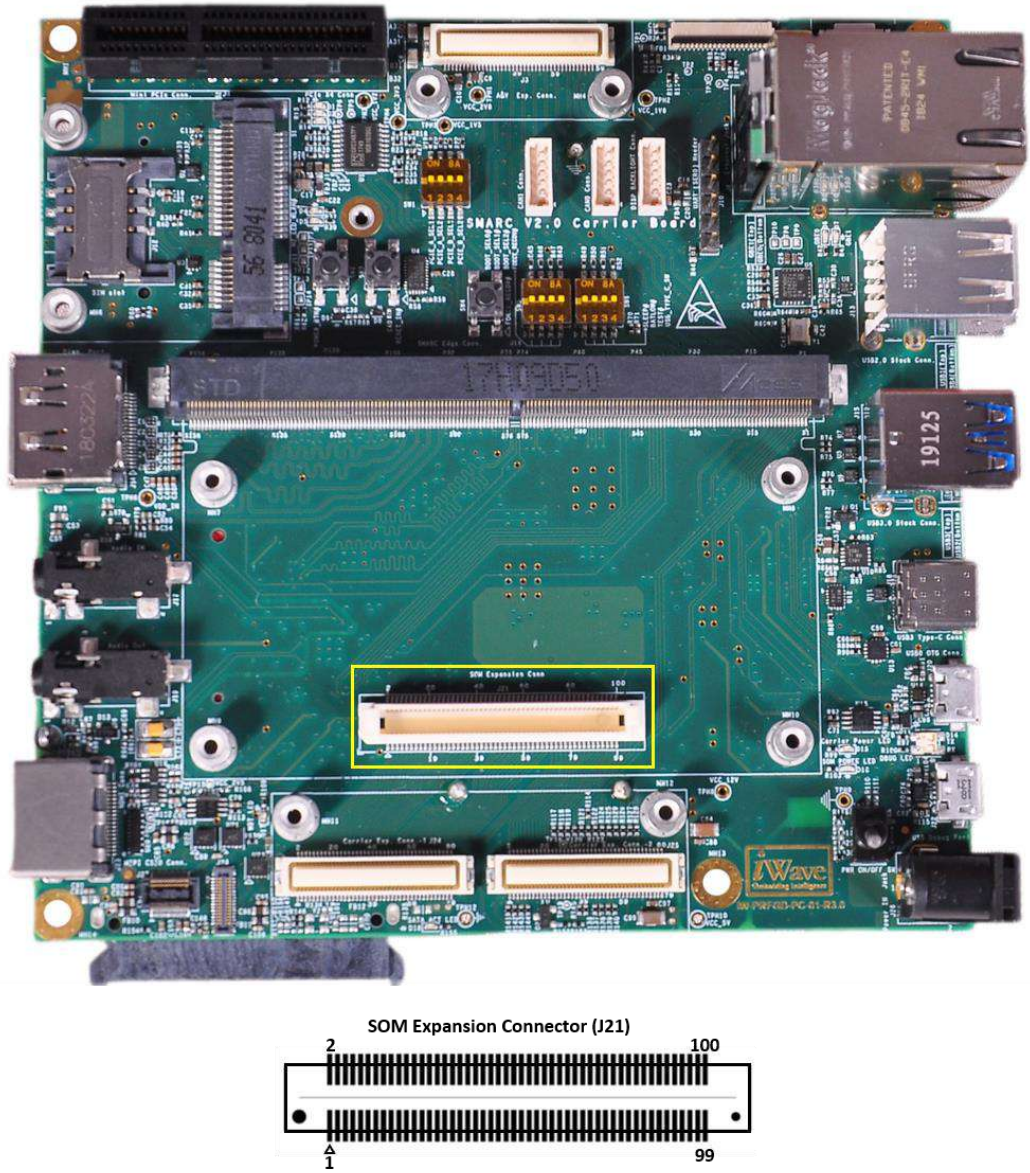


Figure 20: SMARC SOM Expansion Connector

2.12 Carrier Expansion Connectors

The i.MX8M Q/QL/D SMARC Carrier board have two 80pin Expansion Connectors for expansion purpose. All the signals from the SOM expansion connector are directly taken out via these two carrier expansion connectors along with few other signals and power. An add-on module can be designed to utilise these signals. These Expansion connectors (J25 & J26) are physically located at the top of board as shown below.

Connectors Part number : DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector : DF17(2.0)-80DP-0.5V(57) from Hirose

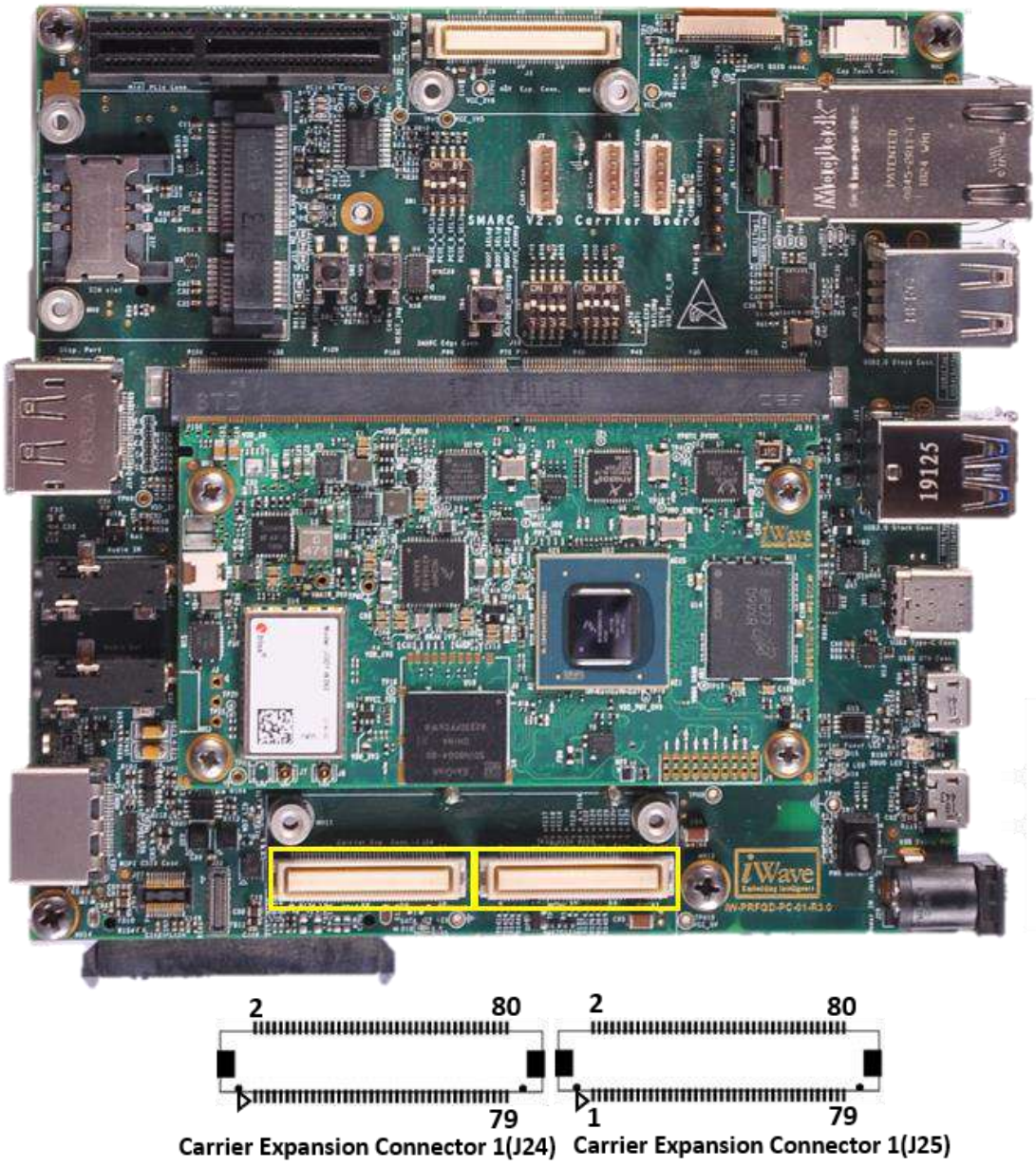


Figure 21: SMARC Expansion Connector

Table 12: Carrier Expansion Connector1 Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 2nd pin.*
2	SAI1_TXD0	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 0. *Note: This pin is connected from SOM Expansion connector 1st pin.*
3	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 4th pin.*
4	SAI1_TXD6	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 6. *Note: This pin is connected from SOM Expansion connector 3rd pin.*
5	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 6th pin.*
6	SAI1_TXD2	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 2. *Note: This pin is connected from SOM Expansion connector 5th pin.*
7	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 8th pin.*
8	SAI1_TXD3	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 3. *Note: This pin is connected from SOM Expansion connector 7th pin.*
9	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 10th pin.*
10	SAI1_TXD4	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 4. *Note: This pin is connected from SOM Expansion connector 9th pin.*
11	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 12th pin.*
12	SAI1_TXD5	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 5. *Note: This pin is connected from SOM Expansion connector 11th pin.*
13	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 14th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
14	SAI1_TXD7	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 7. *Note: This pin is connected from SOM Expansion connector 13th pin.*
15	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 16th pin.*
16	SAI1_TXD1	I, 1.8V CMOS	Serial Audio Interface 1 Data Transmitter 1. *Note: This pin is connected from SOM Expansion connector 15th pin.*
17	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 18th pin.*
18	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 17th pin.*
19	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 20th pin.*
20	SAI1_TXFS	I, 1.8V CMOS	Serial Audio Interface 1 Transmitter Frame Sync. *Note: This pin is connected from SOM Expansion connector 19th pin.*
21	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 22nd pin.*
22	SAI1_TXC	I, 1.8V CMOS	Serial Audio Interface 1 Transmitter Clock. *Note: This pin is connected from SOM Expansion connector 21st pin.*
23	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 24th pin.*
24	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 23rd pin.*
25	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 26th pin.*
26	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 25th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
27	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 28th pin.*
28	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 27th pin.*
29	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 30th pin.*
30	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 29th pin.*
31	BCONFIG_0(GPIO3_2)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 32nd pin.*
32	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 31st pin.*
33	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 34th pin.*
34	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 33rd pin.*
35	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 36th pin.*
36	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 35th pin.*
37	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 38th pin.*
38	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 37th pin.*
39	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 40th pin.*
40	SAI1_RXD2	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 2. *Note: This pin is connected from SOM Expansion connector 39th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
41	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 42nd pin.*
42	SAI1_RXD5	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 5. *Note: This pin is connected from SOM Expansion connector 41st pin.*
43	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 44th pin.*
44	SAI1_RXD4	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 4. *Note: This pin is connected from SOM Expansion connector 43rd pin.*
45	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 46th pin.*
46	SAI1_RXD7	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 7. *Note: This pin is connected from SOM Expansion connector 45th pin.*
47	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 48th pin.*
48	SAI1_RXD3	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 3 *Note: This pin is connected from SOM Expansion connector 47th pin.*
49	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 50th pin.*
50	SAI1_RXFS	O, 1.8V CMOS	Serial Audio Interface 1 Receiver Frame Sync. *Note: This pin is connected from SOM Expansion connector 49th pin.*
51	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 52nd pin.*
52	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 51st pin.*
53	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 54th pin.*
54	SAI1_RXD6	O, 1.8V CMOS	Serial Audio Interface 1 Data Receiver 6. *Note: This pin is connected from SOM Expansion connector 53rd pin.*

Pin No	Signal Name	Signal Type / Termination	Description
55	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 56th pin.*
56	SAI1_RXC	O, 1.8V CMOS	Serial Audio Interface 1 Receiver Clock. *Note: This pin is connected from SOM Expansion connector 55th pin.*
57	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 58th pin.*
58	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 57th pin.*
59	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 60th pin.*
60	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 59th pin.*
61	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 62nd pin.*
62	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 61st pin.*
63	BCONFIG_3(GPIO5_2)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 64th pin.*
64	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 63rd pin.*
65	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 66th pin.*
66	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 65th pin.*
67	BCONFIG_2(GPIO4_29)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 68th pin.*
68	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 67th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
69	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 70th pin.*
70	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 69th pin.*
71	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 72nd pin.*
72	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 71st pin.*
73	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 74th pin.*
74	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 73rd pin.*
75	BCONFIG_1(GPIO4_28)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 76th pin.*
76	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 75th pin.*
77	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 78th pin.*
78	BCONFIG_4(GPIO4_22)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 77th pin.*
79	GND	Power	Ground.
80	GND	Power	Ground.

Table 13: Carrier Expansion Connector2 Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	MIPI_CSI1_DATA2_P	I, MIPI	MIPI CSI1 Differential Data lane 2 positive. This pin is also connected to MIPI CSI Camera connector. *Note: This pin is connected from SOM Expansion connector 80th pin.*
2	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 79th pin*
3	MIPI_CSI1_DATA2_N	I, MIPI	MIPI CSI1 Differential Data lane 2 negative This pin is also connected to MIPI CSI Camera connector. *Note: This pin is connected from SOM Expansion connector 82nd pin*
4	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 81st pin.*
5	GND	Power	Ground *Note: This pin is connected from SOM Expansion connector 84th pin.*
6	GND	Power	Ground *Note: This pin is connected from SOM Expansion connector 83rd pin.*
7	MIPI_CSI1_DATA3_P	I, MIPI	MIPI CSI1 Differential Data lane 3 positive. This pin is also connected to MIPI CSI Camera connector. *Note: This pin is connected from SOM Expansion connector 86th pin.*
8	NC	-	NC. *Note: This pin is connected from SOM Expansion connector85th pin.*
9	MIPI_CSI1_DATA3_N	I, MIPI	MIPI CSI1 Differential Data lane 3 negative. This pin is also connected to MIPI CSI Camera connector. *Note: This pin is connected from SOM Expansion connector 88th pin.*
10	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 87th pin.*
11	GND	Power	Ground. *Note: This pin is connected from SOM Expansion connector 90th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
12	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 89th pin*
13	BCONFIG_5(GPIO4_21)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 92nd pin.*
14	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 91st pin.*
15	HDMI_CEC	IO, 1.8V CMOS	HDMI CEC. *Note: This pin is connected from SOM Expansion connector 94th pin.*
16	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 93rd pin.*
17	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 96th pin.*
18	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 95th pin.*
19	CLK1_P	I, DIFF	Differential Input Clock positive to CPU. *Note: This pin is connected from SOM Expansion connector 98th pin.*
20	NC	-	NC. *Note: This pin is connected from SOM Expansion connector 97th pin.*
21	CLK1_N	I, DIFF	Differential Input Clock negative to CPU. *Note: This pin is connected from SOM Expansion connector 100th pin.*
22	BCONFIG_6(GPIO3_14)	O, 1.8V CMOS	General Purpose Input/Output. *Note: This pin is connected from SOM Expansion connector 99th pin.*
23	BATLOW#	-	NC. This pin is also connected to general purpose DIP switch SW6. *Note: This pin is connected from SMARC Edge connector S156th pin.*
24	WDT_TIME_OUT#	I, 1.8V CMOS	Watch DOG Time Out Interrupt. *Note: This pin is connected from SMARC Edge connector S145th pin.*
25	GND	Power	Ground.

Pin No	Signal Name	Signal Type / Termination	Description
26	UART3_TXD	O, 1.8V CMOS	UART3 Transmitter. *Note: This pin is connected from SMARC Edge connector P135th pin.*
27	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S144th pin.*
28	UART3_RXD	I, 1.8V CMOS	UART3 Receiver. *Note: This pin is connected from SMARC Edge connector P134th pin.*
29	NC	-	NC. *Note: This pin is connected from SMARC Edge connector P122rd pin.*
30	GND	Power	Ground
31	SMARC_GPIO_6(GPIO1_09)	IO, 1.8V CMOS	General Purpose Input /Output. This pin is also connected to USB Type C Controller Interrupt pin. *Note: This pin is connected from SMARC Edge connector P114th pin.*
32	NC	-	NC. *Note: This pin is connected from SMARC Edge connector P121st pin.*
33	PCIe_B_RST#	I, 3.3V CMOS	PCIe Link B Reset Out. *Note: This pin is connected from SMARC Edge connector S76th pin.* *Note: This is optional feature in SOM.*
34	eCSPI1_MISO	O, 1.8V CMOS	eCSPI1 Master In Slave Out. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P45th pin.*
35	GND	Power	Ground
36	eCSPI1_MOSI	I, 1.8V CMOS	eCSPI1 Master Out Slave In This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P46th pin.*
37	MIPI_CSI1_CLK_P	O, MIPI	MIPI CSI1 differential Clock positive. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S8th pin.*
38	eCSPI1_SCLK	I, 1.8V CMOS	eCSPI 1 Clock. This pin is also connected to on board SPI Flash.

Pin No	Signal Name	Signal Type / Termination	Description
			Note: This pin is connected from SMARC Edge connector P44th pin.
39	MIPI_CSI1_CLK_N	O, MIPI	MIPI CSI1 differential Clock negative. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S9th pin.*
40	GND	Power	Ground
41	PCIe_C_RST#	-	NC. *Note: This pin is connected from SMARC Edge connector S77th pin.*
42	I2C3_SDA	IO, 1.8V CMOS	I2C3 Data. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S7th pin.*
43	GND	Power	Ground.
44	MCLK(SAI1_MCLK)	O, 1.8V CMOS	Master Clock for Camera. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S6th pin.*
45	MIPI_CSI1_DATA0_P	O, MIPI	MIPI CSI1 Receiver differential data lane 0 positive. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S11th pin*
46	I2C3_SCL	I, 1.8V CMOS	I2C3 Clock. This pin is connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S5th pin.*
47	MIPI_CSI1_DATA0_N	O, MIPI	MIPI CSI1 Receiver differential data lane 0 negative. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S12th pin.*
48	GND	Power	Ground.
49	GND	Power	Ground.

Pin No	Signal Name	Signal Type / Termination	Description
50	I2C2_SCL	I, 1.8V CMOS	I2C2 Clock. I2C clock for carrier board peripherals. *Note: This pin is connected from SMARC Edge connector S48th pin.*
51	MIPI_CSI1_DATA1_P	O, MIPI	MIPI CSI1 Receiver Differential Data lane 1 positive. This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S14th pin.*
52	I2C2_SDA	IO, 1.8V CMOS	I2C 2 Data I2C data for carrier board peripherals. *Note: This pin is connected from SMARC Edge connector S49th pin.*
53	MIPI_CSI1_DATA1_N	O, MIPI	MIPI CSI1 Receiver Differential Data lane 1 negative This pin is also connected to MIPI CSI camera connector. *Note: This pin is connected from SMARC Edge connector S15th pin.*
54	GND	Power	Ground.
55	QSPI_B_DQS	O, 1.8V CMOS	QSPIB RESET. *Note: This pin is connected from SMARC Edge connector S58th pin.*
56	QSPI_B_SS0_B	I, 1.8V CMOS	QSPIB Chip Select0. This pin is also connected to M.2 connector. *Note: This pin is connected from SMARC Edge connector P54th pin.*
57	QSPI_B_DATA3	IO, 1.8V CMOS	QSPIB Data3. *Note: This pin is connected from SMARC Edge connector S57th pin.*
58	QSPI_B_SS1_B	I, 1.8V CMOS	QSPIB Chip Select1. This pin is also connected to M.2 connector. *Note: This pin is connected from SMARC Edge connector P55th pin.*
59	QSPI_B_DATA2	IO, 1.8V CMOS	QSPIB Data2. *Note: This pin is connected from SMARC Edge connector S56th pin.*
60	QSPI_B_CLK	I, 1.8V CMOS	QSPIB Clock. This pin is connected to M.2 connector. *Note: This pin is connected from SMARC Edge connector P56th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
61	USB_HUB4_OC	O, 3.3V CMOS	USB HUB Over Current Sense 4. *Note: This pin is connected from SMARC Edge connector S55th pin.*
62	QSPI_B_DATA1	IO, 1.8V CMOS	QSPIB DATA1. This pin is connected to M.2 connector *Note: This pin is connected from SMARC Edge connector P58th pin.*
63	RSVD1	-	NC. *Note: This pin is connected from SMARC Edge connector S4th pin.*
64	QSPI_B_DATA0	IO, 1.8V CMOS	QSPIB DATA0. This pin is connected to M.2 connector. *Note: This pin is connected from SMARC Edge connector P57th pin.*
65	SMB_ALERT_1V8#	I, 1.8V CMOS	SM Bus Alert# (interrupt) *Note: This pin is connected from SMARC Edge connector P1st pin.*
66	RSVD3	-	NC. *Note: This pin is connected from SMARC Edge connector S46th pin.*
67	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S43rd pin.*
68	RSVD2	-	NC. *Note: This pin is connected from SMARC Edge connector S45th pin.*
69	SPI0_CS0#	I, 1.8V CMOS	ECSPI1 Chip Select 0. This pin is also connected to on board SPI Flash. *Note: This pin is connected from SMARC Edge connector P43rd pin.*
70	NC	-	NC. *Note: This pin is connected from SMARC Edge connector P31st pin.*
71	VCC_1V8	O, Power	1.8V Supply voltage.
72	NC	-	NC. *Note: This pin is connected from SMARC Edge connector S44th pin.*
73	GND	Power	Ground.
74	GND	Power	Ground.
75	VCC_5V	O, 5V Power	5V Supply voltage.
76	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
77	VCC_5V	O, 5V Power	5V Supply voltage.

Pin No	Signal Name	Signal Type / Termination	Description
78	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.
79	VCC_5V	O, 5V Power	5V Supply voltage.
80	VCC_3V3	O, 3.3V Power	3.3V Supply voltage.

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX8M Q/QL/D SMARC Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The i.MX8M Q/QL/D SMARC Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the SMARC Carrier Board through Power Jack (J26). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm. This connector is physically placed at the top of the board as shown below.

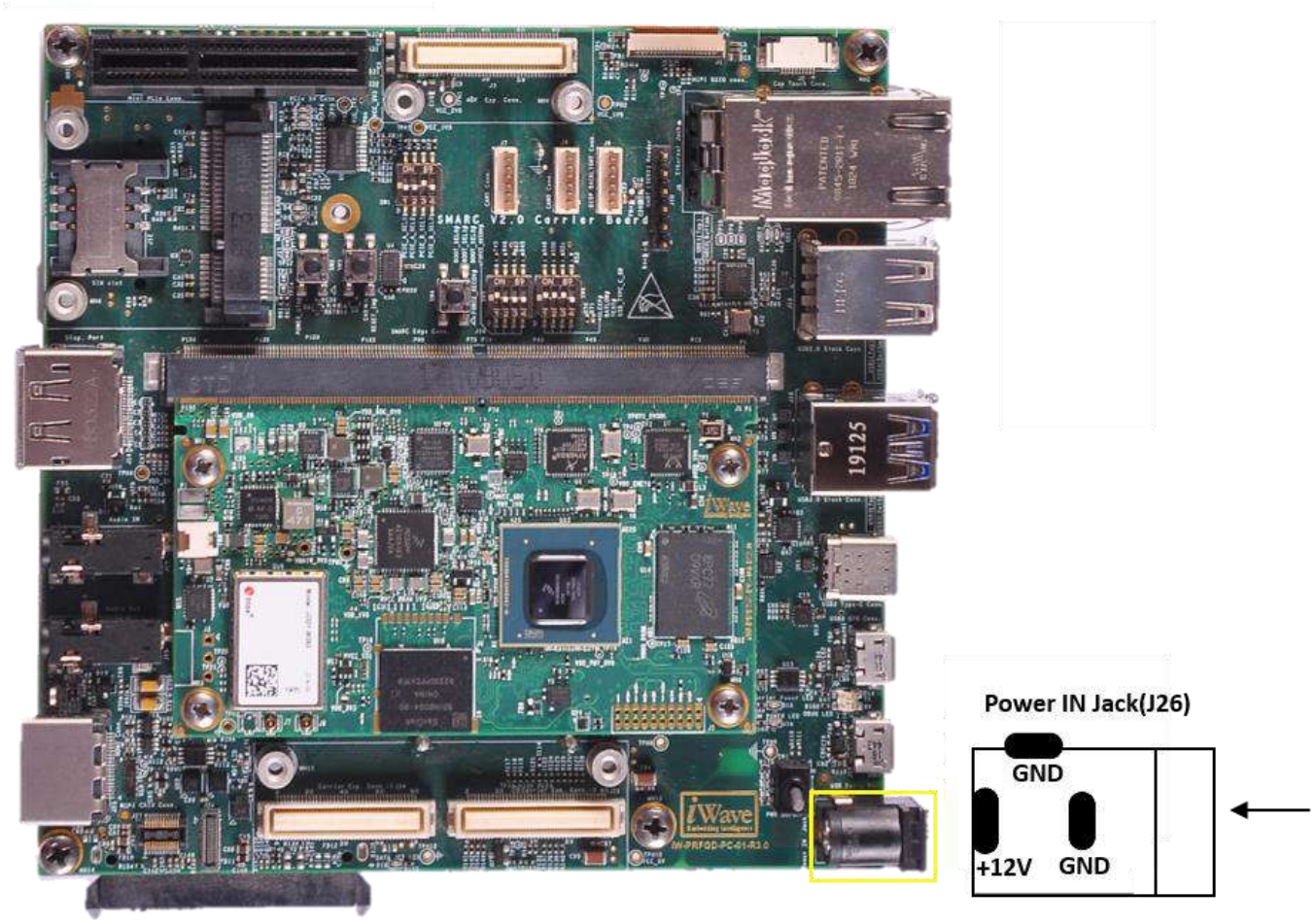


Figure 22: Power Jack

The below table provides the Power Input Requirement of i.MX8M Q/QL/D SMARC Carrier Board.

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] SMARC Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX8M Q/QL/D SMARC SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

3.2 Power Output Specification

The i.MX8M Q/QL/D SMARC Carrier Board has dedicated power regulator to provide +5V power to SMARC SOM for VIN power supply. Also +3V RTC power from coin cell holder is provided to Qseven SOM for Real time clock support.

The i.MX8M Q/QL/D SMARC carrier board also shares different on-board power to Audio & Video connector and Carrier Expansion connector2 for its Add-On Module power.

Table 15: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to SMARC SOM (through SMARC MXM connector)					
1	VIN_5V	4.85V	5V	5.15V	5000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Audio & Video Connector)					
1	VCC_12V	11.75V	12V	12.25V	500mA
2	VCC_5V	4.85V	5V	5.15V	1000mA
3	VCC_3V3	3.15	3.3	3.45	1500mA
4	VCC_2V8	2.5	2.55	2.6	500mA
5	VCC_1V8	1.7	1.8	1.9	500mA
6	VCC_1V5	1.35	1.5	1.65	500mA
7	VCC_1V2	1.1	1.2	1.3	500mA
Power to Add-On Module (through Expansion Connector2)					
1	VCC_5V	4.85V	5V	5.15V	1500mA
2	VCC_3V3	3.15	3.3	3.45	1500mA
3	VCC_1V8	1.7	1.8	1.9	500mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX8M Q/QL/D SMARC Development Platform.

Table 16: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's i.MX8M Q/QL/D SMARC Development Platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX8M Q/QL/D SMARC Development Platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX8M Q/QL/D SMARC Carrier Board Mechanical Dimensions

The i.MX8M Q/QL/D SMARC Development Platform PCB size is 120 mm x 120 mm x 1.6mm. SMARC carrier card mechanical dimension is shown below. (All dimensions are shown in mm)

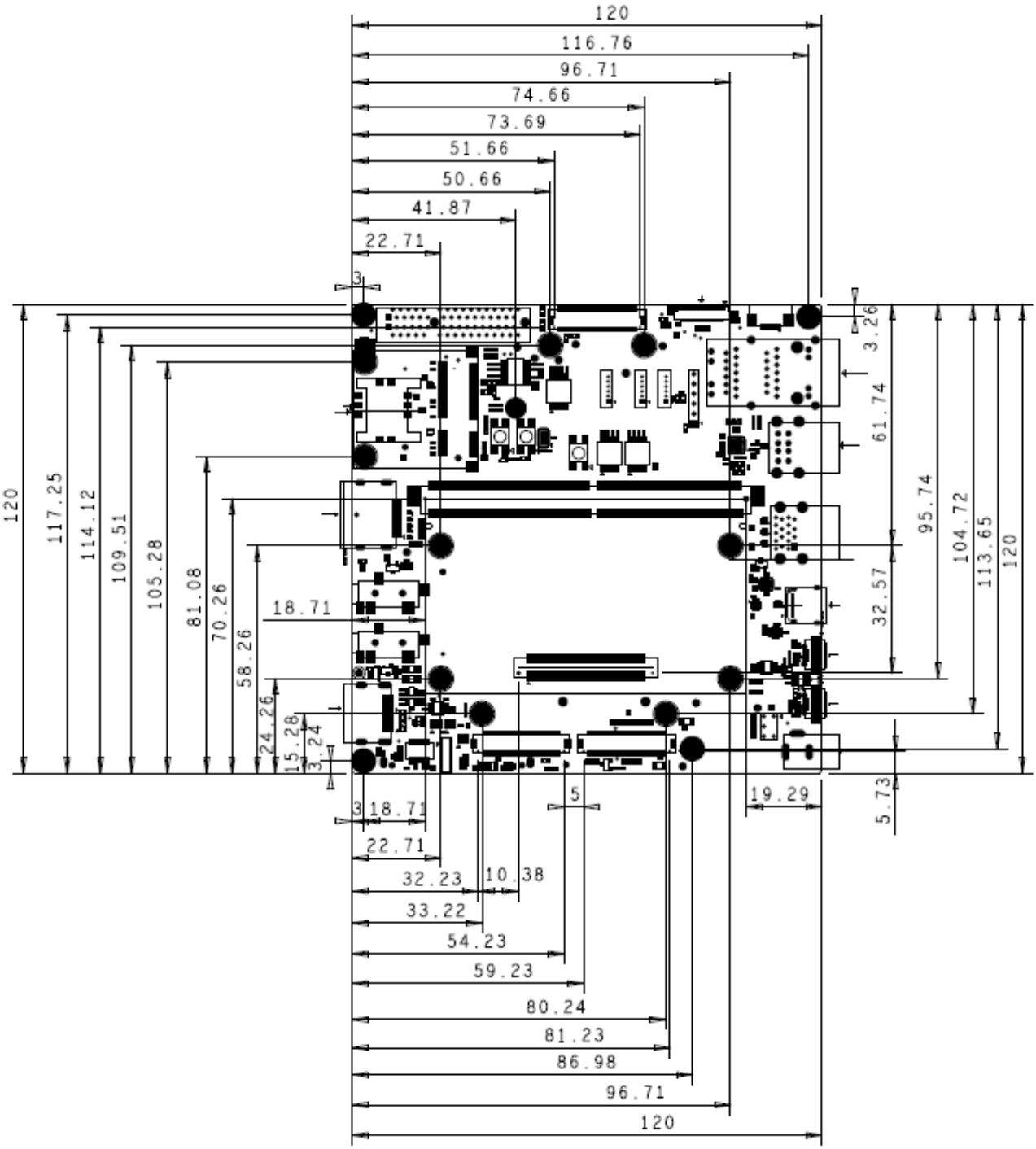


Figure 23: Mechanical dimension of i.MX8M Q/QL/D SMARC Carrier Board- Top View

The i.MX8M Q/QL/D SMARC Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector dual Ethernet Jack J6 (29.34mm) followed by USB3.0 Stack slot J15(15.6mm) and bottom side maximum height component is inductor (7mm). Please refer the below figure which gives height details of the i.MX8M Q/QL/D SMARC Development kit.

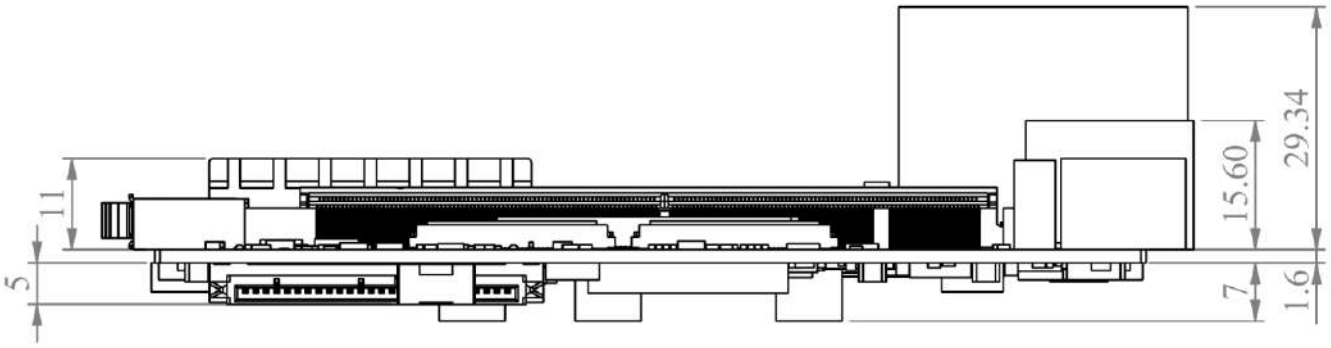


Figure 24: Mechanical dimension of i.MX8M Q/QL/D SMARC Carrier Board - Side View

3.4.2 Guidelines to insert the SMARC SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the SMARC module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of SMARC module is proper while inserting.
- Once the SMARC module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

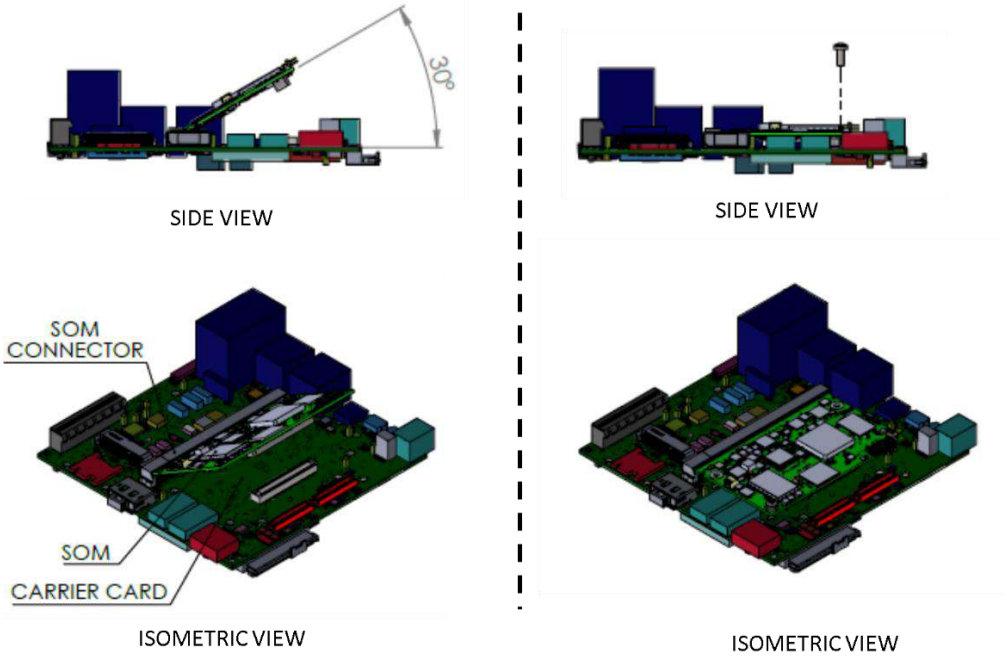


Figure 25: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8M Q/QL/D SMARC Development Platform which includes i.MX8M Q/QL/D SMARC SOM and SMARC carrier board.

Table 17: Orderable Product Part Numbers

Product Part Number	Description	Temperature
i.MX8M Quad SMARC Development Platform		
iW-G33D-SCMQ-4L002G-E008G-LCC	i.MX8M Quad SMARC SOM 2xEthernet Linux Development Platform with 2GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCMQ-4L002G-E008G-LCD	i.MX8M Quad SMARC SOM Linux Development Platform with 2GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCMQ-4L002G-E008G-ACC	i.MX8M Quad SMARC SOM 2xEthernet Android Development Platform with 2GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCMQ-4L002G-E008G-ACD	i.MX8M Quad SMARC SOM 2xEthernet Android Development Platform with 2GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial
i.MX8M QuadLite SMARC Development Platform		
iW-G33D-SCML-4L002G-E008G-LCC	i.MX8M QuadLite SMARC SOM 2xEthernet Linux Development Platform with 2GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCML-4L002G-E008G-LCD	i.MX8M QuadLite SMARC SOM 2xEthernet Linux Development Platform with 2GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCML-4L002G-E008G-ACC	i.MX8M QuadLite SMARC SOM 2xEthernet Android Development Platform with 2GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCML-4L002G-E008G-ACD	i.MX8M QuadLite SMARC SOM 2xEthernet Android Development Platform with 2GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial
i.MX8M Dual SMARC Development Platform		
iW-G33D-SCMD-4L001G-E008G-LCC	i.MX8M Dual SMARC SOM 2xEthernet Linux Development Platform with 1GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCMD-4L001G-E008G-LCD	i.MX8M Dual SMARC SOM 2xEthernet Linux Development Platform with 1GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial
iW-G33D-SCMD-4L001G-E008G-ACC	i.MX8M Dual SMARC SOM Android 2xEthernet Development Platform with 1GB RAM, 8GB eMMC with 5.5" Capacitive touch LCD display	Commercial

Product Part Number	Description	Temperature
iW-G33D-SCMD-4L001G-E008G-ACD	i.MX8M Dual SMARC SOM 2xEthernet Android Development Platform with 1GB RAM, 8GB eMMC without 5.5" Capacitive touch LCD display	Commercial

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.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