Data Sheet For Video Scaler

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24th Dec '11	Initial Version	AS
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Video Scaler Module. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Video Scaler Core:

- Scaling factor: downscale/upscale by min 1 to max 4 independently in vertical and horizontal direction
- Programmable non-integer scaling factor
- Algorithm: 5-tap interpolating filter
- Quantization Level: Inter Pixel = 6, Filter Coefficients = 12
- Coefficients are software programmable
- Image size programmable from QCIF to Full HD
- Video Format: 4:4:4 RGB/YCbCr
- 8-bit per pixel per color
- 3 color plane in parallel processing

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
RGB	Red Green Blue
HD	High definition
QCIF	Quarter Common Intermediate Format

2 Video Scaler

2.1 Block Diagram

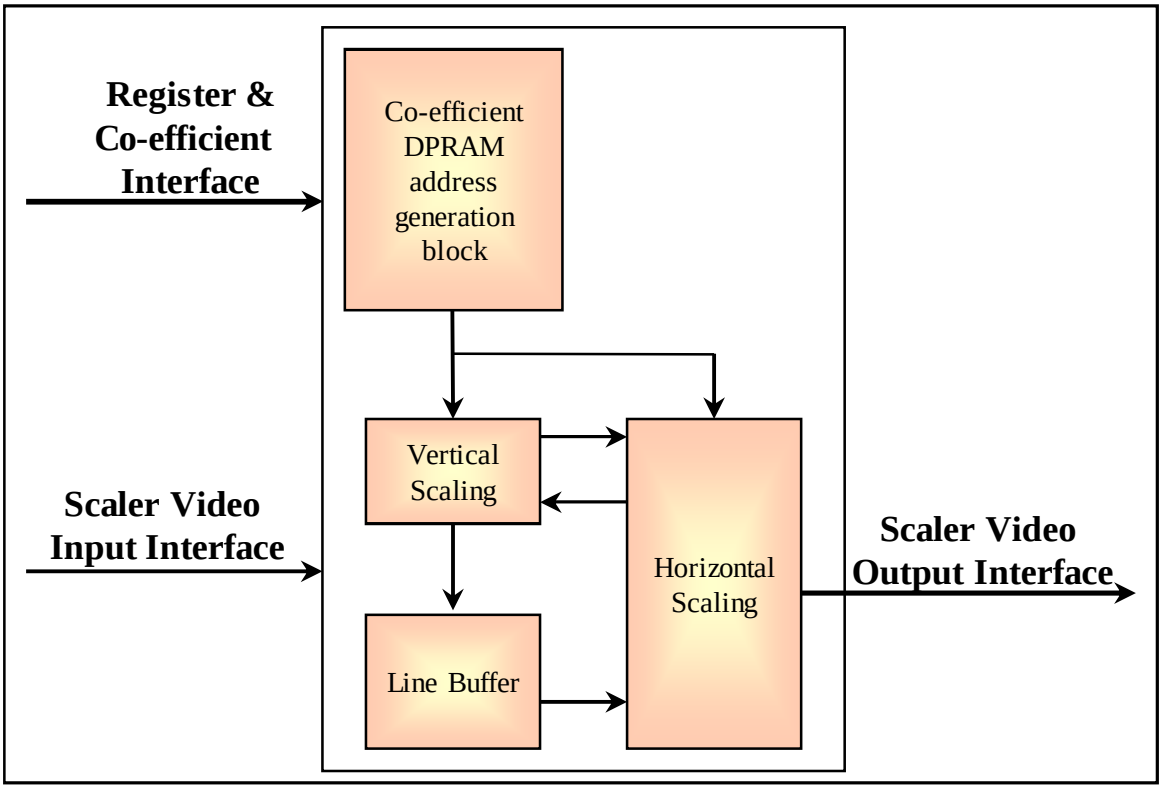

Figure 1: Video Scaler Block Diagram

2.2 Description

This module up and down scales incoming data by 1 to 4 times independently in vertical and horizontal direction. The horizontal scale factor and vertical scale factor is configurable. Scaling factor is 16-bit, 4-bit for integer number and 12-bit for fractional number. The scaling is done by 5-tap interpolation filter and filter co-efficient is configurable. The filter coefficients value depends on the quantized value of the fractional number. To get the scaled image, the incoming data is first vertically scaled, and then that result will be horizontally scaled.

- **Co-efficient DPRAM address generation block:** This module generates the filter co-efficient DPRAM read address for each pixel to get the filter coefficients from DPRAM. The fractional value of scaling factor is loaded into 12-bit counter and the counter increments by the same fractional value of scaling factor for every pixel/line in the destination image. Incremented counter output as an address to the Coefficient DPRAM.

- **Line Buffer:** Line buffer is maintained to store the incoming data to facilitate the vertical sampling operation. Five line buffers are used and each line buffer has a depth of 1920 and 24bit width to store the incoming lines.

- **Vertical scaling:** The incoming data is stored in the line buffer. A counter is maintained for sending out the scaled lines and the counter increments by the vertical scaling factor for every line is send out.

- **Horizontal scaling:** This module does the scaling on the data read from the line buffer in the horizontal direction. A counter is maintained for sending out the scaled pixels in the horizontal direction and the counter increments by horizontal scaling factor for every pixel is send out.

2.3 I/O Signal Description

Table 2: Video Scaling IO Signals

Signal	I/O	Width	Description
clk_i	I	1	Clock input
rst_n_i	I	1	Asynchronous active low reset input.
lpf_i[10:0]	I	11	No. of lines per frame of input video.
ppl_i[10:0]	I	11	No. of pixels per line of input video.
scalar_lpf_i[10:0]	I	11	No. of lines per frame from scalar,
scalar_ppl_i[10:0]	I	11	No. of pixels per line from scalar.
vscale_i[15:0]	I	16	Vertical Scaling Factor input from the register block
hscale_i[15:0]	I	16	Horizontal Scaling Factor input from the register block
coeff_ram_raddr_o[5:0]	O	6	Filter co-efficient DPRAM read address output
tap1_coeffi_i[12:0]	I	14	1st Tap Filter co-efficient DPRAM read data
tap2_coeffi_i[12:0]	I	14	2nd Tap Filter co-efficient DPRAM read data
tap3_coeffi_i[12:0]	I	14	3rd Tap Filter co-efficient DPRAM read data
tap4_coeffi_i[12:0]	I	14	4th Tap Filter co-efficient DPRAM read data
tap5_coeffi_i[12:0]	I	14	5th Tap Filter co-efficient DPRAM read data
Data Input Interface			
din_valid_i	I	1	Data valid input. Indicates that the data on the input data bus is valid
r_data_i[7:0]	I	8	Red pixel data from video input
g_data_i[7:0]	I	8	Green pixel data from video input
b_data_i[7:0]	I	8	Blue pixel data from video input
line_cnt_i[10:0]	I	11	Line count input from video input module

pixel_cnt_i[10:0]	I	11	Pixel count input from video input module
Data Output Interface			
dout_valid_o	O	1	Data valid output. Indicates that the data on the output data bus is valid
r_data_o[7:0]	O	8	Red pixel data bus towards the padding/cropping module
g_data_o[7:0]	O	8	Green pixel data bus towards the padding/cropping module
b_data_o[7:0]	O	8	Blue pixel data bus towards the padding/cropping module
scalar_line_cnt_o[10:0]	O	11	Scalar line count output
scalar_pixel_cnt_o[10:0]	O	11	Scalar pixel count output