Data Sheet For Camera/HDMI Video Input Core

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24th Dec '11	Initial Version	AS
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Camera/HDMI Video Input Module. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Camera/HDMI Video Input Core:

- Core supports HSYNC and HREF mode to capture
- Core capture up to 1080p video data
- 444 RGB/YCbCr from HDMI or 422 YCbCr from Digital camera
- 24-bit pixel data from HDMI or 8-bit pixel data from Digital camera
- Supports Progressive type scan
- Programmable resolution up to 1080p
- Programmable interface timing (front and back porch)
- Programmable polarity of frame clock & line clock

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
RGB	Red Green Blue
HD	High definition
QCIF	Quarter Common Intermediate Format

2 Camera/HDMI Video Input

2.1 Block Diagram

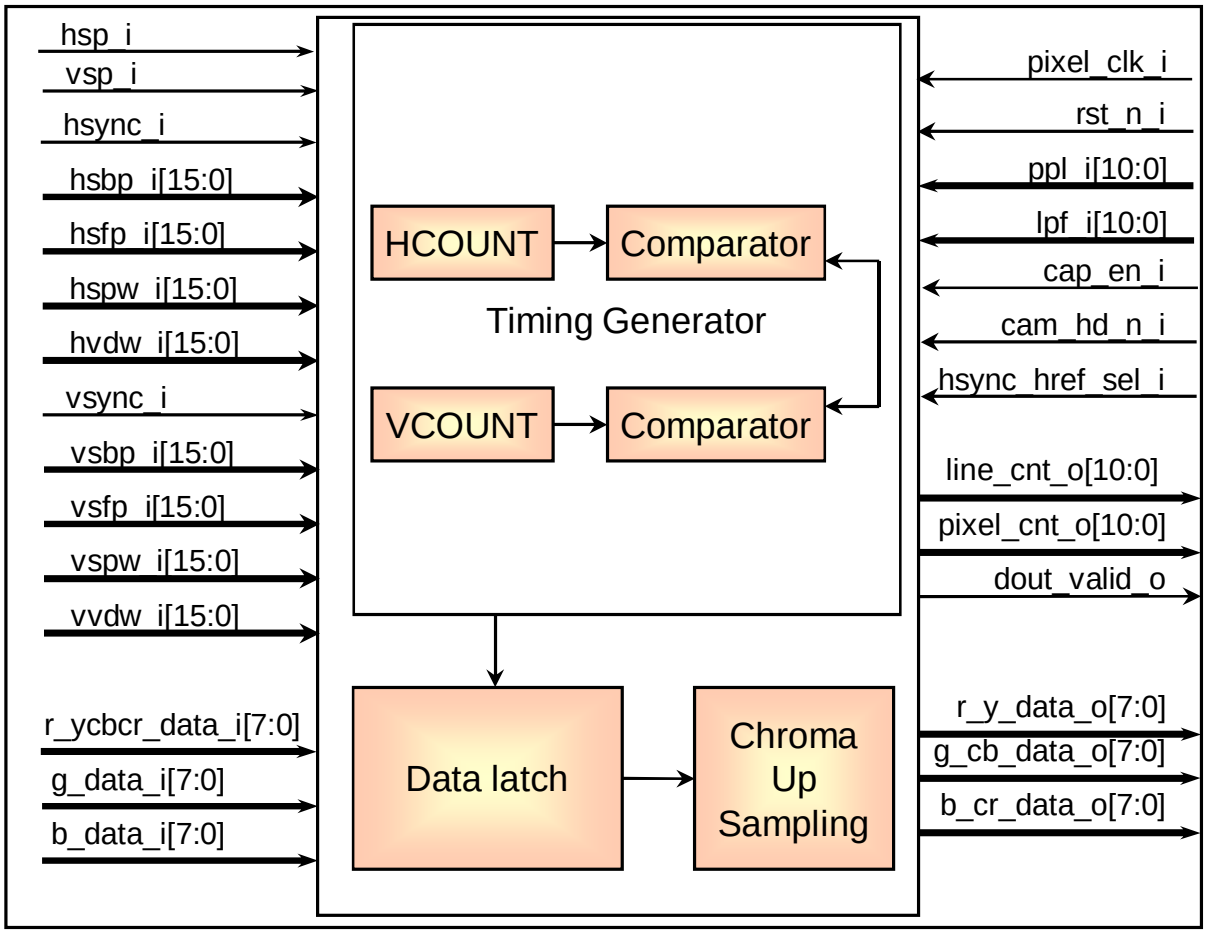

Figure 1: Camera/HDMI Video Input Block Diagram

2.2 Description

This module implements the logic required to capture the data from the capture interface according to the timing specified in control registers. Video Input block uses progressive scan inputs. It accepts 24-bit RGB data 4:4:4 format or 8-bit YCbCr data 4:2:2 format with PIXEL_CLOCK, VSYNC and HSYNC signals. When 8-bit YCbCr 4:2:2 data is captured with pixel clock then captured data is chroma up-sampled from YCbCr 4:2:2 to YCbCr 4:4:4 format. This module output is RGB 4:4:4/YCbCr 4:4:4 format.

2.3 I/O Signal Description

Table 2: Camera/HDMI Video Input IO Signal Description

Signal	I/O	Width	Description
rst_n_i	I	1	Asynchronous active low reset input.
ppl_i[10:0]	I	11	Pixels per line in capture input video
lpf_i[10:0]	I	11	Lines per frame in capture input video
Data Input Interface			
pixel_clk_i	I	1	Capture pixel clock
vsync_i	I	1	Vertical synchronization signal
hsync_i	I	1	Horizontal synchronization signal
r_ycbcr_data_i[7:0]	I	8	8-bit Red/YCbCr data input
g_data_i[7:0]	I	8	8-bit Green data input
b_data_i[7:0]	I	8	8-bit Blue data input
Register Interface			
cap_en_i	I	1	Capture enable input
cam_hd_n_i	I	1	Camera or HD/VGA input selection
hsync_href_sel_i	I	1	HSYNC/HREF mode selection
hsp_i	I	1	HSYNC Polarity Input
vsp_i	I	1	VSYNC Polarity Input
hsbp_i[15:0]	I	16	HSYNC Back Porch
hsfp_i[15:0]	I	16	HSYNC front Porch
hspw_i[15:0]	I	16	HSYNC Pulse Width
hvdw_i[15:0]	I	16	Horizontal Valid Data Width
vsbp_i[15:0]	I	16	VSYNC Back Porch
vsfp_i[15:0]	I	16	VSYNC Front Porch
vspw_i[15:0]	I	16	VSYNC Pulse Width

Signal	I/O	Width	Description
rst_n_i	I	1	Asynchronous active low reset input.
ppl_i[10:0]	I	11	Pixels per line in capture input video
lpf_i[10:0]	I	11	Lines per frame in capture input video
Data Input Interface			
pixel_clk_i	I	1	Capture pixel clock
vsync_i	I	1	Vertical synchronization signal
hsync_i	I	1	Horizontal synchronization signal
r_ycbcr_data_i[7:0]	I	8	8-bit Red/YCbCr data input
g_data_i[7:0]	I	8	8-bit Green data input
b_data_i[7:0]	I	8	8-bit Blue data input
Register Interface			
cap_en_i	I	1	Capture enable input
vvdw_i[15:0]	I	16	Vertical Valid Data Width
Data Output Interface			
dout_valid_o	O	1	Data valid output. Indicates that the data on the output data bus is valid
r_y_data_o[7:0]	O	8	8-bit Red/Luma data output
g_cb_data_o[7:0]	O	8	8-bit Green/Chroma data output
b_cr_data_o[7:0]	O	8	8-bit Blue/Chroma data output
line_cnt_o[10:0]	O	11	Present line count
pixel_cnt_o[10:0]	O	11	Present pixel position

3 Timing Waveforms

3.1 Camera YCbCr422 Input Timing

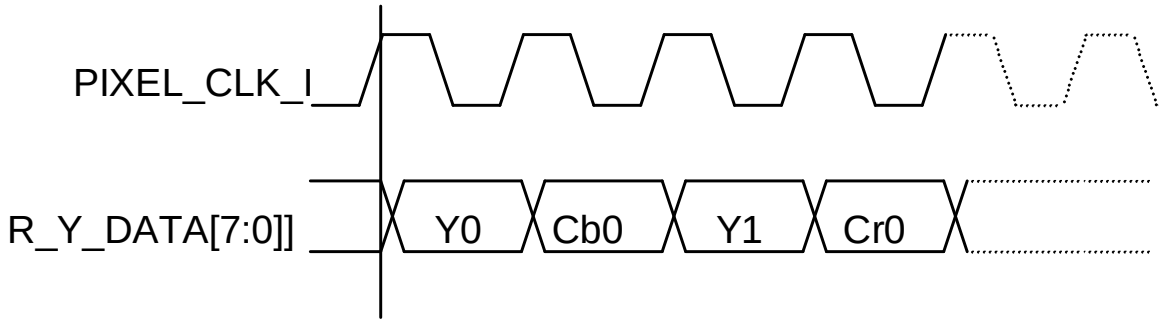

Figure 2: Camera YCbCr422 Input Timing

3.2 HD RGB444 Input Timing

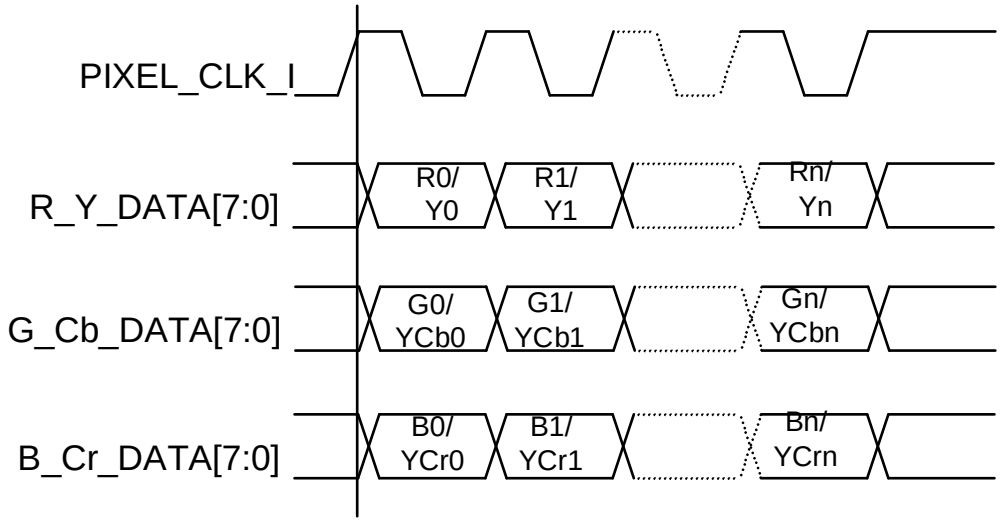

Figure 3: HD RGB444 Input Timing

3.3 Video Input Vertical Timing

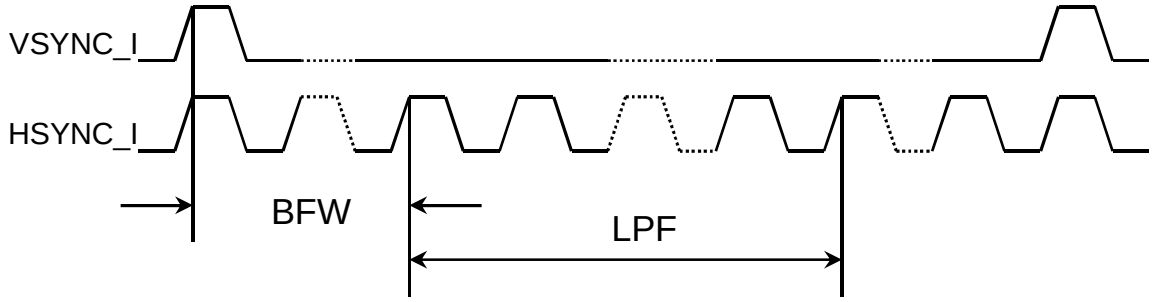

Figure 4: Video Input Vertical Timing

3.4 Video Input Horizontal Timing

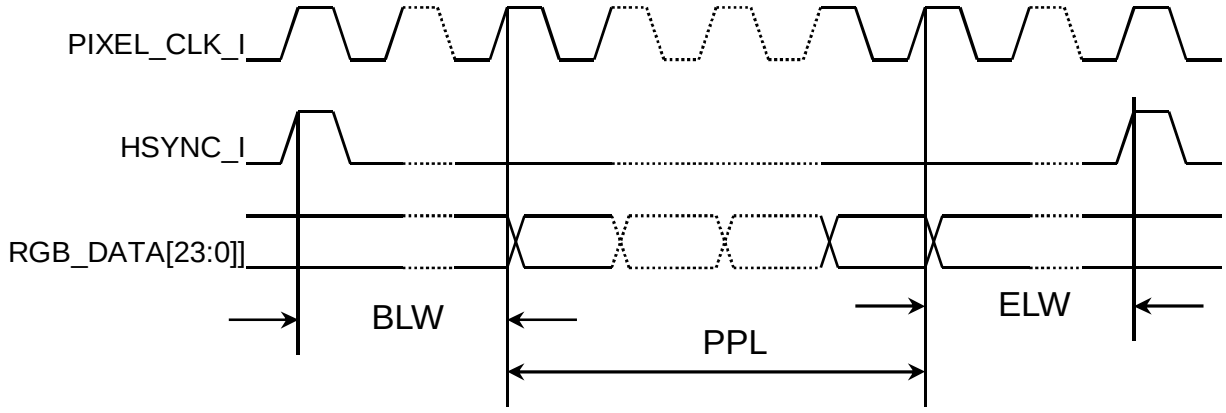

Figure 5: Video Input Horizontal Timing