

Data Sheet For Video Encoder Interface

DOCUMENT REVISION HISTORY

| Revision | Date | Change Description | Author |
|----------|----------------|--------------------------------|--------|
| 1.0 | 19th Dec, 2011 | Initial Version | PG |
| REL1.0 | 16th Aug, 2012 | Removed implementation results | VC |
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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Video Encoder Interface core. It includes the overall architectural description, detailed functional specifications and interface definitions

1.2 Features

The following lists the main features of the Video Encoder Interface Core:

- BT656 standard interface
- Parallel interface support for 10-bit
- YCbCr 4:2:2 data
- Support interlace type scan
- Support for both PAL & NTSC resolution
- Programmable polarity of frame clock & line clock

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

| Term | Meaning |
|------|-------------------------------|
| FPGA | Field Programmable Gate Array |
| FIFO | First In First Out |

2 Video Encoder Interface

2.1 Block Diagram

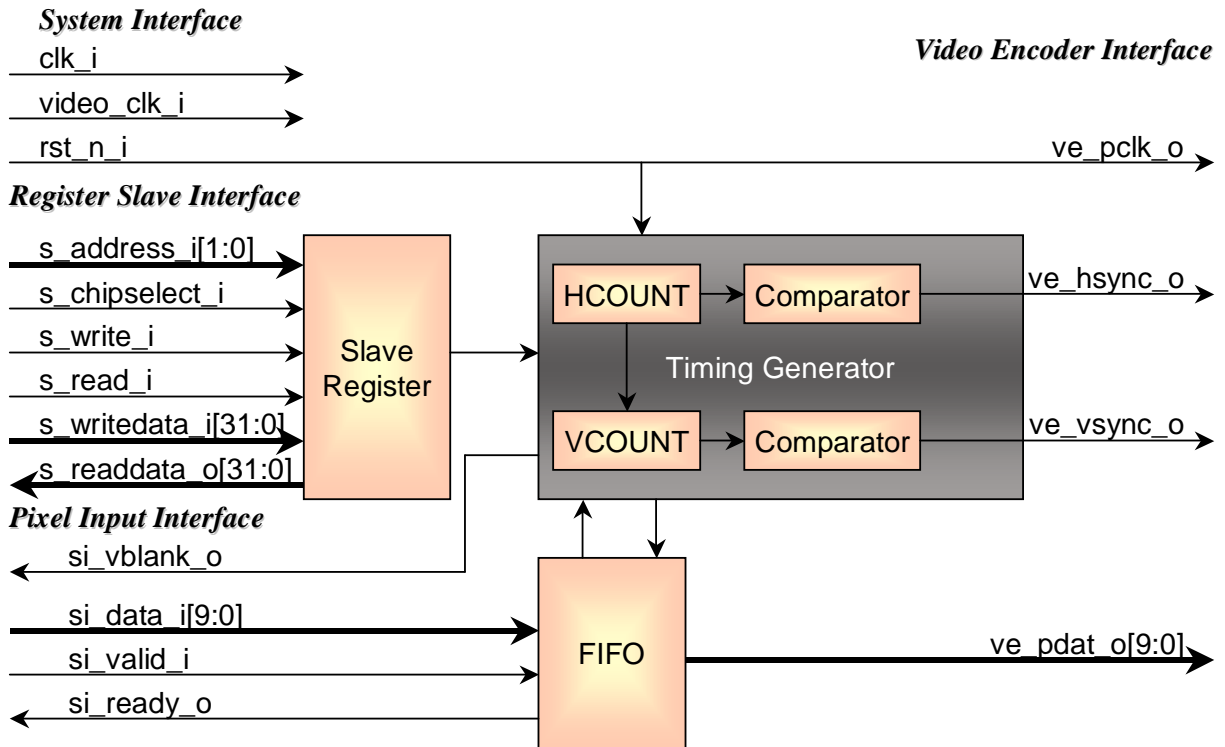


Figure 1: Video Encoder Interface Block Diagram

2.2 Description

The main blocks in Video Encoder Interface are:

- **Slave Register:** Implements all the control and timing register required for the functionality of the Video Encoder Interface.
- **Timing Generator:** This module generates all the video timing signals such as output enable, frame clock & line clock. It also controls the read of pixel data from FIFO.
- **FIFO:** This is a async FIFO which holds the pixel data in the YCbCr 4:2:2 format. The width of the FIFO is 10-bit and depth is 256.

2.3 I/O Signal Description

Table 2: System Interface IO Signals

| Signal | I/O | Width | Description |
|---------------------------------|-----|-------|---|
| <i>System Interface</i> | | | |
| rst_n_i | I | 1 | Asynchronous reset input |
| clk_i | I | 1 | Clock input |
| video_clk_i | I | 1 | Clock input |
| <i>Slave Register Interface</i> | | | |
| s_address_i[1:0] | I | 2 | Address lines from memory mapped bus |
| s_chipselect_i | I | 1 | Chip select signal to the slave |
| s_read_i | I | 1 | Read request to the slave |
| s_write_i | I | 1 | Write request to the slave |
| s_writedata_i[31:0] | I | 32 | Data lines from memory mapped bus for write transfers |
| s_readdata_o[31:0] | O | 32 | Data lines to memory mapped bus for read transfers |
| <i>Pixel Input Interface</i> | | | |
| si_data_i[9:0] | I | 10 | Pixel data input |
| si_valid_i | I | 1 | Input data valid |
| si_ready_o | O | 1 | Core ready to accept data |
| si_vblank_o | O | 1 | Vertical Blanking period status output |
| <i>Video Encoder Interface</i> | | | |
| ve_pclk_o | O | 1 | Pixel Clock |
| ve_hsync_o | O | 1 | Horizontal Synchronization Signal |

| Signal | I/O | Width | Description |
|-----------------|------------|--------------|---------------------------------|
| ve_vsync_o | O | 1 | Vertical Synchronization Signal |
| ve_pdata_o[7:0] | O | 10 | Pixel data output |

3 Timing Waveforms

3.1 Video Encoder Interface

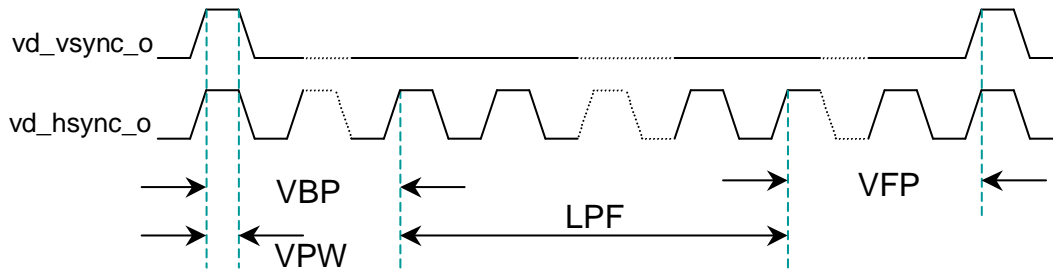


Figure 2: Video Encoder Interface Vertical Timing Diagram

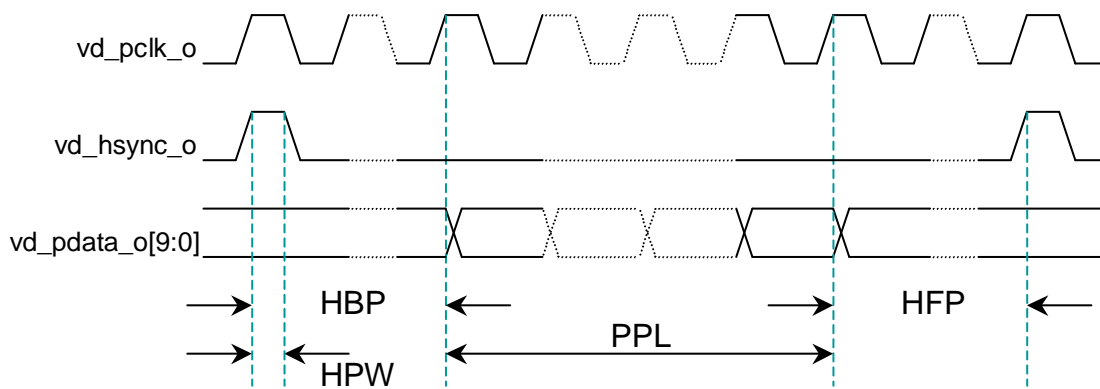


Figure 3: Video Encoder Interface Horizontal Timing Diagram

3.2 Register Slave Interface

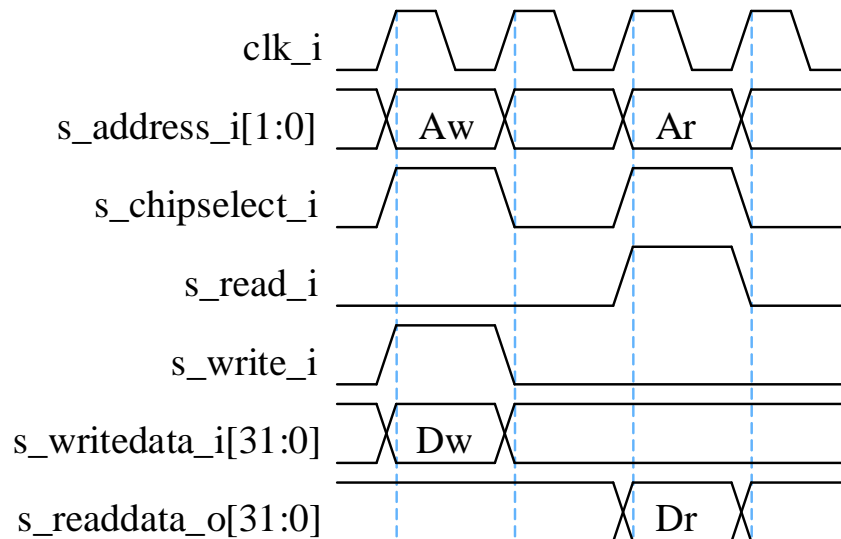


Figure 4: Slave Register Access Timing Diagram

3.3 Pixel Input Interface

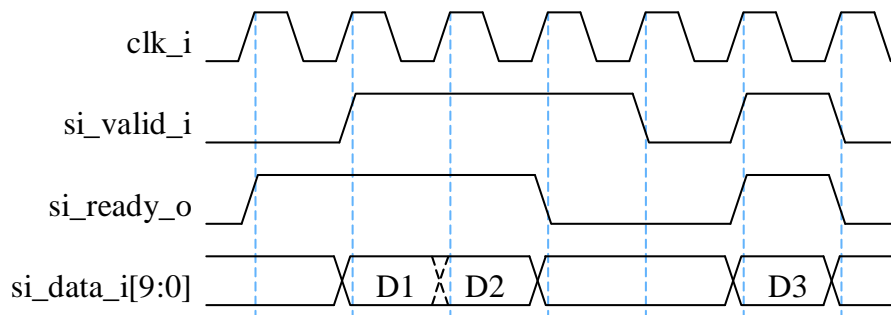


Figure 5: Pixel Input Interface Timing Diagram