Data Sheet For Video Decoder Interface

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	16th Dec '11	Initial Version	PG
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Video Decoder Interface core. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Video Decoder Interface Core:

- Supports BT601 interface
- Supports BT656 interface
- Supports both NTSC & PAL resolution
- Programmable polarity of frame clock & line clock
- Can be used to interface to Video Decoders such as ADV7180

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
FIFO	First In First Out

2 Video Decoder

2.1 Block Diagram

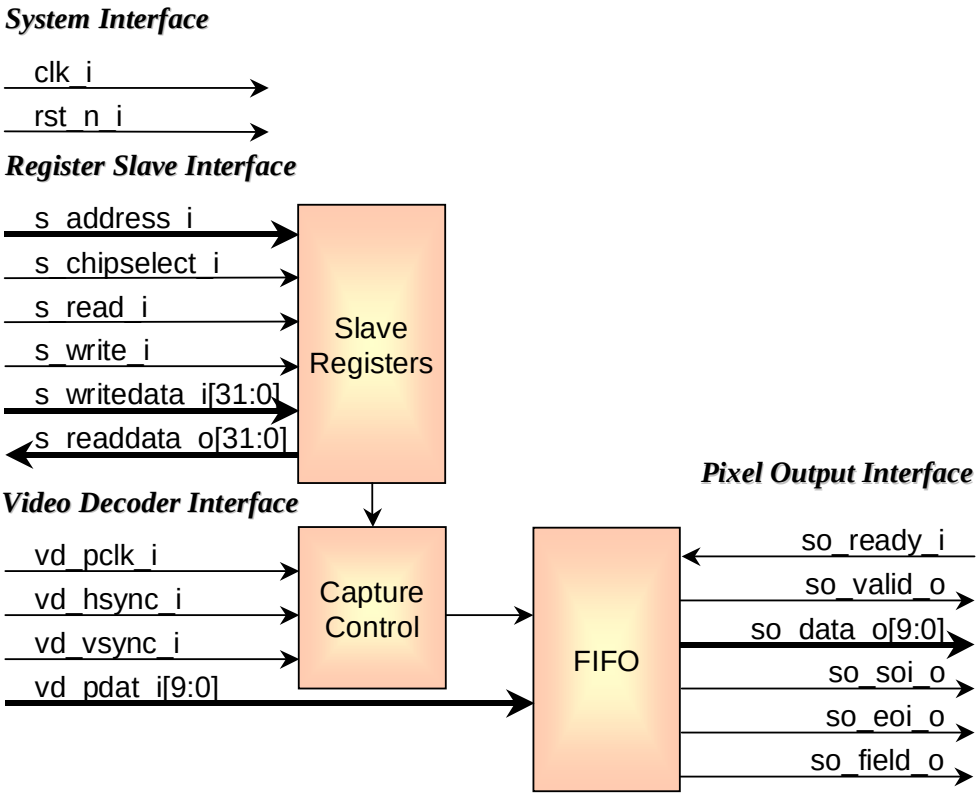

Figure 1: Video Decoder Interface Block Diagram

2.2 Description

The main blocks in Video Decoder Interface are:

- **Register Slave**: Implements all the control and timing register required for the functionality of the Video Decoder Interface.
- **Capture Control**: This is a state machine capturing the data from Video Decoder according to BT656 or nonBT656 timing.
- **FIFO**: This is a async FIFO which holds the pixel data . The width of the FIFO is 13-bit and depth is 256.

2.3 I/O Signal Description

Table 2: System Interface IO Signals

Signal	I/O	Width	Description
System Interface			
rst_n_i	I	1	Asynchronous reset input
clk_i	I	1	Clock input
Register Slave Interface			
s_address_i	I	1	Address lines from memory mapped bus
s_chipselect_i	I	1	Chip select signal to the slave
s_read_i	I	1	Read request to the slave
s_write_i	I	1	Write request to the slave
s_writedata_i[31:0]	I	32	Data lines from memory mapped bus for write transfers
s_readdata_o[31:0]	O	32	Data lines to memory mapped bus for read transfers
Pixel Output Interface			
so_ready_i	I	1	Indicates that sink device can accept data
so_valid_o	O	1	Asserted to qualify data_o lines
so_data_o[9:0]	O	10	Data signal
so_soi_o	O	1	First pixel of the image
so_eoi_o	O	1	Last pixel of the image
so_field_o	O	1	Field indication
Video Decoder Interface			

Signal	I/O	Width	Description
vd_pclk_i	I	1	Pixel clock
vd_hsync_i	I	1	Horizontal synchronization signal
vd_vsync_i	I	1	Vertical synchronization signal
vd_pdat_i[9:0]	I	10	Pixel data

3 Timing Waveforms

3.1 Video Decoder Interface

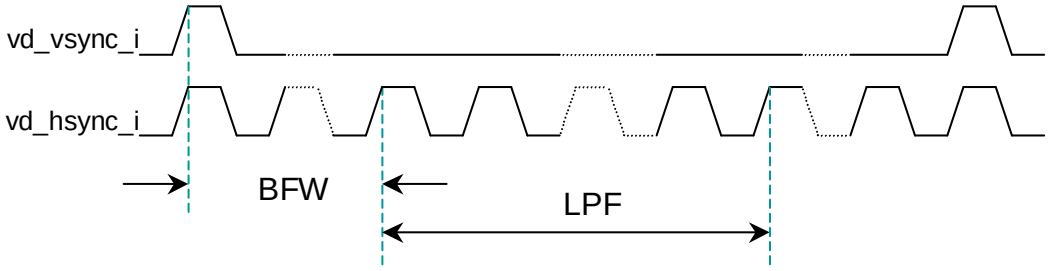

Figure 2: Video Decoder Interface Vertical Timing Diagram

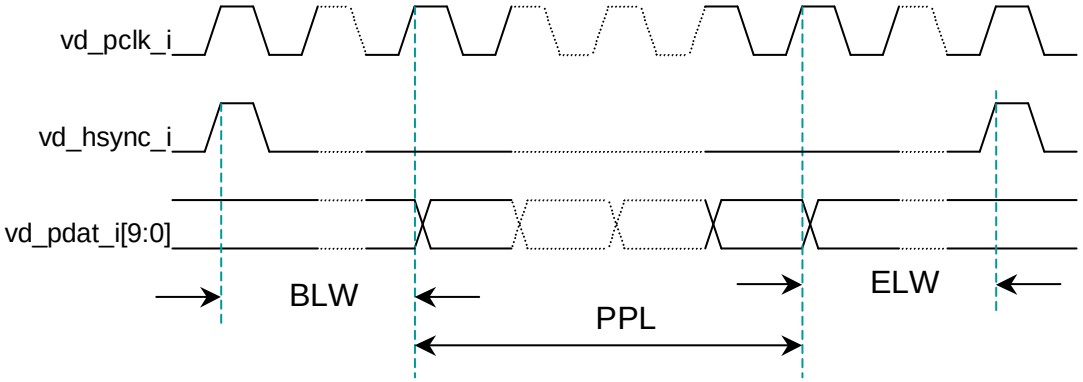

Figure 3: Video Decoder Interface Horizontal Timing Diagram

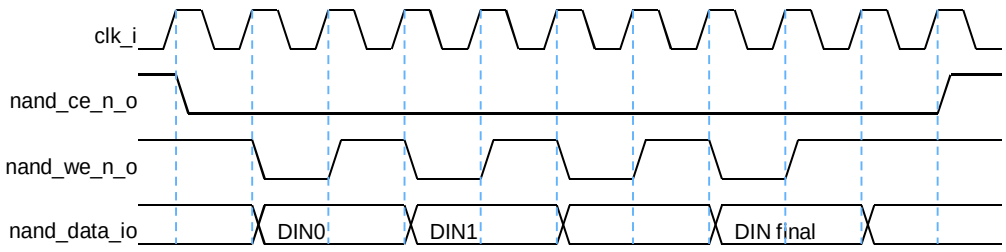

Figure 4: Data-In Cycle

3.2 Register Slave Interface

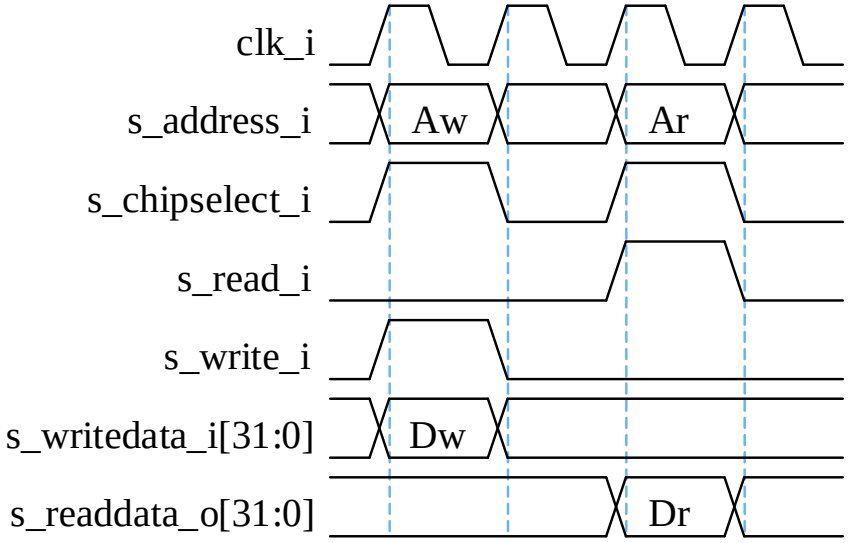

Figure 5: Slave Register Access Timing Diagram

3.3 Pixel Output Interface

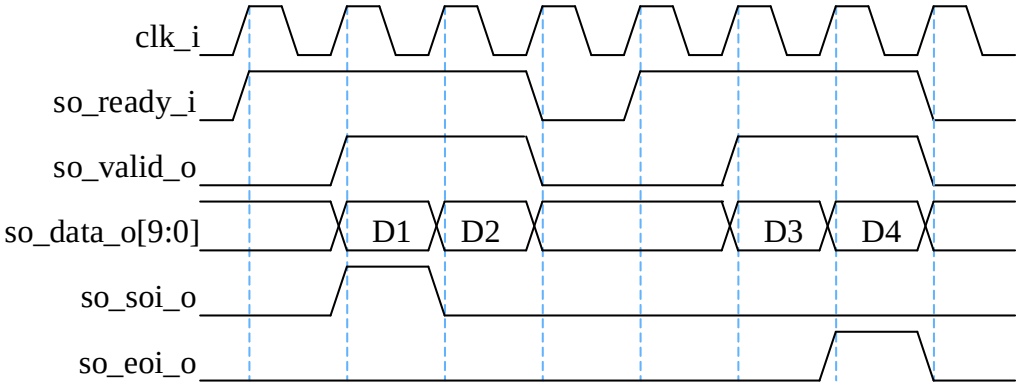

Figure 6:Pixel Output Interface Timing Diagram