

Data Sheet For Color Space Conversion Core

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24 th Dec '11	Initial Version	AS
REL 1.0	16 th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Color Space Conversion Module. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Color Space Conversion Core:

- Supports the following Color Space Converter Core :
 - YCbCr to RGB.
 - RGB to YcbCr
- Format: 4:4:4
- Image size resolution can be from QCIF to Full HD
- Coefficients are software programmable
- Pipelined multiplier
- Latency of 4 clocks
- 8-bit per pixel per color
- 3 color plane in parallel processing

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
RGB	Red Green Blue
HD	High definition
QCIF	Quarter Common Intermediate Format

2 Color Space Conversion

2.1 Block Diagram

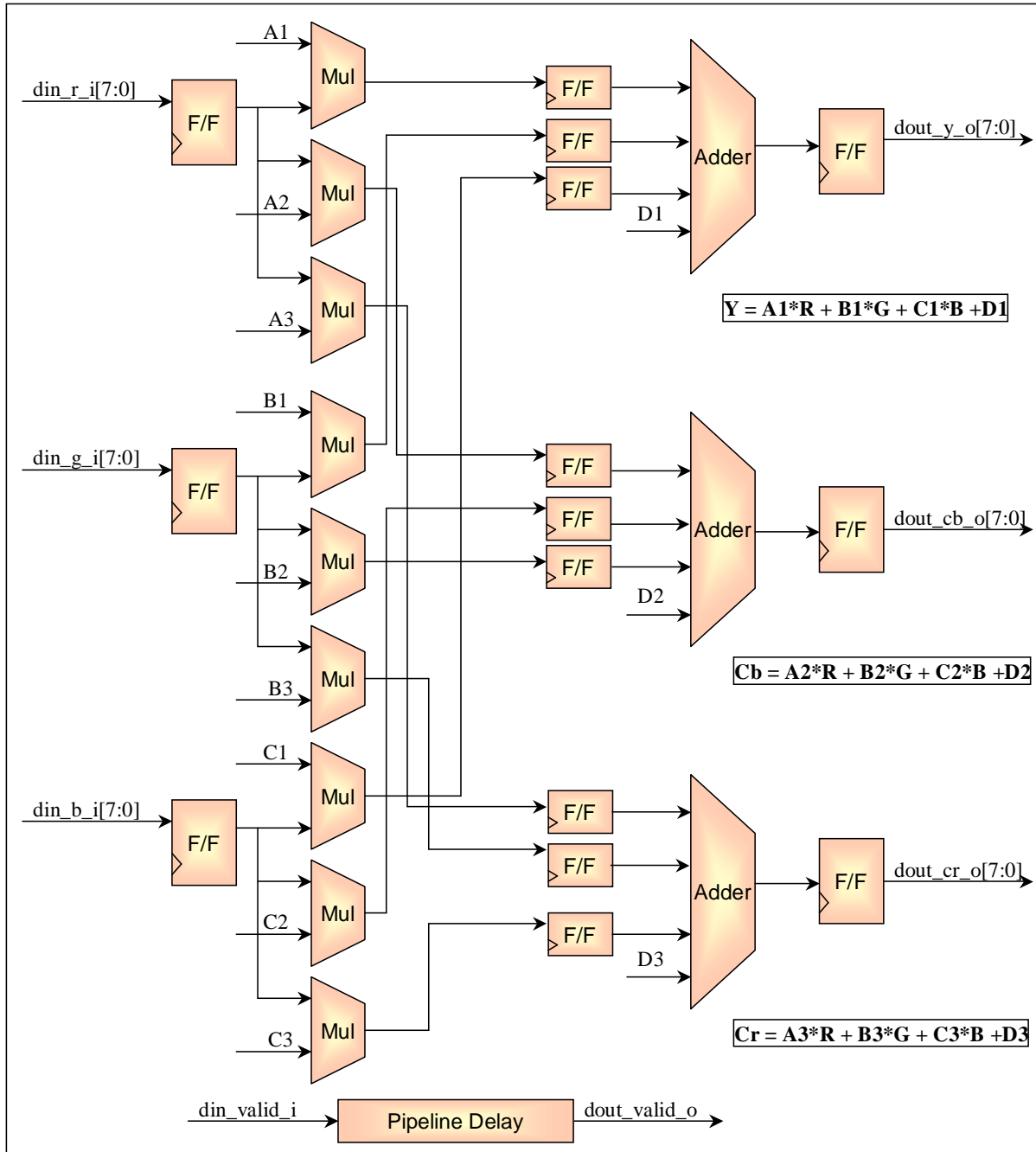


Figure 1: Color Space Conversion Block Diagram

2.2 Description

This module converts YCbCr data format to RGB format or vice versa. Following equation is used to convert from one format to other:

$$R/Y = A1*R + B1*G + C1*B + D1$$

$$G/Cb = A2*R + B2*G + C2*B + D2$$

$$B/Cr = A3*R + B3*G + C3*B + D3$$

The coefficients A1, B1, .., C3 and D3 are real numbers. These coefficients are programmable from processor.

The RGB/YCbCr data will be saturated at 0 and 255 levels if there underflow or overflow respectively.

2.3 I/O Signal Description

Table 2: Color Space Conversion IO Signals

Signal	I/O	Width	Description
clk_i	I	1	Clock input
rst_n_i	I	1	Asynchronous active low reset input.
Data Input Interface			
din_valid_i	I	1	Data valid input. Indicates that the data on the input data bus is valid
din_r_i[7:0]	I	8	Input data bus carrying input format pixel data
din_g_i[7:0]	I	8	Input data bus carrying input format pixel data
din_b_i[7:0]	I	8	Input data bus carrying input format pixel data
Data Output Interface			
dout_valid_o	O	1	Data valid output. Indicates that the data on the output data bus is valid
dout_y_o[7:0]	O	8	Output data bus carrying output format samples
dout_cb_o[7:0]	O	8	Output data bus carrying output format samples
dout_cr_o[7:0]	O	8	Output data bus carrying output format samples