## DOCUMENT REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Change Description</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>24th Dec ‘11</td>
<td>Initial Version</td>
<td>AS</td>
</tr>
<tr>
<td>REL 1.0</td>
<td>16th Aug ‘12</td>
<td>Removed implementation results</td>
<td>VC</td>
</tr>
</tbody>
</table>

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1 Introduction

1.1 Purpose
This document describes the Technical Specification of the Color Space Conversion Module. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features
The following lists the main features of the Color Space Conversion Core:

- Supports the following Color Space Converter Core:
  - YCbCr to RGB.
  - RGB to YcbCr
- Format: 4:4:4
- Image size resolution can be from QCIF to Full HD
- Coefficients are software programmable
- Pipelined multiplier
- Latency of 4 clocks
- 8-bit per pixel per color
- 3 color plane in parallel processing

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

<table>
<thead>
<tr>
<th>Term</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
</tr>
<tr>
<td>RGB</td>
<td>Red Green Blue</td>
</tr>
<tr>
<td>HD</td>
<td>High definition</td>
</tr>
<tr>
<td>QCIF</td>
<td>Quarter Common Intermediate Format</td>
</tr>
</tbody>
</table>
2 Color Space Conversion

2.1 Block Diagram

![Block Diagram of Color Space Conversion](image)

\[
Y = A1R + B1G + C1B + D1
\]

\[
Cb = A2R + B2G + C2B + D2
\]

\[
Cr = A3R + B3G + C3B + D3
\]

Figure 1: Color Space Conversion Block Diagram
2.2 Description

This module converts YCbCr data format to RGB format or vice versa. Following equation is used to convert from one format to other:

\[
\begin{align*}
R/Y &= A1*R + B1*G + C1*B + D1 \\
B/Cr &= A3*R + B3*G + C3*B + D3 \\
\end{align*}
\]

The coefficients \( A1, B1, \ldots, C3 \) and \( D3 \) are real numbers. These coefficients are programmable from processor.

The RGB/YCbCr data will be saturated at 0 and 255 levels if there underflow or overflow respectively.
### 2.3 I/O Signal Description

**Table 2: Color Space Conversion IO Signals**

<table>
<thead>
<tr>
<th>Signal</th>
<th>I/O</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk_i</td>
<td>I</td>
<td>1</td>
<td>Clock input</td>
</tr>
<tr>
<td>rst_n_i</td>
<td>I</td>
<td>1</td>
<td>Asynchronous active low reset input.</td>
</tr>
<tr>
<td><strong>Data Input Interface</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>din_valid_i</td>
<td>I</td>
<td>1</td>
<td>Data valid input. Indicates that the data on the input data bus is valid</td>
</tr>
<tr>
<td>din_r_i[7:0]</td>
<td>I</td>
<td>8</td>
<td>Input data bus carrying input format pixel data</td>
</tr>
<tr>
<td>din_g_i[7:0]</td>
<td>I</td>
<td>8</td>
<td>Input data bus carrying input format pixel data</td>
</tr>
<tr>
<td>din_b_i[7:0]</td>
<td>I</td>
<td>8</td>
<td>Input data bus carrying input format pixel data</td>
</tr>
<tr>
<td><strong>Data Output Interface</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>dout_valid_o</td>
<td>O</td>
<td>1</td>
<td>Data valid output. Indicates that the data on the output data bus is valid</td>
</tr>
<tr>
<td>dout_y_o[7:0]</td>
<td>O</td>
<td>8</td>
<td>Output data bus carrying output format samples</td>
</tr>
<tr>
<td>dout_cb_o[7:0]</td>
<td>O</td>
<td>8</td>
<td>Output data bus carrying output format samples</td>
</tr>
<tr>
<td>dout_cr_o[7:0]</td>
<td>O</td>
<td>8</td>
<td>Output data bus carrying output format samples</td>
</tr>
</tbody>
</table>