Data Sheet for ARINC 818-2 IP Core

iW-EMELW-DS-01-R1.0

REL1.0

10th May. '18

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DOCUMENT IDENTIFICATION

Project Name	ARINC 818-2 IP Core
Document Name	iW-EMELW-DS-01-R1.0-REL1.0-FPGA.pdf
Document Home	iWave Server
Revision No	R1.0/REL1.0

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author	Reviewer
R1.0/REL1.0	10th May. '18	Initial Release	Abhishek	Sheik

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of ARINC818-2 IP Core. It includes the overall architectural description, functional specifications and interface definitions of the coré.

1.2 Features

The following are the main features of the ARINC818-2 IP:

- Streaming Interface used as Video transmit and receive interface, which provide high throughput video transfer.

- Video Input Format Supported
    - Resolution depends on the FPGA transceiver speed used for implementation.
    - For SXGA (1280x1024@60Hz) resolution, required data rate is 2.5Gbps**

- Pixel Format supported.
    - Monochrome
    - RGB
    - YcbCr
    - RGBA

- Pixel Aspect ratio supported.
    - 1:1
    - 1:1.2
    - 1.2:1
    - NTSC (approx 8:9)
    - PAL (16:15)

- Frame Rate supported.
    - 15fps
    - 20fps
    - 24
    - 24 * 1000 / 1001
    - 25 (PAL)
    - 30
    - 30 * 1000 / 1001 (29.97 NTSC)
    - 60
    - 50
    - 60 * 1000 / 1001 (59.94 NTSC)

- 50 (VESA DMT)
- 60 (VESA DMT)
- 75 (VESA DMT)
- 85 (VESA DMT)
- 50 (VESA CVT)
- 60 (VESA CVT)
- 75 (VESA CVT)
- 85 (VESA CVT)

- Pixel Table Number supported
  - 8-bit Components, four components per transmission word
- Pixel Array Order supported
  - Left to Right, Top to Bottom
- Line Synchronous Mode supported
- 32-bit Full Image CRC supported
- Following parameters will be expected from user
  - No. Of rows
  - No. Of Columns
  - Video Format Code
  - Video Frame rate
  - Pixel Aspect Ratio
  - Color Information Code for Transmitter
  - VSYNC_POLARITY
  - TX_DEST_ID
  - TX_SRC_ID
  - RX_DEST_ID
  - RX_SRC_ID
  - Vertical Backporch
  - Horizontal Total number of pixel

** 1280 pixels/row x 1024 rows x 8 bits/element gray scale x 3 elements/pixel x 60 Hz refresh x 1.25 8B/10B x 1.05 (typical FC-AV protocol overhead) is approximately equal to 2.5 Gbps

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
ADVB	Avionics Digital Video Bus
FPGA	Field Programmable Gate Array
FIFO	First In First Out
RGB	Red Green Blue

2 Architecture

2.1 Block Diagram

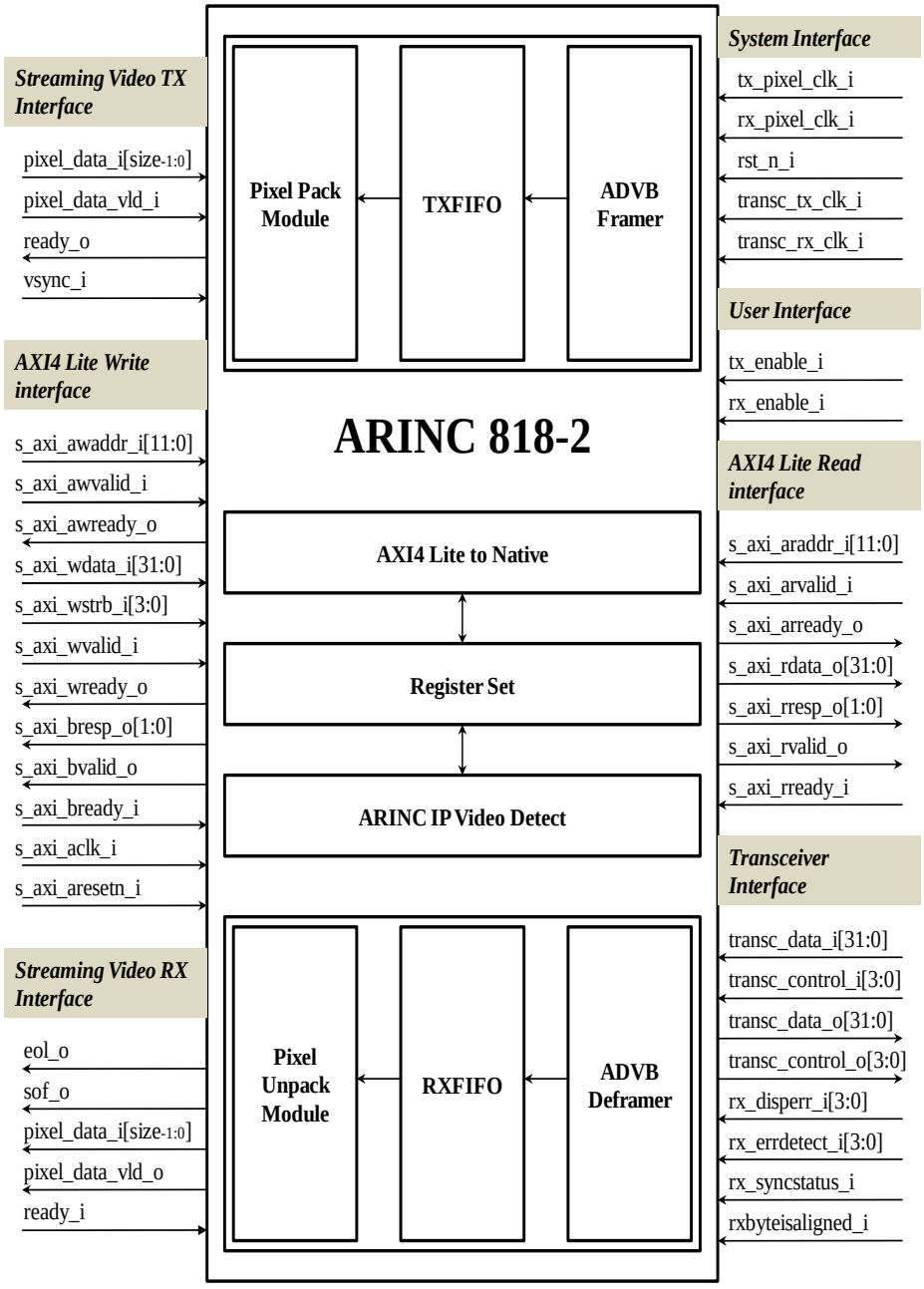

Figure 1: ARINC818-2 Block Diagram

2.2 Description

The main blocks of ARINC 818-2 IP Core are given below

This design expect following data from user.

- No. Of rows
- No. Of Columns
- Video Format Code
- Video Frame rate
- Pixel Aspect Ratio
- Color Information Code for Transmitter
- VSYNC_POLARITY
- TX_DEST_ID
- TX_SRC_ID
- RX_DEST_ID
- RX_SRC_ID
- Vertical Backporch
- Horizontal Total number of pixel

- **Pixel Pack Module:** This module will capture supported resolution/format video data, pack it as per color format and generates valid and send towards Transmit FIFO.

- **TX_FIFO:** This module is used to store the video data captured. The size of the FIFO is configured depending on resolution. Asynchronous FIFO is used to store the each line pixel data.

- **ADVB Framer:** This module is used to frame the video data in ADVB frame structure and sends to transceiver interface. The module will get the header and object0 Frame information from register block and payload data from FIFO. CRC generation will be done in this block.

- **ADVB Deframer Module:** This module is receiving the ADVB frame from the transceiver interface. Extracts header and object 0 frame information from the frame and stores in register block. Similarly extract the pixel data from the frame payload data field and store the same in Receive FIFO. In this block CRC checking will be done.

- **RX_FIFO:** Asynchronous FIFO is used to store the video data extracted from the ADVB frame. The size of the FIFO is configured depending on resolution

- **Pixel Unpack Module:** This module will read the data from the receive FIFO and as per color format unpack it and send to Video RX interface.

- **AXI4 Lite to Native**: This module converts AXI4 lite interface to native interface.

- **Register Set**: This module defines the user accessible registers. Software has the capability to write to or read from these registers by giving request over the AXI4 Lite interface.

- **ARINC IP Video Detect**: Main functionality of this module is to check the presence of valid video data in ARINC IP receive path. It also helps the re-initialization of ARINC IP and Xilinx video IPs to recover from error state.

2.3 IO Signals

Table 2: System Interface IO Signals

Signal	Dir	Width	Description
tx_pixel_clk_i	I	1	Pixel clock Frequency. Clock from Video source to transmitter interface
rx_pixel_clk_i	I	1	Pixel clock Frequency. Clock from Video Sink to receiver Interface.
transc_tx_clk_i	I	1	Transceiver clock Frequency at which framing will be done.
transc_rx_clk_i	I	1	Transceiver clock Frequency at which de-framing will be done.
rst_n_i	I	1	Active low Reset input

Table 3: User Interface IO Signals

Signal	Dir	Width	Description
rx_enable_i	I	1	For capturing frame, keep this asynchronous signal always high or set rx_enable bit in Transmit receive enable register using AXI Lite interface.
tx_enable_i	I	1	For transmitting frame, keep this asynchronous signal always high or set tx_enable bit in Transmit receive enable register using AXI Lite interface.

Table 4: Streaming Video TX Interface IO Signals

Signal	Dir	Width	Description
pixel_data_i	I	SIZE	Pixel data. Synchronous with tx_pixel_clk_i.
ready_o	O	1	Data ready signal. When this signal asserts source will send data with valid.
pixel_data_vld_i	I	1	Pixel data valid.
vsync_i	I	1	VSYNC signal. When vsync is detected, container will be send.

Table 5: Streaming Video RX Interface IO Signals

Signal	Dir	Width	Description
pixel_data_o	O	SIZE	Deframed Video Data signal
pixel_dvld_o	O	1	Deframed Video Data Valid signal.
ready_i	I	1	Data receive ready. When this signal assert, data will be send with valid.
sof_o	O	1	Start of frame signal.
eol_o	O	1	End of line output.

Table 6: Transceiver Interface IO Signals

Signal	Dir	Width	Description
transc_data_o	O	32	Transmit data to Transceiver interface
transc_control_o	O	4	8B/10B encoder /Kx.y/ or /Dx.y/ control When asserted high, the 8B/10B encoder encodes the data on the tx_data port as a /Kx.y/ control code group. When de-asserted low, it encodes the data on the tx_data port as a /Dx.y/ data code group.
transc_data_i	I	32	Receive data
transc_control_i	I	4	8B/10B decoder /Kx.y/ or /Dx.y/ control indication
rx_disperr_i	I	4	This signal asserted when a disparity error occurs.
rx_errdetect_i	I	4	This signal asserts when there is 8b/10B code error or disparity error.
rx_syncstatus_i	I	1	Sync status signal. 1: Link is up.
rxbyteisaligned_i	I	1	This signal become high when transceiver is byte aligned

Table 7: AXI4 Lite Interface IO Signals

Signal	Dir	Width	Description
s_axi_aclk_i	I	1	AXI4 lite interface clock
s_axi_aresetn_i	I	1	Asynchronous reset.
s_axi_awaddr_i	I	12	Write address.
s_axi_awvalid_i	I	1	Write address valid input.
s_axi_awready_o	O	1	Write address ready output.
s_axi_wdata_i	I	32	Write data input.
s_axi_wstrb_i	I	4	Write strobes input.
s_axi_wvalid_i	I	1	Write data valid input.
s_axi_wready_o	O	1	Write data ready output.
s_axi_bresp_o	O	2	Write response output.
s_axi_bvalid_o	O	1	Write response valid output.
s_axi_bready_i	I	1	Write response ready input.
s_axi_araddr_i	I	12	Read address.
s_axi_arvalid_i	I	1	Read address valid input.
s_axi_arready_o	O	1	Read address ready output.
s_axi_rdata_o	O	32	Read data output.
s_axi_rresp_o	O	2	Read response output.

Signal	Dir	Width	Description
s_axi_rvalid_o	O	1	Read valid output.
s_axi_rready_i	I	1	Read ready input.

**SIZE– Size depends on the video color information code. This is 24-bit for RGB

3 Resource Utilization

The table below shows the resource utilization summary of ARINC 818-2 IP Core in Xilinx and Altera FPGAs.

Table 8: Resource Utilization in Xilinx KC705

	KC705		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
LUT	1302	203800	0.64
LUTRAM	2	64000	0.003125
FF	1308	407600	0.32
BRAM	4	445	0.9
DSP	1	840	0.12

Table 9: Resource Utilization in Xilinx AC701

	AC701		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
LUT	1305	134600	0.97
LUTRAM	2	46200	0.0043290043
FF	1308	269200	0.49
BRAM	4	365	1.1
DSP	1	740	0.14

Table 10: Resource Utilization in Xilinx KCU105

	KCU105		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
LUT	1314	242400	0.54
LUTRAM	2	112800	0.0017730497
FF	1282	484800	0.26
BRAM	4	600	0.67
DSP	1	1920	0.05

Table 11: Resource Utilization in Xilinx ZC706

	ZC706		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
LUT	1303	218600	0.6
LUTRAM	2	70400	0.0028409092
FF	1308	437200	0.3
BRAM	4	545	0.73
DSP	1	900	0.11

Table 12: Resource Utilization in Altera Cyclone V

	Cyclone V		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
Combinational ALUTs	1194	-	-
ALMs	724	56480	0.0128
LABs	96	5648	0.017
Logic Registers	834	225920	0.73
Memory Bits	278528	14049280	0.02

Table 13: Resource Utilization in Altera Arria 10

	Arria 10		
RESOURCE	**UTILIZATION**	**AVAILABLE**	**UTILIZATION %**
Combinational ALUTs	1,193	-	-
ALMs	746	427,200	0.0017
LABs	103	42,720	0.0024
Logic Registers	814	1708800	0.0004
Memory Bits	299008	111124480	0.002