Data Sheet For Alpha Blender

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	16th Dec '11	Initial Version	PG
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the Alpha Blender core. It includes the overall architectural description, detailed functional specifications and interface definitions.

1.2 Features

The following lists the main features of the Alpha Blender Core:

- Blend 2 video source
- Pipelined multiplier
- Latency of 4 clocks

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array

2 Alpha Blender

2.1 Block Diagram

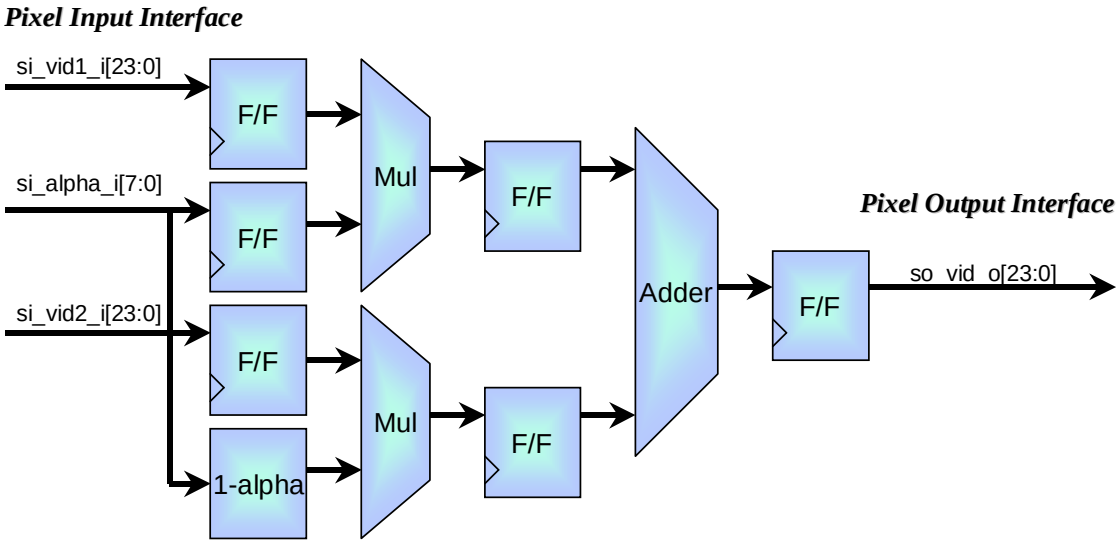

Figure 1: Alpha Blender Block Diagram

2.2 Description

The Alpha Blender module blend 2 different video source. Following is the equation

dout_o = alpha*din1 + (1-alpha)* din2.

The value of alpha (1 ≥ alpha ≥ 0) will be programmable from processor. The alpha bender's output has 4 clock cycles latency.

2.3 I/O Signal Description

Table 2: Alpha Blender IO Signal Description

Signal	I/O	Width	Description
System Interface			
rst_n_i	I	1	Asynchronous reset input
clk_i	I	1	Clock input
Pixel Input Interface			
si_vid1_i[23:0]	I	24	Video1 data input
si_vid2_i[23:0]	I	24	Video2 data input
si_alpha_i[7:0]	I	8	Alpha data input
si_valid_i	I	1	Data valid on input bus
Pixel Output Interface			
so_vid_o[23:0]	O	24	Blended video red color output
so_valid_o	O	1	Data valid in output data bus

3 Timing Waveforms

3.1 Pixel Input & Output Interface

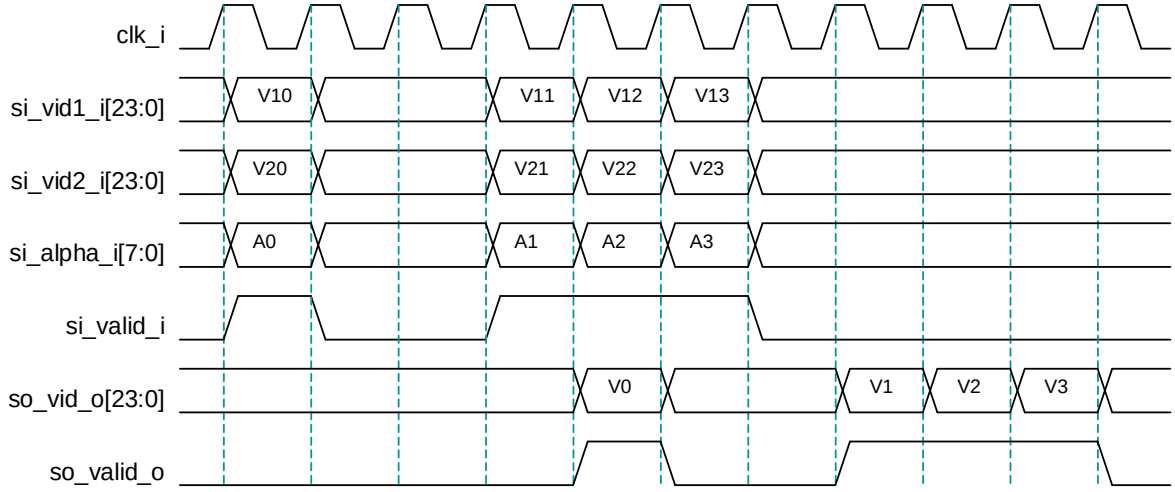

Figure 2: Pixel Input & Output Interface Timing Diagram