Data Sheet For MMC Host Controller

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
R1.0REL1.0	22nd April'11	Initial Version	Preeti.N
R1.0REL1.1	22nd Aug'11	Added support for ADMA	Preeti.N
R1.0REL1.2	29th Oct'11	IO Signal naming & timing diagram updated	Preeti.N

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1. General Description

This MMC host controller supports 1-bit, 4-bit,8-bit memory card interface. This allows 1-bit, 4-bit SD/MMC transaction and 8-bit MMC transactions. The device conforms to the SD Host Standard Specification Version 2.0 and also supports MMC specification 4.3 version. This manages the physical layer of SD, MMC protocols and can be used together with SD Host Standard compatible driver software to add SD/MMC host functionality to a variety of microprocessor systems.

Processor interface is used here for connecting processor. Processor interface module consists Register block, through which the Host Driver software can configure the host controller and initiate transactions to and from an SD/MMC target. This consists 2 KB data buffer allows for a low interrupt latency time and efficient communication with the host processor at high data rates. The MMC Host controller also supports ADMA functionality to off-load the host processor for data transfer and increase overall system performance. An additional clock divider is used for generating required clock frequency for internal logic, which enables the user to achieve the maximum desired clock speed from the external clock source.

2. Features

The following are the main features of the MMC Host Controller:

- Compliant with SD Host Controller Standard Specification Version 2.0
- Compliant with SD Physical Layer Specification Version 2.0
- Compliant with MMC Specification Version 4.41
- Supports 1-bit,4-bit SD/MMC modes and 8-bit MMC modes.
- Supports SD Card Detection input pin
- Supports SD Card Write Protection input pin
- Supports programmable clock frequency generation to the SD/MMC card.
- Supports Interrupt and ADMA2 transfer mode of operation.
- Individual 2Kbyte data buffer for read and write.
- Cyclic Redundancy Check (CRC) for command and data.
- Supports timeout monitoring for response, data, CRC token & busy.
- Supports a maximum block length of 2Kbyte.
- Supports both single block and multi block data transfer.
- Supports power ON/OFF control to SD/MMC card.
- Supports 32-bit synchronous memory interface towards host processor

3. Block Diagram

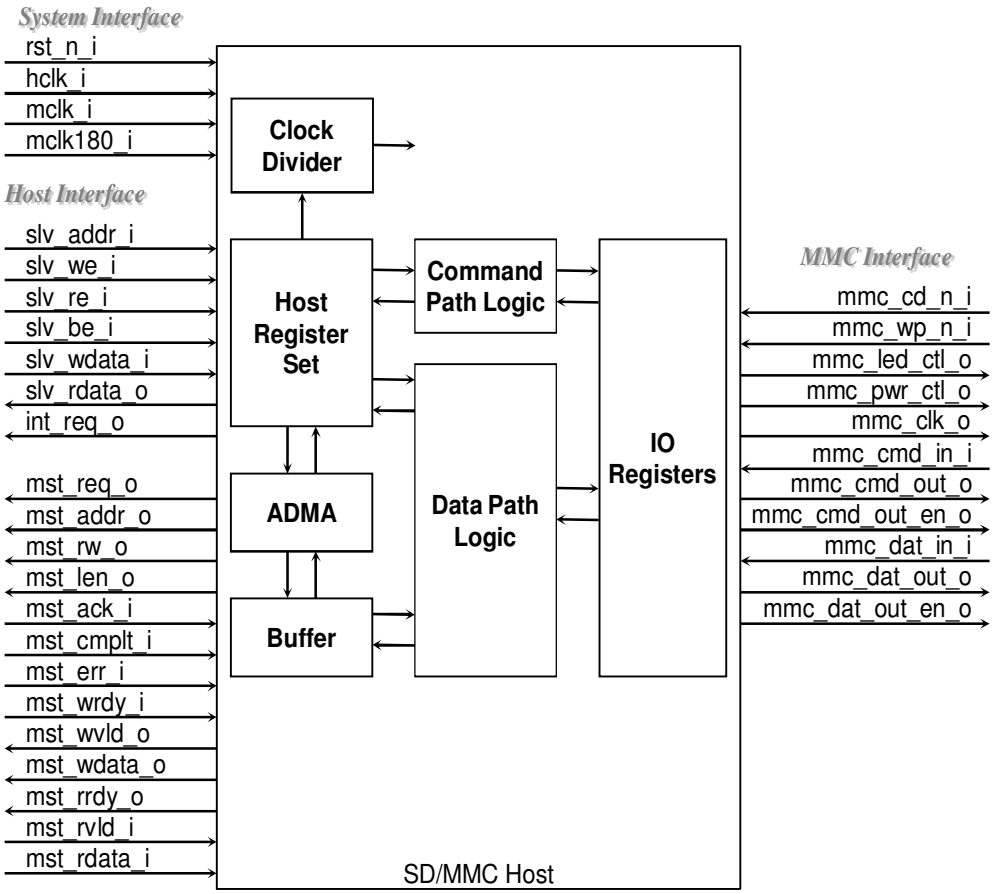

Figure 1: MMC Host Controller Block Diagram

4. IO Signals

Table 1:System Interface IO Signals

Signal	Dir	Width	Description
rst_n_i	I	1	Asynchronous reset
hclk_i	I	1	Host Processor Interface clock

Signal	Dir	Width	Description
mclk_i	I	1	MMC base clock This clock is used as base clock to MMC side logic
mclk180_i	I	1	MMC base clock inverted

Table 2: Host Processor Interface IO Signals

Signal	Dir	Width	Description
Host Processor Interface Slave			
slv_addr_i	I	8	Address bus
slv_we_i	I	1	Write enable
slv_re_i	I	1	Read enable
slv_be_i	I	4	Byte enable
slv_wdata_i	I	32	Write data bus
slv_rdata_o	O	32	Read data bus
int_req_o	O	1	Interrupt request When HIGH indicates there is request for interrupt from the IP
Host Processor Interface Master			
mst_req_o	O	1	Transfer Request When HIGH indicates ADMA wants to do data transfer
mst_addr_o	O	32	Transfer Address Indicates the system address from/to which data transfer need to be done.
mst_rw_o	O	1	Transfer direction 0 – write transfer 1 – read transfer

Signal	Dir	Width	Description
Host Processor Interface Slave			
mst_len_o	O	10	Transfer length 0x1 = 1DWORD 0x2 = 2 DWORDS . . 0x3FF = 1023 DWORDS 0x0 = 1024 DWORDS
mst_ack_i	I	1	Transfer acknowledge
mst_cmplt_i	I	1	Transfer Complete
mst_err_i	I	1	Transfer error
mst_wrdy_i	I	1	Ready to accept write data
mst_wvld_o	O	1	Write data valid
mst_wdata_o	O	32	Write data bus
mst_rrdy_o	O	1	Ready to accept read data
mst_rvld_i	I	1	Read data valid
mst_rdata_i	I	32	Read data bus

Table 3: MMC Interface IO Signals

Signal	Dir	Width	Description
mmc_cd_n_i	I	1	Card Detect Connected to card detect switch of SD connector
mmc_wp_n_i	I	1	Write Protect Connected to write protect switch of SD connector

Signal	Dir	Width	Description
mmc_led_ctl_o	O	1	LED Control 0 – LED OFF 1 – LED ON
mmc_pwr_ctl_o	O	1	Power Control 0 – Power OFF 1 – Power ON
mmc_clk_o	O	1	Clock
mmc_cmd_in_i	I	1	Command Line input
mmc_cmd_out_o	O	1	Command line output
mmc_cmd_out_en_o	O	1	Command line output enable
mmc_dat_in_i	I	8	Data Line input
mmc_dat_out_o	O	8	Data line output
mmc_dat_out_en_o	O	8	Data line output enable

5. Functional Description

The main blocks in MMC Host Controller are:

- **Host Register Set**: This module implements the register set as per SD Host specification 2.0. It also implements debounce logic for card detect signal..
- **Command Path**: This module implements logic required to send command and receive response from SD/MMC card. It also instantiates 7-bit CRC generation circuit used for protection of command.
- **Data Path**: This module implements logic required to send and receive data from SD/MMC card. It also instantiates 16-bit CRC generation circuit to each data line used for protection of data.
- **Buffer:** This module implements 2Kbyte buffer to store read and write data.

- **ADMA:** This module implements scatter gather DMA logic used for data transfer between system memory and memory card.
- **Clock Divider:** This module generates and controls the different clock frequencies, required for MMC side logic.
- **MMC IO Register module:** This module implements necessary registers for MMC IO signals.

6. Standard Host Register Overview

The Register list of the MMC device is as shown in 4 below.

These Registers can be accessed by the MMC Host.

Table 4: MMC Host Controller Register Map

Sl. No	Registers	Width	Address Offset
1.	Block Size Register	16	0x04
2.	Block Count Register	16	0x06
3.	Argument Register	32	0x08
4.	Transfer Mode Register	16	0x0C
5.	Command Register	16	0x0E
6.	Response0 Register	32	0x10
7.	Response2 Register	32	0x14
8.	Response4 Register	32	0x16
9.	Response6 Register	32	0x1C
10.	Buffer Data Port Register	32	0x20
11.	Present State Register	32	0x24
12.	Host Control Register	8	0x28
13.	Power Control Register	8	0x29
14.	Clock Control Register	16	0x2C
15.	Timeout Control Register	8	0x2E
16.	Software Reset Register	8	0x2F
17.	Normal Interrupt Status Register	16	0x30
18.	Error Interrupt Status Register	16	0x32

Sl. No	Registers	Width	Address Offset
19.	Normal Interrupt Status Enable Register	16	0x34
20.	Error Interrupt Status Enable Register	16	0x36
21.	Normal Interrupt Signal Enable Register	16	0x38
22.	Error Interrupt Signal Enable Register	16	0x3A
23.	Capabilities Register	32	0x40
24.	ADMA Error Status Register	8	0x54
25.	ADMA System Address Register	32	0x58
26.	Host Controller Version	16	0xFE

Note: All register to be accesses at 32-bit boundary

7. Timing Waveforms

Below waveforms shows the timing diagram of processor interface signals

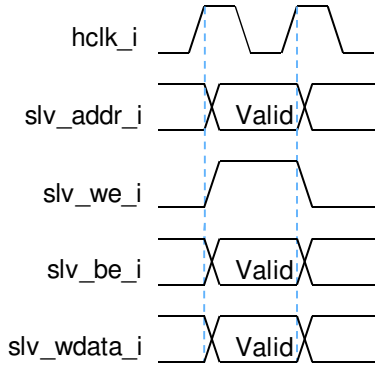

Figure 2: Register Write Cycle

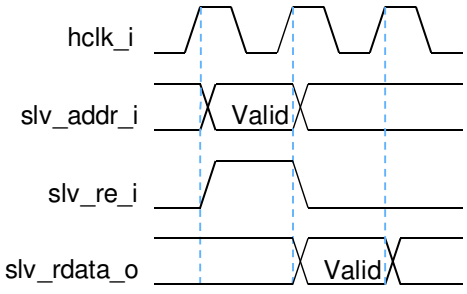

Figure 3: Register Read Cycle

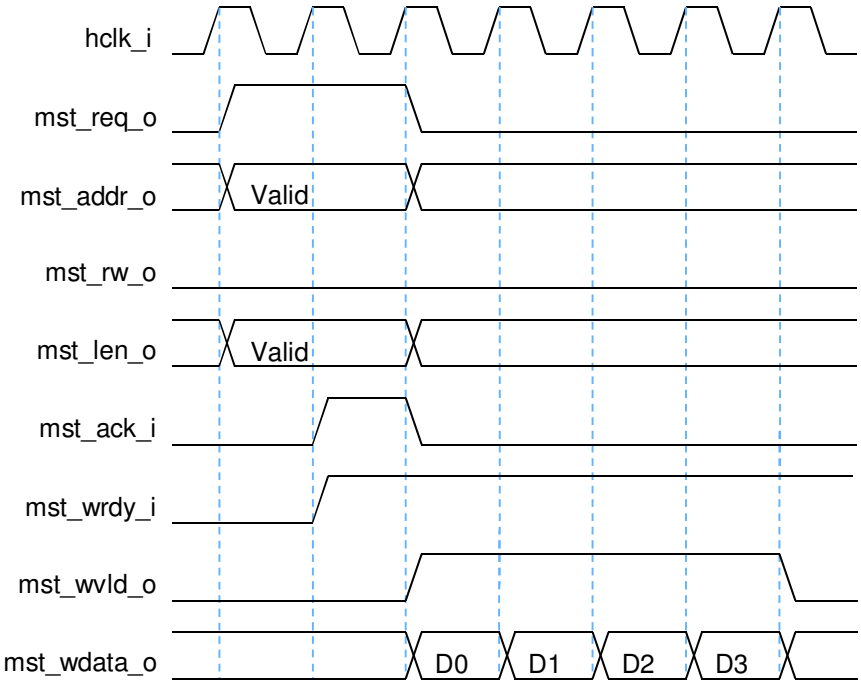

Figure 4: DMA Write Cycle (4 DWORD Burst)

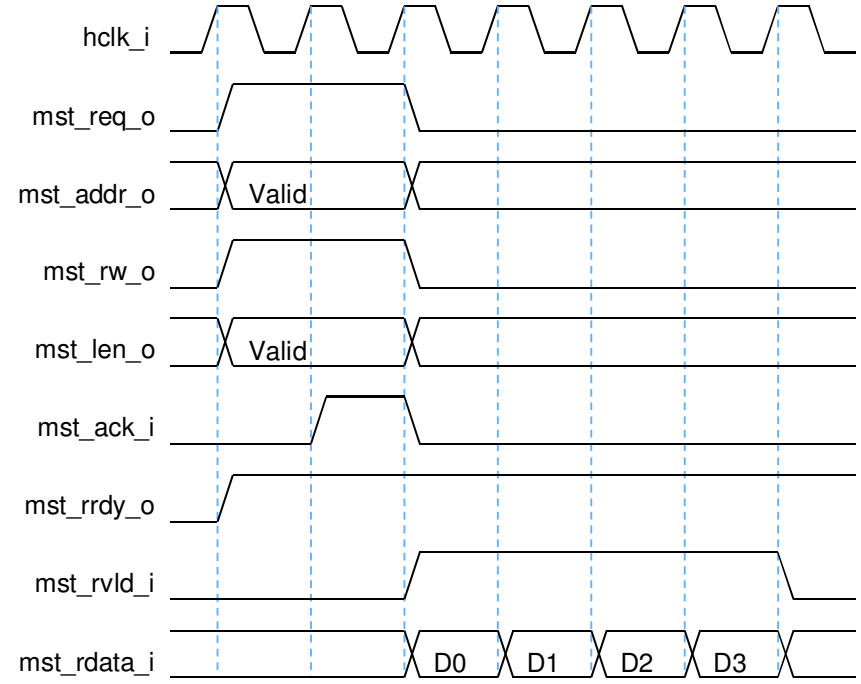

Figure 5: DMA Read Cycle (4 DWORD Burst)

8. Resource Utilization

The table below shows the utilization summary from the implementation of MMC Host Controller for different FPGA devices.

Device Utilization Summary for Actel ProASIC3

Logic Utilization	Used
Number of Core SEQ	1243
Number of Core COMB	2782
RAM/FIFO	8
Number of IOs	96

Table 5:Device Utilization Summary for Xilinx Spartan-6

Logic Utilization	Used
Number of Slice Registers	1,244
Number of Slice LUTs	1167
Number of IOs	96
Number of RAMB16BWERs	2

Table 6: Device Utilization Summary for Altera Cyclone IVE

Logic Utilization	Used
Combinational functions	1420
Dedicated logic registers	1243
Total block memory bits	32,768
Number of IOs	98

Table 7:Device Utilization Summary for LatticeXP2

Logic Utilization	Used
Number of Slice Registers	1492
Number of Slice LUTs	2602
Number of block RAMs	0
Number of PIO	96