Data Sheet For MMC Host Controller
DOCUMENT REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Change Description</th>
<th>Author</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1.0REL1.0</td>
<td>22&lt;sup&gt;nd&lt;/sup&gt; April’11</td>
<td>Initial Version</td>
<td>Preeti.N</td>
</tr>
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<td>Preeti.N</td>
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</table>

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1. General Description

This MMC host controller supports 1-bit, 4-bit, 8-bit memory card interface. This allows 1-bit, 4-bit SD/MMC transaction and 8-bit MMC transactions. The device conforms to the SD Host Standard Specification Version 2.0 and also supports MMC specification 4.3 version. This manages the physical layer of SD, MMC protocols and can be used together with SD Host Standard compatible driver software to add SD/MMC host functionality to a variety of microprocessor systems.

Processor interface is used here for connecting processor. Processor interface module consists Register block, through which the Host Driver software can configure the host controller and initiate transactions to and from an SD/MMC target. This consists 2 KB data buffer allows for a low interrupt latency time and efficient communication with the host processor at high data rates. The MMC Host controller also supports ADMA functionality to off-load the host processor for data transfer and increase overall system performance. An additional clock divider is used for generating required clock frequency for internal logic, which enables the user to achieve the maximum desired clock speed from the external clock source.

2. Features

The following are the main features of the MMC Host Controller:

- Compliant with SD Host Controller Standard Specification Version 2.0
- Compliant with SD Physical Layer Specification Version 2.0
- Compliant with MMC Specification Version 4.41
- Supports 1-bit, 4-bit SD/MMC modes and 8-bit MMC modes.
- Supports SD Card Detection input pin
- Supports SD Card Write Protection input pin
- Supports programmable clock frequency generation to the SD/MMC card.
- Supports Interrupt and ADMA2 transfer mode of operation.
- Individual 2Kbyte data buffer for read and write.
- Cyclic Redundancy Check (CRC) for command and data.
- Supports timeout monitoring for response, data, CRC token & busy.
- Supports a maximum block length of 2Kbyte.
- Supports both single block and multi block data transfer.
- Supports power ON/OFF control to SD/MMC card.
- Supports 32-bit synchronous memory interface towards host processor.
3. Block Diagram

![ MMC Host Controller Block Diagram ](image)

Figure 1: MMC Host Controller Block Diagram

4. IO Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rst_n_i</td>
<td>I</td>
<td>1</td>
<td>Asynchronous reset</td>
</tr>
<tr>
<td>hclk_i</td>
<td>I</td>
<td>1</td>
<td>Host Processor Interface clock</td>
</tr>
</tbody>
</table>
## Signal Dir Width Description

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mclk_i</td>
<td>I</td>
<td>1</td>
<td>MMC base clock</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This clock is used as base clock to MMC side logic</td>
</tr>
<tr>
<td>mclk180_i</td>
<td>I</td>
<td>1</td>
<td>MMC base clock inverted</td>
</tr>
</tbody>
</table>

### Table 2: Host Processor Interface IO Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>slv_addr_i</td>
<td>I</td>
<td>8</td>
<td>Address bus</td>
</tr>
<tr>
<td>slv_we_i</td>
<td>I</td>
<td>1</td>
<td>Write enable</td>
</tr>
<tr>
<td>slv_re_i</td>
<td>I</td>
<td>1</td>
<td>Read enable</td>
</tr>
<tr>
<td>slv_be_i</td>
<td>I</td>
<td>4</td>
<td>Byte enable</td>
</tr>
<tr>
<td>slv_wdata_i</td>
<td>I</td>
<td>32</td>
<td>Write data bus</td>
</tr>
<tr>
<td>slv_rdata_o</td>
<td>O</td>
<td>32</td>
<td>Read data bus</td>
</tr>
<tr>
<td>int_req_o</td>
<td>O</td>
<td>1</td>
<td>Interrupt request When HIGH indicates there is request for interrupt from the IP</td>
</tr>
</tbody>
</table>

### Host Processor Interface Master

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mst_req_o</td>
<td>O</td>
<td>1</td>
<td>Transfer Request When HIGH indicates ADMA wants to do data transfer</td>
</tr>
<tr>
<td>mst_addr_o</td>
<td>O</td>
<td>32</td>
<td>Transfer Address Indicates the system address from/to which data transfer need to be done.</td>
</tr>
<tr>
<td>mst_rw_o</td>
<td>O</td>
<td>1</td>
<td>Transfer direction 0 – write transfer 1 – read transfer</td>
</tr>
</tbody>
</table>
Table 3: MMC Interface IO Signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Dir</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
</table>
| mmc_cd_n_i | I   | 1     | Card Detect
|           |     |       | Connected to card detect switch of SD connector       |
| mmc_wp_n_i | I   | 1     | Write Protect
|           |     |       | Connected to write protect switch of SD connector     |
## 5. Functional Description

The main blocks in MMC Host Controller are:

- **Host Register Set**: This module implements the register set as per SD Host specification 2.0. It also implements debounce logic for card detect signal.
- **Command Path**: This module implements logic required to send command and receive response from SD/MMC card. It also instantiates 7-bit CRC generation circuit used for protection of command.
- **Data Path**: This module implements logic required to send and receive data from SD/MMC card. It also instantiates 16-bit CRC generation circuit to each data line used for protection of data.
- **Buffer**: This module implements 2Kbyte buffer to store read and write data.
o **ADMA:** This module implements scatter gather DMA logic used for data transfer between system memory and memory card.

o **Clock Divider:** This module generates and controls the different clock frequencies, required for MMC side logic.

o **MMC IO Register module:** This module implements necessary registers for MMC IO signals.

### 6. Standard Host Register Overview

The Register list of the MMC device is as shown in 4 below. These Registers can be accessed by the MMC Host.

**Table 4: MMC Host Controller Register Map**

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Registers</th>
<th>Width</th>
<th>Address Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Block Size Register</td>
<td>16</td>
<td>0x04</td>
</tr>
<tr>
<td>2.</td>
<td>Block Count Register</td>
<td>16</td>
<td>0x06</td>
</tr>
<tr>
<td>3.</td>
<td>Argument Register</td>
<td>32</td>
<td>0x08</td>
</tr>
<tr>
<td>4.</td>
<td>Transfer Mode Register</td>
<td>16</td>
<td>0x0C</td>
</tr>
<tr>
<td>5.</td>
<td>Command Register</td>
<td>16</td>
<td>0x0E</td>
</tr>
<tr>
<td>6.</td>
<td>Response0 Register</td>
<td>32</td>
<td>0x10</td>
</tr>
<tr>
<td>7.</td>
<td>Response2 Register</td>
<td>32</td>
<td>0x14</td>
</tr>
<tr>
<td>8.</td>
<td>Response4 Register</td>
<td>32</td>
<td>0x16</td>
</tr>
<tr>
<td>9.</td>
<td>Response6 Register</td>
<td>32</td>
<td>0x1C</td>
</tr>
<tr>
<td>10.</td>
<td>Buffer Data Port Register</td>
<td>32</td>
<td>0x20</td>
</tr>
<tr>
<td>11.</td>
<td>Present State Register</td>
<td>32</td>
<td>0x24</td>
</tr>
<tr>
<td>12.</td>
<td>Host Control Register</td>
<td>8</td>
<td>0x28</td>
</tr>
<tr>
<td>13.</td>
<td>Power Control Register</td>
<td>8</td>
<td>0x29</td>
</tr>
<tr>
<td>14.</td>
<td>Clock Control Register</td>
<td>16</td>
<td>0x2C</td>
</tr>
<tr>
<td>15.</td>
<td>Timeout Control Register</td>
<td>8</td>
<td>0x2E</td>
</tr>
<tr>
<td>16.</td>
<td>Software Reset Register</td>
<td>8</td>
<td>0x2F</td>
</tr>
<tr>
<td>17.</td>
<td>Normal Interrupt Status Register</td>
<td>16</td>
<td>0x30</td>
</tr>
<tr>
<td>18.</td>
<td>Error Interrupt Status Register</td>
<td>16</td>
<td>0x32</td>
</tr>
</tbody>
</table>
## 7. Timing Waveforms

Below waveforms shows the timing diagram of processor interface signals

![Waveform Diagram](image)

**Figure 2: Register Write Cycle**
Figure 3: Register Read Cycle

Figure 4: DMA Write Cycle (4 DWORD Burst)

Figure 5: DMA Read Cycle (4 DWORD Burst)
8. Resource Utilization

The table below shows the utilization summary from the implementation of MMC Host Controller for different FPGA devices.

Device Utilization Summary for Actel ProASIC3

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Core SEQ</td>
<td>1243</td>
</tr>
<tr>
<td>Number of Core COMB</td>
<td>2782</td>
</tr>
<tr>
<td>RAM/FIFO</td>
<td>8</td>
</tr>
<tr>
<td>Number of IOs</td>
<td>96</td>
</tr>
</tbody>
</table>

Table 5: Device Utilization Summary for Xilinx Spartan-6

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers</td>
<td>1,244</td>
</tr>
<tr>
<td>Number of Slice LUTs</td>
<td>1167</td>
</tr>
<tr>
<td>Number of IOs</td>
<td>96</td>
</tr>
<tr>
<td>Number of RAMB16BWES</td>
<td>2</td>
</tr>
</tbody>
</table>

Table 6: Device Utilization Summary for Altera Cyclone IVE

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combinational functions</td>
<td>1420</td>
</tr>
<tr>
<td>Dedicated logic registers</td>
<td>1243</td>
</tr>
<tr>
<td>Total block memory bits</td>
<td>32,768</td>
</tr>
<tr>
<td>Number of IOs</td>
<td>98</td>
</tr>
</tbody>
</table>

Table 7: Device Utilization Summary for LatticeXP2

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers</td>
<td>1492</td>
</tr>
<tr>
<td>Number of Slice LUTs</td>
<td>2602</td>
</tr>
<tr>
<td>Number of block RAMs</td>
<td>0</td>
</tr>
<tr>
<td>Number of PIO</td>
<td>96</td>
</tr>
</tbody>
</table>