Data Sheet For NAND Flash Host Controller

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
R1.0	27th Jan '11	Initial Version	Preeti.N
REL 1.0	16th Aug '12	Removed implementation results	VC

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1. General Description

This NAND Flash host controller supports 8-bit NAND Flash Interface. It has streaming interface towards user logic for data read and write .The data transfer between the host and NAND flash is carried out using command sequences like Read, Read for Copy Back, Reset, Page Program, Copy-Back Program, Block Erase, Random Data Input, Random Data Output and Read Status.

This consists of 2KB data buffer for storing data to be written to NAND Flash and 2KB data buffer for storing read data. NAND Flash Host Controller consists of ECC logic where Hamming code is to correct 1-bit error and detect 2-bit errors. It supports feature of Indentifying factory defined invalid blocks.

2. Features

The following are the main features of the NAND Flash Host Controller:

- 8-bit NAND Flash Interface
- SLC NAND Flash Memory
- Memory Capacity: 1 G-Bit
- Page Size: 2K-Byte
- Commands supported towards NAND Flash Memory: Read, Read for Copy Back, Reset, Page Program, Copy-Back Program, Block Erase, Random Data Input, Random Data Output and Read Status
- ECC Logic: Hamming code used to correct 1-bit error and detect 2-bit errors
- Simple streaming interface towards user logic for data read and write
- Commands supported from user: Block Erase, Read, Program and Copy-Back Program.
- 2K-byte buffer for write data
- 2K-byte buffer for read data
- Indentify factory defined invalid blocks

3. Block Diagram

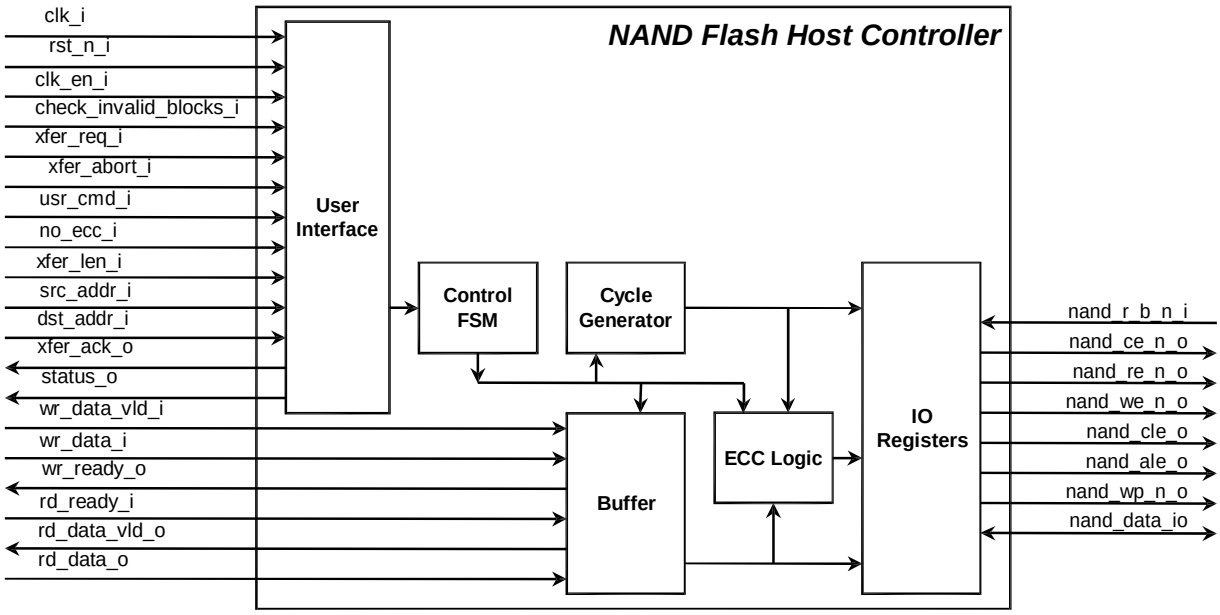

Figure 1: NAND Flash Host Controller Block Diagram

4. IO Signals

Table 1:System Interface IO Signals

Signal	Dir	Width	Description
clk_i	I	1	System Clock. Clock at which the NAND Flash Controller works.
rst_n_i	I	1	System Reset. Active low asynchronous reset.
clk_en_i	I	1	Clock Enable Used to support different timing mode towards NAND.

Table 2: User Interface IO Signals

Signal	Dir	Width	Description

Signal	Dir	Width	Description
check_invalid_blocks_i	I	1	Check Invalid Blocks User logic should assert this signal to enable NAND Flash Host Controller to check for invalid blocks.
xfer_req_i	I	1	Transfer Request User logic should assert this signal HIGH to request NAND Flash Controller for new operation.
xfer_abort_i	I	1	Transfer Abort User logic should assert this signal HIGH to abort existing write or read or copy-back operation to NAND Flash.
usr_cmd_i	I	2	User command 00b – Block Erase 01b – Write 10b – Read 11b – Copy-Back
no_ecc_i	I	1	No ECC User logic should assert this signal HIGH to indicate that for the requested command no ECC generation/checking is required.
xfer_len_i	I	6	Transfer Length User logic indicates the no. of pages to be written or read for current requested transfer using this signal. 00h – 1 Page 01h – 2 Pages . . 3Fh – 64 Pages
src_addr_i	I	16	Source Address User logic indicates the start address for current requested transfer using this signal. This signal is also used as source address in case of Copy-Back command.

Signal	Dir	Width	Description
dst_addr_i	I	16	Destination Address User logic indicates the start address for current requested transfer using this signal. This signal is also used as destination address in case of Copy-Back command. For other commands this signal is not used.
xfer_ack_o	O	1	Transfer Acknowledge Controller asserts this signal indicating it has accepted the current transfer request from user logic.
rd_ready_i	I	1	Ready from user interface User interface should assert this signal HIGH to indicate that it can accept new read data from controller
rd_data_o	O	1	Read Data
rd_data_vld_o	O	1	Read Data Valid Controller asserts this signal HIGH when data is valid on rd_data_o
wr_data_vld_i	I	1	Write Data Valid User logic should assert this signal HIGH to indicate data is valid on wr_data_i
wr_data_i	I	8	Write Data
wr_ready_o	O	1	Ready from controller Controller asserts this signal HIGH when it is ready to accept new data

Signal	Dir	Width	Description
status_o	O	24	Status Indicates the status of current transfer status_o[15:0] – Row address status_o[16] - when HIGH indicates start of identify invalid blocks status_o[17] - when HIGH indicates end of identify invalid blocks status_o[18] - when HIGH indicates invalid block status_o[19] - when HIGH indicates transfer success status_o[20] - when HIGH indicates transfer failure status_o[21] - when HIGH indicates erase failure status_o[22] - when HIGH indicates program failure status_o[23] - when HIGH indicates ECC failure

Table 3: NAND Flash Interface IO Signals

Signal	Dir	Width	Description
nand_r_b_n_i	I	1	Ready/Busy signal of NAND Flash Memory
nand_ce_n_o	O	1	Chip Enable signal of NAND Flash Memory
nand_re_n_o	O	1	Read Enable signal of NAND Flash Memory.
nand_we_n_o	O	1	Write Enable signal of NAND Flash Memory
nand_cle_o	O	1	Command Latch Enable signal of NAND Flash Memory
nand_ale_o	O	1	Address Latch Enable signal of NAND Flash Memory
nand_wp_n_o	O	1	Write Protect signal of NAND Flash memory

Signal	Dir	Width	Description
nand_data_io	O	8	Data Input/Output signal of NAND Flash Memory

5. Functional Description

The main blocks in NAND Flash Host Controller are:

- **User Interface**: This module implements logic required to interface controller to user logic.It provide different command to control FSM to generate different cycles.
- **Control FSM:** This module implements logic to control NAND flash read/write. It accept the commands from the user interface and generates different cycle request to cycle generator.
- **Cycle Generator**: This module implements the logic required for generation of different cycles towards the NAND. It generates command latch, address latch, read and write cycles as per the request from the control FSM.
- **Buffer**: This module implements 2K-byte read buffer and 2K-byte write buffer.
- **ECC Logic**: This module implements logic required to generate ECC and detect 1-bit error and correct it. In addition to that it also check for ECC during read cycle and corrects any 1-bit error in every 512-bytes of data. The ECC parity bits are generated from 512-bytes of data.
- **IO Registers**: This module implements the necessary IO register for NAND signals.

6. Timing Waveforms

Below waveforms shows the timing diagram of processor interface signals

6.1 NAND Flash Interface

6.1.1 Command Latch Cycle

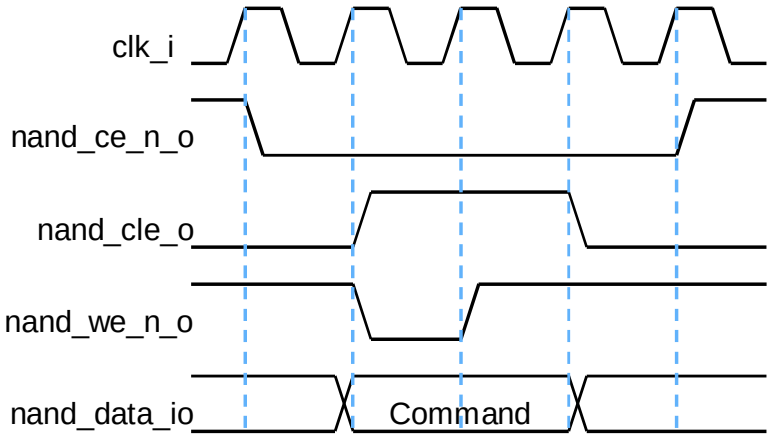

Figure 2: Command Latch Cycle

6.1.2 Address Latch Cycle

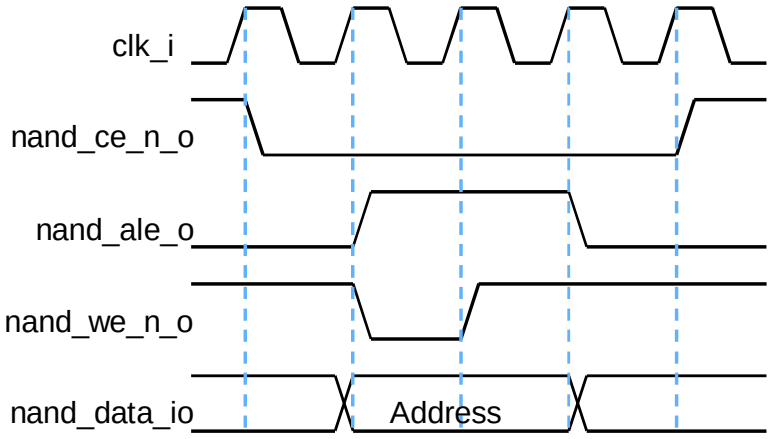

Figure 3: Address Latch Cycle

6.1.3 Data-In Cycle

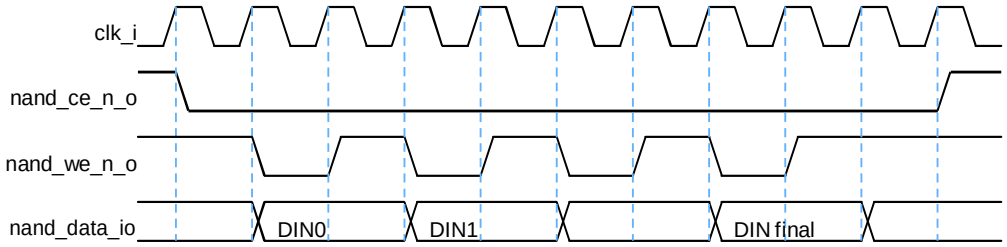

Figure 4: Data-In Cycle

6.1.4 Data-Out Cycle

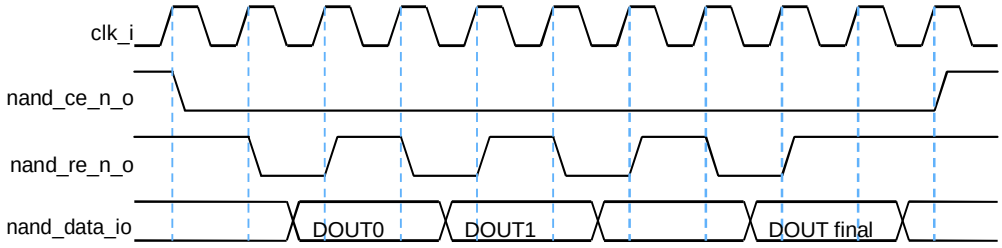

Figure 5: Data-Out Cycle

6.2 User Interface

6.2.1 Control Path

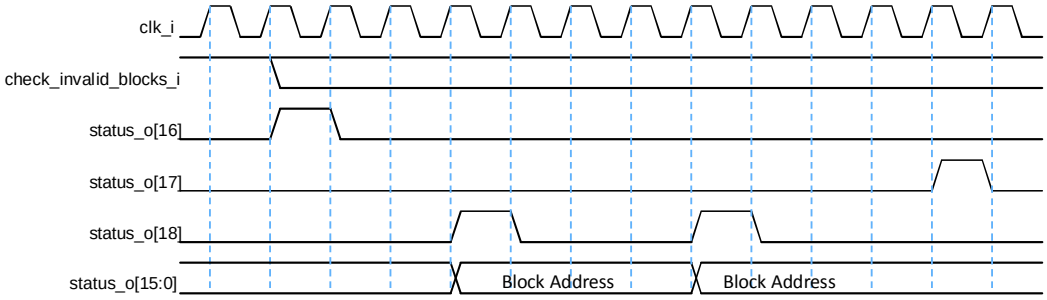

Figure 6: Invalid Block Detection Status Timing Diagram

6.2.2 Data Path

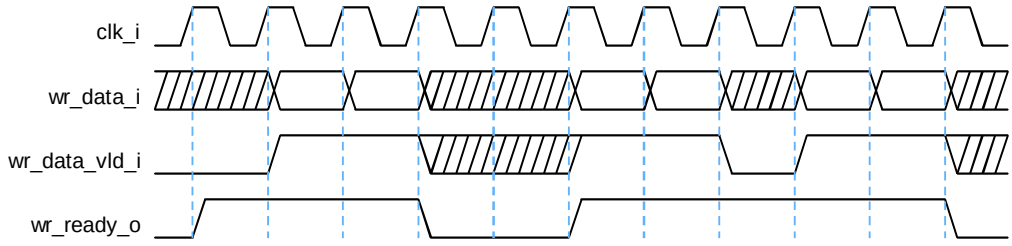

Figure 7: Write Data Path Timing Diagram

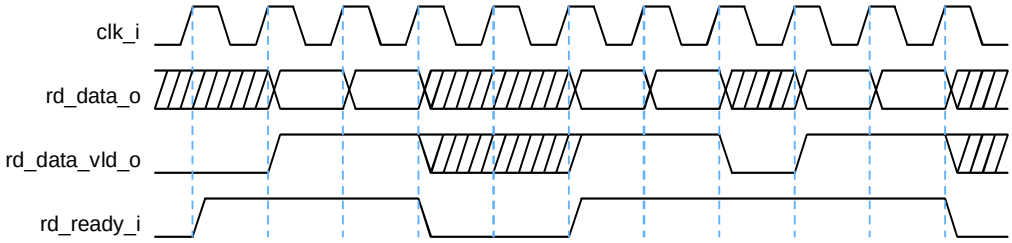

Figure 8: Read Data Path Timing Diagram