Data Sheet For 8237 DMA Control Unit

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	24th Dec '11	Initial Version	SR
REL 1.0	16th Aug '12	Removed implementation results	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification 8237 DMA control unit. It includes the overall features, detailed description, I/O specifications and resource utilization summary for the 8237 DMA control unit.

1.2 Features

The DMAU supports a four-channel DMA controller with the following features

- 24-bit length address register
- 16-bit length count register
- 4 independent DMA channels
- 4 clock / 1 bus cycle
- Byte transfer / word transfer selectable
- Three transfer modes
  - Single transfer mode
  - Demand transfer mode
  - Block transfer mode
- Two bus modes
  - Bus release mode
  - Bus hold mode
- DMA request maskable on an individual channel basis
- Software DMA request in uPD71037 mode
- Auto initialization function
- Transfer address incrementing/decrementing
- Two kinds of channel priority order
  - Fixed priority
  - Rotating priority
- TC_N output at the end of transfer
- Forced service termination by END_N input
- Cascading capability
- I/O – memory and memory – I/O transfer capability

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
DMA	Direct Memory Access
DMAU	DMA Control Unit
FPGA	Field Programmable Gate Array
IO	Input/Output
TC	Transfer Count
TBD	To be done

2 8237 DMA Control Unit (DMAU)

2.1 Block Diagram

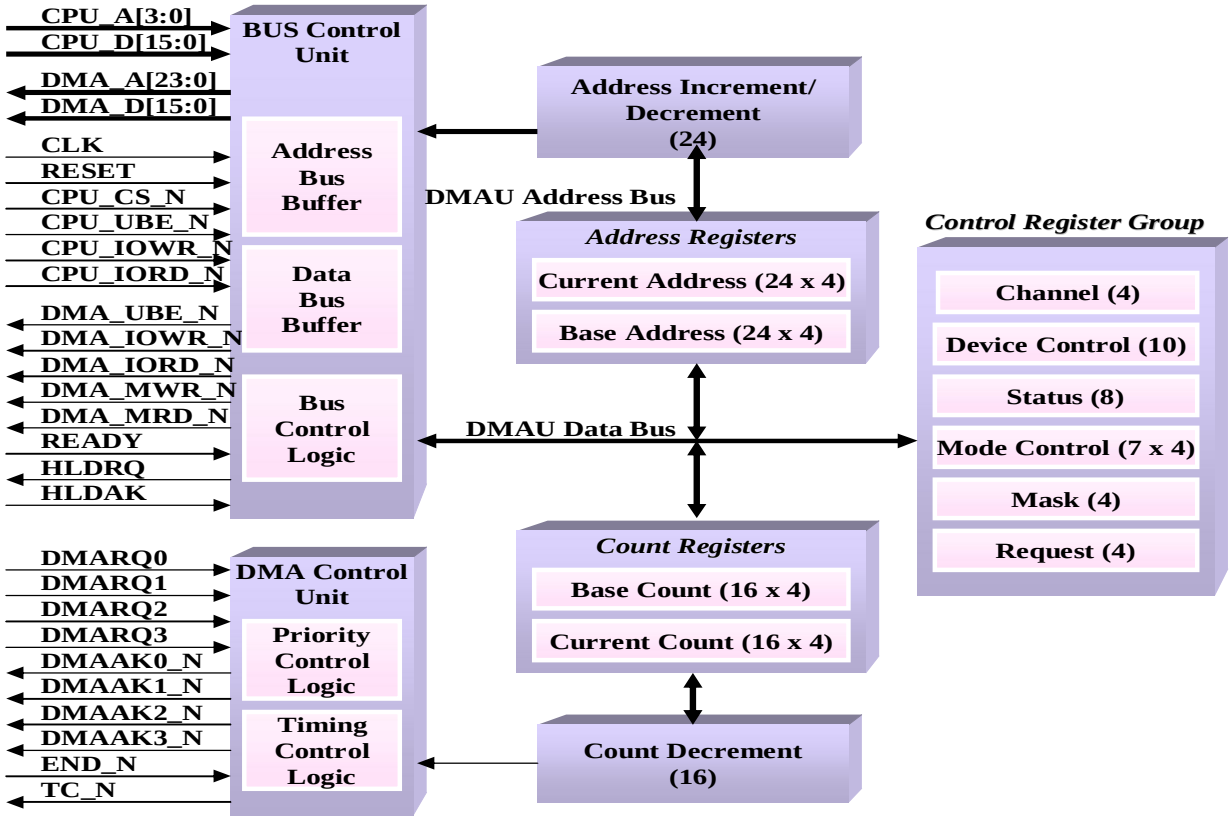


Figure 1: 8237 DMA Controller Block Diagram

2.2 Description

The DMAU has following functional units:

- **Bus Control Unit:** The bus control unit consist of address and data buffers and bus control logic. The bus control logic generates and receives signals that control addresses and data on the internal address and data buses.

- **DMA Control Unit:** The DMA control unit contains the priority and timing control logic. The priority control logic determines the priority level of DMA requests and arbitrates the use of the bus in accordance with this priority level. The DMA control unit also provides internal timing and controls DMA operations.

- **Address Registers:** Each of the four DMA channels has one 24-bit base address register and one 24-bit current address register. The base address register holds a value determined by the CPU and transfers this value to the current address register during auto initialization (address and count are automatically initialized). The channel's current address register is incremented/decremented for each transfer and always contains the address of the data to be transferred next.

- **Address Incrementer/Decrementer:** The address incrementer/decrementer updates the contents of the current address register whenever a DMA transfer completes.

- **Count Registers:** Each of the four DMA channels has one 16-bit base count register and one 16-bit current count register. The base count register holds a value written by the CPU and transfers the value to the current count register during auto initialization. A channel's current count register is decremented for each transfer and generates a terminal count when the count register is decremented to FFFFH.

- **Count Decrementer:** The count decrementer decrements the contents of the current count register by one when each DMA transfer cycle ends.

- **Control Registers:** The DMAU contains following control registers.
  - Channel
  - Device
  - Status
  - Mode
  - Request
  - Mask

  These registers control DMAU operating functions.

2.3 I/O Signal Description

Table 2: CPU Interface Signals

SIGNAL	I/O	WIDTH	DESCRIPTION
CLK_I	I	1	Clock controls the internal operation and data transfer speed of this block.
RESET_I	I	1	Active high reset initializes the DMAU internal register and leaves the DMAU in idle cycle.
CPU_A_I[15:0]	I	16	In idle cycle A3-A0 becomes address inputs to select internal registers for the CPU to read or write. To access bank registers in uPD71037 mode
CPU_D_I[15:0]	I	16	Data bus from CPU.
CPU_UBE_N_I	I	1	UBE_N indicates the upper byte of data bus is valid during 16-bit mode.
CPU_IORD_N_I	I	1	In idle cycle, IORD_N inputs a read signal from CPU.
CPU_IOWR_N_I	I	1	In idle cycle, IOWR_N inputs a write signal from CPU.
CPU_CS_N_I	I	1	During idle cycle, CS_N selects the DMAU as an I/O device.
READY_I	I	1	During DMA operation READY indicates that a data transfer for one cycle has been completed and may be terminated. To meet the requirements of low speed I/O devices or memory READY may be negated to insert wait states to extend the bus cycle until READY is again asserted.
HLDAK_I	I	1	When asserted, HLDAK indicates that CPU has granted the DMAU the use of system bus.
HLDRQ_O	O	1	DMAU request the CPU for system bus by asserting HLDRQ.
CPU_BUSCY_O	O	1	Indicates start of the DMA cycle

CPU_BUSST_O[2:0]	O	1	Gives bus status DMA write transfer: 101 DMA read transfer: 101 Write and read transfer differentiated by R/Wn signal
CPU_A_O[23:0]	O	24	These address line outputs memory address during DMA cycle.
CPU_D_O[15:0]	O	16	DMA data bus.
SCTL_REG_I[3:0]	I	4	System control register
OPHA_ REG_I[7:0]	I	8	Sets the higher order of the IO address for the DMAU in uPD71037 mode
BANK_SEL_REG_I[7:0]	I	8	Bank selection register decides settable bits of the lower byte of the IO address
BANK_ADDR_REG_I[7:0]	I	8	Bank address register sets the lower order of the IO address for the DMAU in uPD71037 mode

2.3.1 DMA Interface

Table 3: DMA Interface

SIGNAL	I/O	WIDTH	DESCRIPTION
DMARQ0_O	O	1	DMARQ0 accept DMA service requests from peripheral devices. DMARQ0 must be asserted till DMAAK0_N is asserted.
DMARQ1_O	O	1	DMARQ1 accept DMA service request from peripheral device. DMARQ1 must be asserted till DMAAK1_N is asserted.
DMARQ2_O	O	1	DMARQ2 accept DMA service request from peripheral device. DMARQ3 must be asserted till DMAAK2_N is asserted.
DMARQ3_O	O	1	DMARQ3 accept DMA service request from peripheral device. DMARQ3 must be asserted till DMAAK3_N is asserted.
DMAAK0_N_I	I	1	DMACK0_N indicates to the peripheral device that DMA service has been granted.
DMAAK1_N_I	I	1	DMACK1_N indicates to the peripheral device that DMA service has been granted.

DMAAK2_N_I	I	1	DMACK2_N indicates to the peripheral device that DMA service has been granted.
DMAAK3_N_I	I	1	DMACK3_N indicates to the peripheral device that DMA service has been granted.
END_N_I/ TC_N_O	I/O	1	END_N input is used to terminate the current DMA transfer. TC_N indicates the designated cycles of the DMA count transfer have finished
DMA_UBE_N_O	O	1	UBE_N indicates the upper byte of data bus is valid during 16-bit mode.
DMA_IORD_N_O	O	1	In DMA cycle, IORD_N outputs a read signal to an I/O device.
DMA_IOWR_N_O	O	1	In DMA cycle, IOWR_N outputs a write signal to an I/O device.
DMA_MRD_N_O	O	1	During DMA cycle, MRD_N outputs a read signal to memory.
DMA_MWR_N_O	O	1	During DMA cycle, MWR_N outputs a write signal to memory.

3 Timing Waveforms

3.1 DMAU Waveforms

3.1.1 Bus arbitration

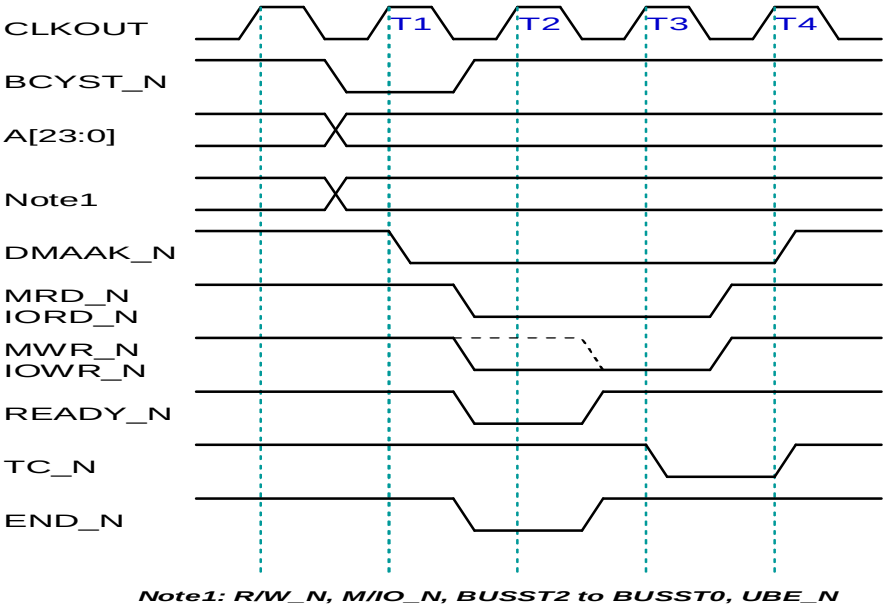
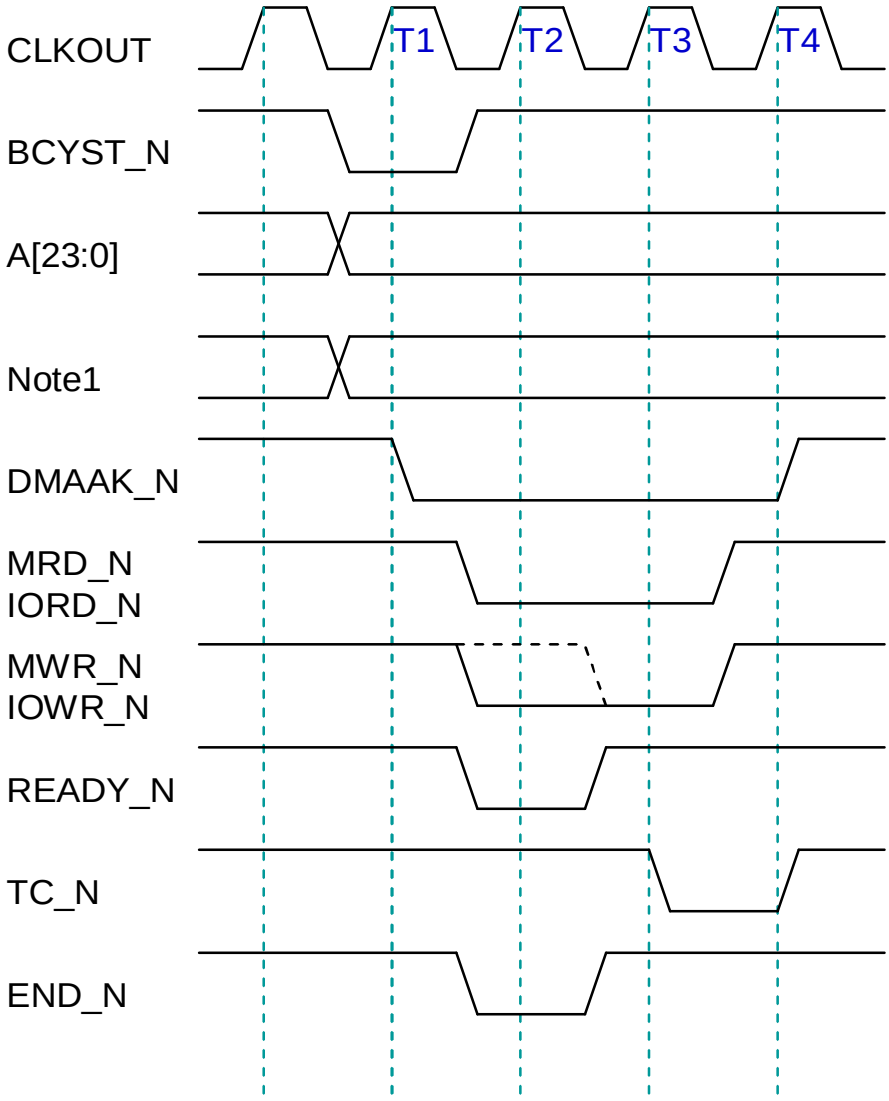


Figure 2: Bus arbitration cycles

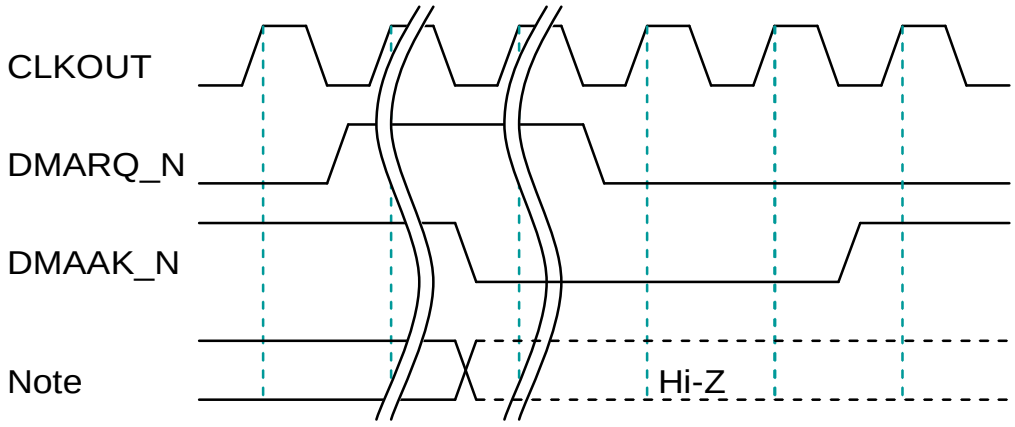
3.1.2 DMA cycle



Note1: R/W_N, M/IO_N, BUSST2 to BUSST0, UBE_N

Figure 3: DMA Controller in Normal Mode

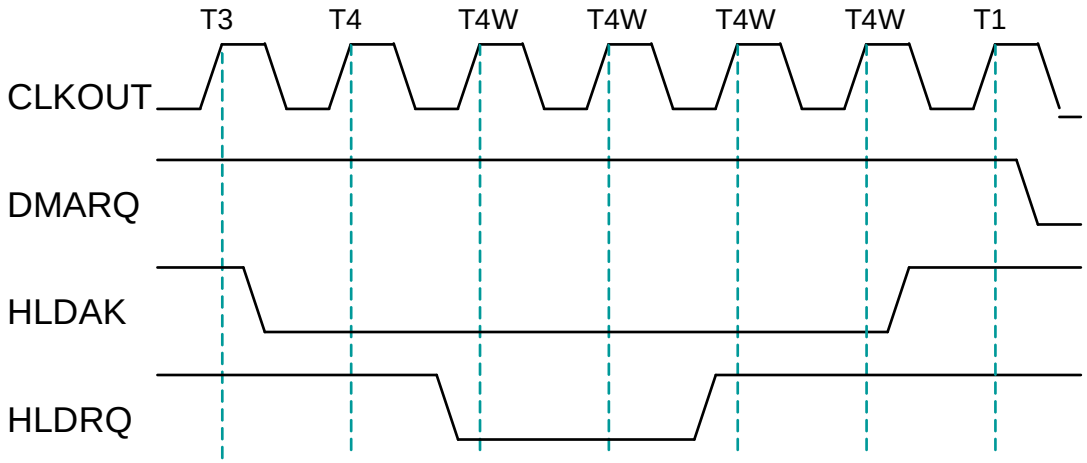
3.1.3 Cascading Mode



Note: A[23:0], UBE_N, MRD_N, MWR_N, IORD_N, IOWR_N, BUFEN_N, BCYST_N, DSTB_N

Figure 4: DMA Controller in Cascading Mode

3.1.4 Bus Wait Timing



Note: A[23:0], UBE_N, MRD_N, MWR_N, IORD_N, IOWR_N

Figure 5: Bus wait operation