iWave
Embedding Intelligence

iW-80188XL Core

Overview

iW- 80188XL is a powerful 16 - bit microprocessor core, executes instruction list compatible with 80188XL microprocessor. The design along with multiple peripherals can be fit into single FPGA.

Features

- iW-80188XL Core
  - Multiplexed 20 - bit address and 8 - bit data bus
  - 1MB memory space divided into 4 segments
  - 64KB IO space
  - Non Maskable Interrupt support
  - Arithmetic - Logic Unit
    - # 8, 16 & 32 - bit operations
    - # 8 & 16 - bit logical operations
    - # Boolean manipulations
    - # 16 x 16 bit multiplication (signed or unsigned)
    - # 32 / 16 - bit division (signed or unsigned)
- CPU on - chip peripherals
  - Programmable Timer / Counter Unit
    - # 3 programmable independent 16 - timers
    - # TOUT0 to TOUT1 pin outputs
    - # TIN0 & TIN1 used either as clock or control signals
    - # Timer - 2 can be used to clock other 2 timers
    - # Internal / external input clock selectable
  - Direct Memory Access Unit
    - # Two independent high-speed DMA channels
    - # Data can be transferred between any combination of memory & IO space
    - # DMA transfer can be initiated by external, internal request or by direct programming
    - # 20-bit length address register
    - # 16-bit length transfer count register
    - # Transfer address can be incrementing, decrementing or remained constant
    - # Two kinds of channel priority order : Fixed priority & Rotating priority
    - # DMAU can be programmed to produce interrupt request when its transfer count reaches zero
    - # Both byte & word transfer is possible in case of 80186XL;word transfer is illegal in case of 80188XL processor
  - Interrupt Controller Unit
    - # Four external interrupt request inputs (INT0 to INT3)
    - # Timer 0, Timer1, Timer 2 and DMA 0, DMA1 Interrupts (Internal Interrupts)
    - # Edge or level triggered interrupt request inputs
    - # Individually Mask-able interrupts request
    - # Programmable interrupt request priority orders
    - # Polling operation capability
    - # Cascade with external 8259A interrupts (only on INT0 and INT1) operates in either Master mode or Slave mode
    - # Special fully nested mode support
  - Chip Select Unit
    - # Thirteen programmable chip-select outputs
    - # Six of the chip-selects map only into memory address space, while the remaining seven can map into either memory or I/O address space
    - # Programmable block size and start / end address
    - # Memory or I/O bus cycle decoder
    - # Programmable wait-state generator
    - # Provision to disable a chip select
    - # Provision to override bus ready
  - Clock Generator

Core Benifits

- Compatible with Intel 80188XL instruction set
- High FPGA integration enables lower BOM cost and smaller board design
- Supports retarget and merge external peripherals and traditional custom old ASICs
- Enhancements of system performance with increased operating frequency and integration

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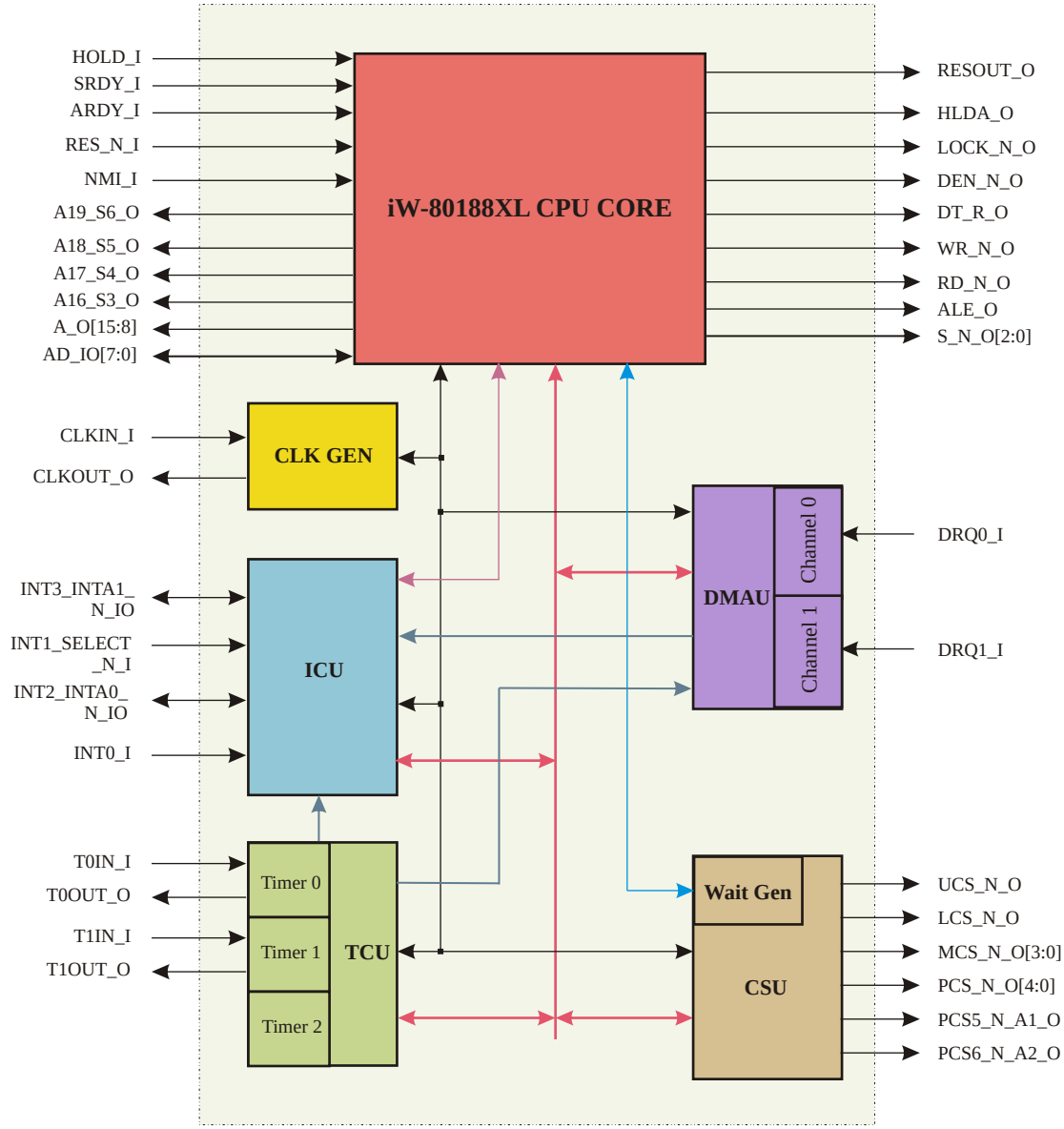
Block Diagram



Core Applications

- Quick migration of 80188XL based designs to an FPGA platform
- Replacement for 80188XL processor and ASICs
- Typical processor applications such as industrial, automotive and etc.

Deliverables

- Technical Specification
- RTL Verilog Synthesizable Code
- Comprehensive Test Environment
- Technical Support and Maintenance

About Us

***i*Wave** Systems Technologies is an embedded Hardware and Software Turnkey Design Services company, focused on providing integrated solutions for developing innovative products and systems in the areas of Communication, Consumer electronics and Multimedia. iWave offers complete turnkey solutions for systems engineering and product development.

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