Data Sheet For 80186EC Core

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1 Introduction

1.1 Purpose

The iW-80186EC is a powerful 16-bit microprocessor core, executes instruction list compatible with 80186EC microprocessor. The design along with multiple peripherals can be fit into single FPGA.

1.2 Features

The following are the main features of the 80186EC Core:

- iW-80186EC CPU Core
  - Multiplexed 20-bit address and 16-bit data bus
  - 1M-byte memory space divided into 4 segments
  - 64K-byte IO space
  - Non Maskable Interrupt support
  - Arithmetic-Logic Unit
    - 8,16,32-bit arithmetic operations
    - 8,16-bit logical operations
    - Boolean manipulations
    - 16 x 16 bit multiplication (signed or unsigned)
    - 32/16-bit division (signed or unsigned)
- CPU On-Chip Peripherals
  - Programmable Timer / Counter Unit
    - Three programmable independent 16-bit timers
    - TOUT0 to TOUT1 pin outputs
    - TIN0 & TIN1 used either as clock or control signals
    - Timer-2 can be used to clock other two timers
    - Internal / external input clock selectable
  - Serial Communications Unit
    - RS-232-C protocol support (on-chip CTS_N, SINT_N pins)
    - Only asynchronous mode is supported
    - Two independent identical channels
    - Full duplex operation in asynchronous mode
    - Programmable seven, eight or nine data bits in asynchronous mode

- Independent baud rate generator
- Double-buffered transmit and receive
- Clear-to-Send feature for transmission
- Break character transmission and detection
- Programmable even, odd or no parity
- Detects both framing and overrun errors
- Supports interrupt on transmit and receive

- Interrupt Controller Unit
  - Edge trigger / level trigger selectable
  - Individually maskable interrupt requests
  - Programmable interrupt request priority orders
  - Supports Cascading and polling mode
  - 8 external interrupt request inputs (INTx ; x=0,1,2,..,7)
  - 7 internal interrupt input pins (SCU, TCU, and DMAU)
- Chip Select Unit
  - Ten programmable chip-select outputs
  - Programmable start and stop addresses
  - Memory or I/O bus cycle decoder
  - Programmable wait-state generator
  - Provision to disable a chip-select
  - Provision to override bus ready
- Direct Memory Access Unit
  - four DMA channels can be accessed independently
  - priority of channels can be modified using priority registers.
  - DMA requests can be masked by DMA HALT registers.
  - four separate External DMA requests pins.
  - internal requests either by timer.
  - programmable software request to start the DMA.
  - The four channel DMAs are integrated using two channel module.
- Watchdog Timer Unit
  - 32-bit down counter used,
  - reload and disable option for the watchdog timer.

- Asserts a signal to indicate if the program hangs, or some infinite loop occurs.

- Multiplexed general purpose Input Output port
  - Three ports of total having 22 pins
  - A 8 pin inout port multiplexed with the Serial controller unit
  - A 8 pin output port multiplexed with Chip Select Unit.
  - A 6 pin output port multiplexed with DMA and SCU interrupts(4 pins) and two pins as general purpose inouts.
- Clock Generator

1.3 Features Not Supported

- Crystals cannot be directly connected to the FPGA (External clock input required for FPGA)
- ONCE mode
- Power down modes
- Refresh Control Unit
- WAIT instruction is not supported
- Synchronous mode in Serial Communication Unit

1.4 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Array
CPU	Central Processing Unit
I/O	Input/ Output
DMAU	Direct Memory Access Unit
BIU	Bus Interface Unit
CSU	Chip Select Unit
TCU	Timer Control Unit
ICU	Interrupt Control Unit
SCU	Serial Control Unit
IOPU	Input Output Port Unit

2 80186EC Core

2.1 Block Diagram

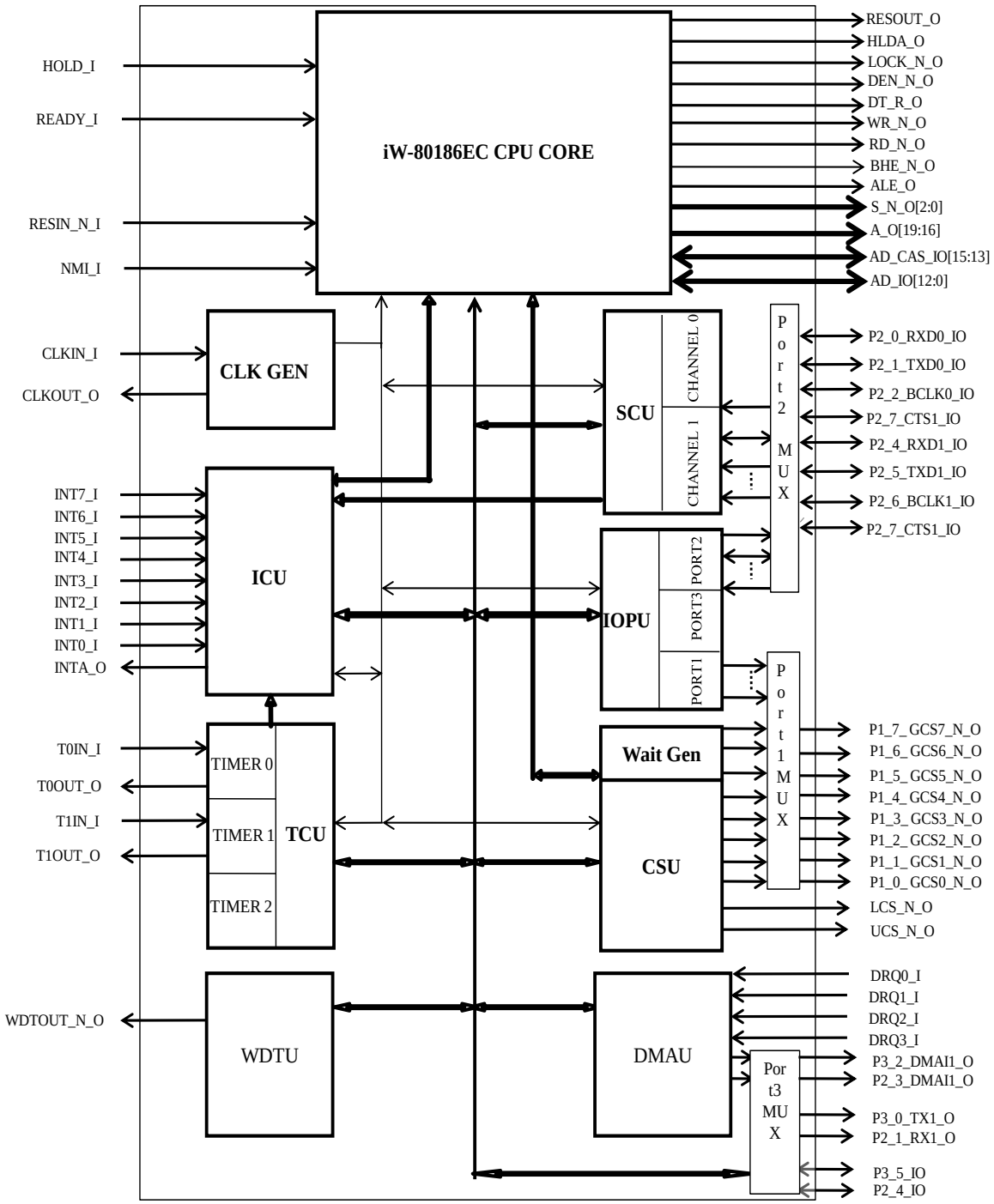

Figure 1: 80186EC Core Block Diagram

2.2 Description

The main blocks in 80186EC Core:

- **Central Processing Unit (CPU)**: This module executes instructions, which include fetching, decoding instructions and generating appropriate requests to the Bus Interface Unit.
- **Timer / Counter Unit (TCU):** This module provides three programmable 16-bit timer/counters. Two of these are highly flexible and are connected to external pins for control or clocking. A third timer is not connected to any external pins and can only be clocked internally.
- **Serial Communications Unit (SCU):** This module supports both synchronous and asynchronous communications modes and contains two independent channels. Each channel has its own baud rate generator that is independent of the TCU, and can be internally or externally clocked at up to one half of the operating frequency.
- **Interrupt Control Unit (ICU):** This module serves 8 external interrupts and 7 internal interrupts , using master and slave 8259 programmable interrupt controller. The master 8259A module offers the ability to cascade to up to seven other 8259A modules. This arrangement is used to expand the interrupt handling capability of an 80C186EC system to 57 external sources.
- **Chip-Select Unit (CSU):** This module integrates logic, which provides up to ten programmable chip selects to access both memories and peripherals. Besides selecting a specific device, each chip-select can be used to control the number of wait states inserted into the bus cycle
- **I/O Port Unit (IOPU):** This module supports two 8-bit channels of input, output, or input/output operation
- **DMAU:** This module supports Direct memory access with 4 channels, with MEM/IO to IO/MEM transfers or vice versa.
- **WDTU:** Watchdog unit continuously monitor the system operation for any hang-outs or indefinite loops in execution.
- **Clock Generator:** This module generates both internal and external clock

2.3 I/O Signal Description

Table 2: 80186EC Core IO Signals—not finished

Signal	I/O	Width	Description
RESIN_N_I	I	1	An active low signal causes the processor to immediately terminate any bus cycle in progress and assume an initialized state. All pins will be driven to a known state, and RESOUT will also be driven active.
RESOUT_O	O	1	Indicates the processor is currently in the reset state. RESOUT will remain active as long as RESIN_N remains active.
CLKIN_I	I	1	External clock input operating at two times the processor operating frequency.
CLKOUT_O	O	1	Processor Clock output. It is half of Clock input (CLKIN_I).
A19/S6, A18/S5 A17/S4 A16/S3	I/O	1	These pins drive address information during the address phase of the bus cycle. During T2 and T3 these pins drive status information. S6 is low to indicate CPU bus cycles and high to indicate DMA or refresh bus cycles. S3 to S6 are always 0 on the 80C186EC.
AD15/CAS2 AD14/CAS1 AD13/CAS0	I/O	1	These pins are part of the multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 15 through 13 are presented on these pins and can be latched using ALE. Data information is transferred during the data phase of the bus cycle. Pins AD15:13/CAS2:0 drive the 82C59 slave address information during interrupt acknowledge cycles.
AD_IO	I/O	13	These pins provide a multiplexed ADDRESS and DATA bus. During the address phase of the bus cycle, address bits 0 through 12 are presented on the bus and can be latched using ALE. Data information is transferred during the data phase of the bus cycle.

<table>
<tr><th>Signal</th><th>I/O</th><th>Width</th><th>Description</th></tr>
<tr><td>BHE_N_O</td><td>O</td><td>1</td><td>Byte High Enable output indicates that the bus cycle in progress is transferring data over the upper half of the data bus. BHE and A0 have the following logical encoding scheme

<table><tr><th>A0</th><th>BHE_N_O</th><th>Encoding</th></tr><tr><td>0</td><td>0</td><td>Word Transfer</td></tr><tr><td>0</td><td>1</td><td>Even byte transfer</td></tr><tr><td>1</td><td>0</td><td>Odd byte transfer</td></tr><tr><td>1</td><td>1</td><td>NA</td></tr></table></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td>ALE_O</td><td>O</td><td>1</td><td>Address Latch Enable, an active high signal used to strobe address information into a transparent type latch during the address phase of the bus cycle.</td></tr>
<tr><td>S_N_O[2:0]</td><td>O</td><td>3</td><td>Bus cycle Status are encoded on these pins to provide bus transaction information. S[2:0] are
<table><tr><th>S2</th><th>S1</th><th>S0</th><th>BUS CYCLE</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Interrupt Acknowledge</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Read I/O</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Write I/O</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Processor HALT</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Queue Instruction Fetch</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Read Memory</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Write Memory</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Passive(no bus activity)</td></tr></table></td></tr>
</table>

Signal	I/O	Width	Description
READY_I	I	1	Active high Ready input to signal the completion of a bus cycle. It must be active to terminate any bus cycle, unless it is ignored by correctly programming the Chip-Select Unit.
RD_N_O	O	1	Active low Read output signals that the accessed memory or I/O device must drive data information onto the data bus.
WR_N_O	O	1	Active low Write output signals that data available on the data bus are to be written into the accessed memory or I/O device.
DEN_N_O	O	1	Active low Data enable output to control the enable of bi-directional transceivers in a buffered system. DEN is active only when data is to be transferred on the bus.
DT_R_O	O	O	Data Transmit/Receive output controls the direction of a bi-directional buffer in a buffered system.
HOLD_I	I	1	HOLD request input to signal that an external bus master wishes to gain control of the local bus.
HLDA_O	O	1	The processor generates HLDA in response to a HOLD indicating that bus is granted. It indicates that the processor has relinquished control of the local bus.
LOCK_N_O	O	1	The processor will not service other bus requests (such as HOLD) while LOCK is active.
NMI_I	I	1	Non-Maskable Interrupt input causes a TYPE-2 interrupt to be serviced by the CPU. NMI is latched internally.
UCS_N_O	O	1	Upper Chip Select will go active whenever the address of a memory or I/O bus cycle is within the address limitations programmed by the user.
LCS_N_O	O	1	Lower Chip Select will go active whenever the address of a memory bus cycle is within the address limitations programmed by the user.

Signal	I/O	Width	Description
P1_0_GCS0_N_O to P1_7_GCS7_N_O	O	1	These pins provide a multiplexed function. If enabled, each pin can provide a Generic Chip Select output, which will go active whenever, the address of a memory or I/O bus cycle is within the address limitations programmed by the user. When not programmed as a Chip-Select, each pin may be used as a general-purpose output Port. As an output port pin, the value of the pin can be read internally.
T0OUT0_O, T1OUT1_O	O	1	Timer output pins can be programmed to provide a single clock or continuous waveform generation, depending on the timer mode selected.
T0IN0_I,T1IN1_I	I	1	Timer input is used either as clock or control signals, depending on the timer mode selected.
INT0_I, INT1_I, INT2_I, INT3_I, INT4_I, INT5_I, INT6_I, INT7_I	I	1	Maskable interrupt input will cause a vector to a specific type interrupt routine. The INT6:0 pins can be used as cascade inputs from slave 8259A devices. The INT pins can be configured as level or edge sensitive
INTA_O	O	1	Interrupt Acknowledge output is a handshaking signal used by external 82C59A Programmable Interrupt Controllers.
P3_5_IO, P3_4_IO	I/O	1	Bidirectional, open-drain port pins.
P3_3_DMAI1_O, P3_2_DMAI0_O	O	1	DMA Interrupt output goes active to indicate that the channel has completed a transfer. DMAI1 and DMAI0 are multiplexed with output only port functions.
P3_1_TXI1_O	O	1	Transmit Interrupt output goes active to indicate that serial channel 1 has completed a transfer. TXI1 is multiplexed with an output only Port function.
P3_0_RXI1_O	O	1	Receive Interrupt output goes active to indicate that serial channel 1 has completed a reception. RXI1 is multiplexed with an output only port function.

Signal	I/O	Width	Description
WDTOUT_N_O	O	1	WatchDog Timer output is driven low for four clock cycles when the watchdog timer reaches zero. WDTOUT may be ANDed with the power-on reset signal to reset the processor when the watchdog timer is not properly reset.
P2_7_CTS1_ IO P2_3_CTS0_IO	I/O	1	Clear-To-Send input is used to prevent the transmission of serial data on the TXD signal pin. CTS1 and CTS0 are multiplexed with an I/O Port function.
P2_6_BCLK1_IO P2_2_BCLK0_IO	I/O	1	Baud Clock input can be used as an alternate clock source for each of the integrated serial channels. The BCLK inputs are multiplexed with I/O Port functions. The BCLK input frequency cannot exceed (/2 the operating frequency of the processor.
P2_5_TXD1_IO P2_1_TXD0_IO	I/O	1	Transmit Data output provides serial data information. The TXD outputs are multiplexed with I/O Port functions. During synchronous serial communications, TXD will function as a clock output.
P2_4_RXD1_IO P2_0_RXD0_ IO	I/O	1	Receive Data input accepts serial data information. The RXD pins are multiplexed with I/O Port functions. During synchronous serial communications, RXD is bi-directional and will become an output for transmission of data (TXD becomes the clock).
DRQ3_O, DRQ2_O, DRQ1_O, DRQ0_O	O	1	DMA Request input pins are used to request a DMA transfer. The timing of the request is dependent on the programmed synchronization mode.

3 Timing Waveforms

3.1 CPU Write Cycle

3.1.1 CPU Write Cycle (RDY = 0 and without wait state)

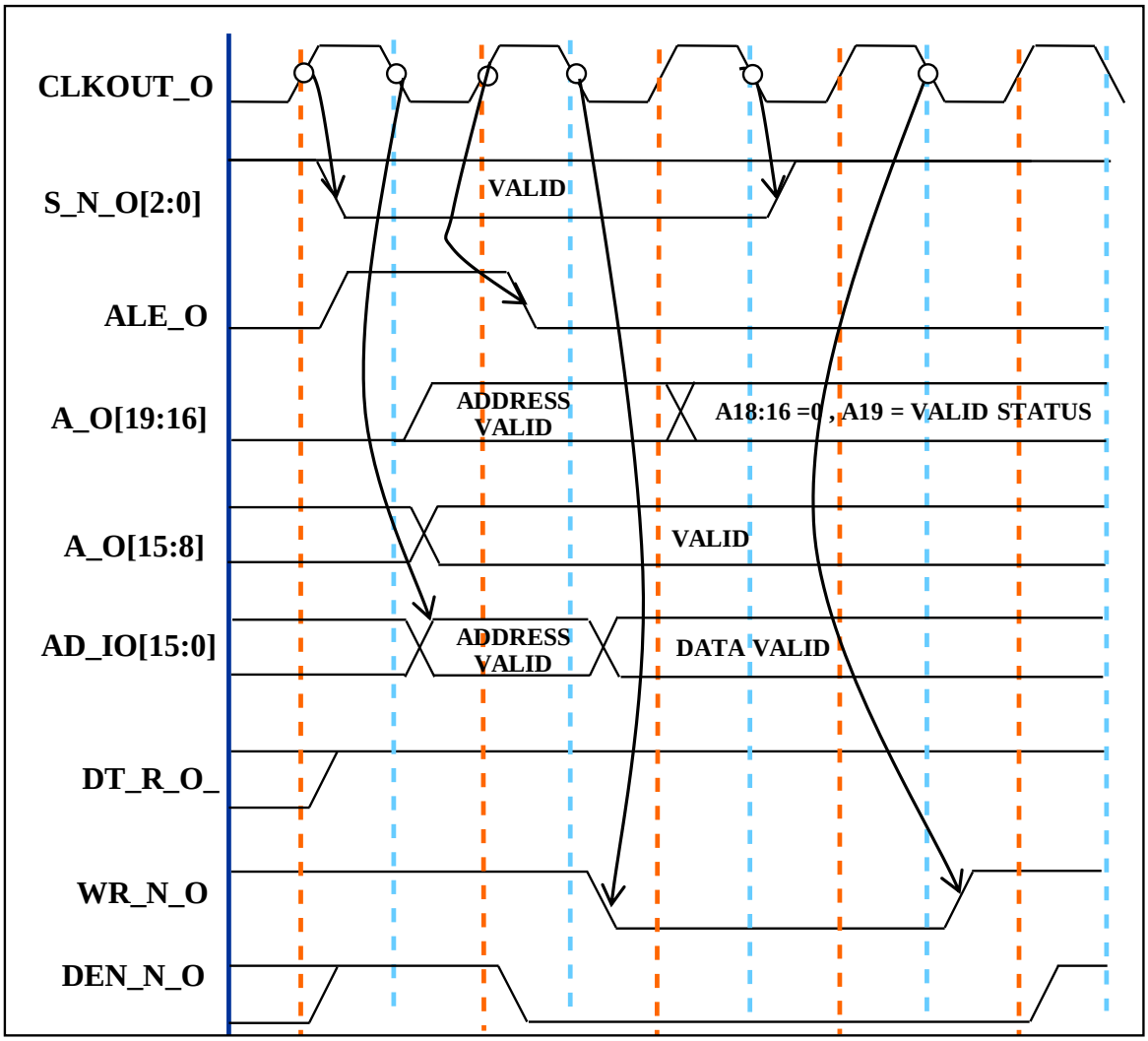

Figure 2: CPU Write Cycle (RDY = 0 and Without wait state)

3.1.2 CPU Write Cycle (RDY = 0 and with wait state)

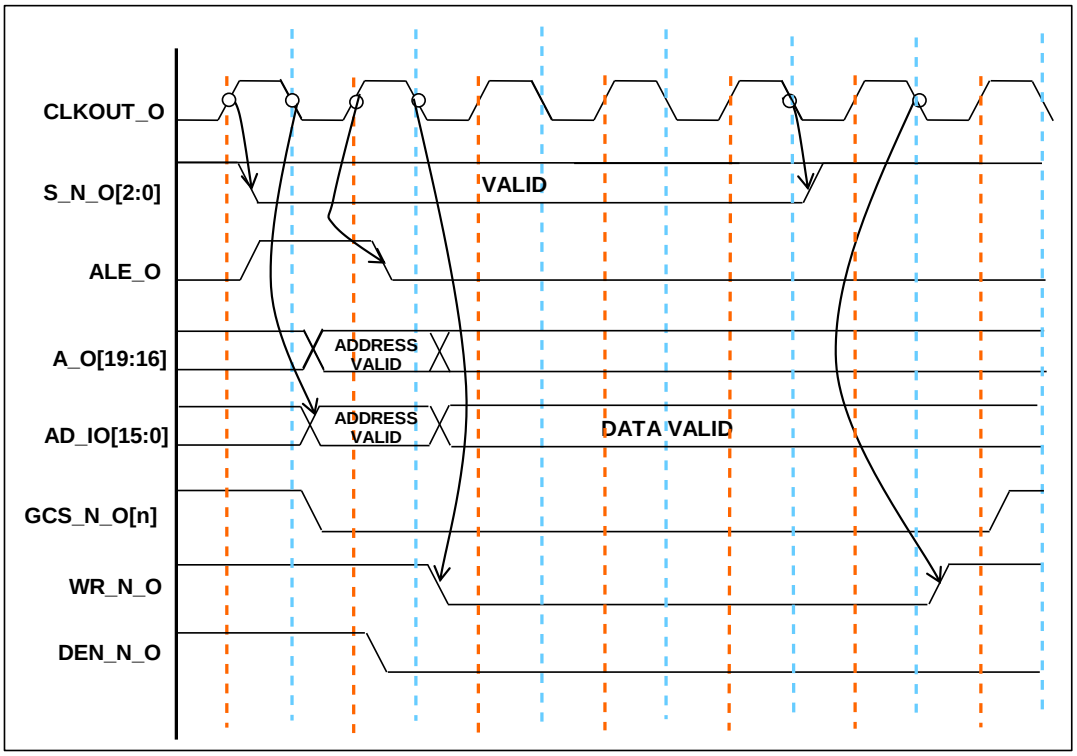

Figure 3: CPU Write Cycle (RDY = 0 and With wait state)

3.1.3 CPU Write Cycle (RDY = 1)

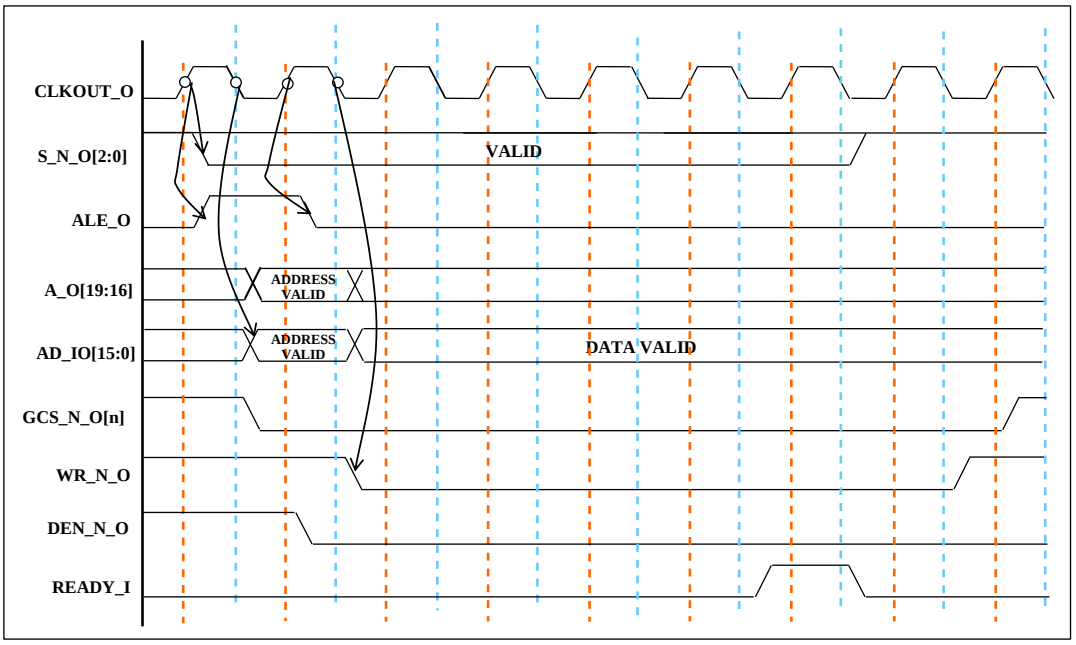

Figure 4: CPU Write Cycle (RDY = 1)

3.2 CPU Read Cycle

3.2.1 CPU Read Cycle

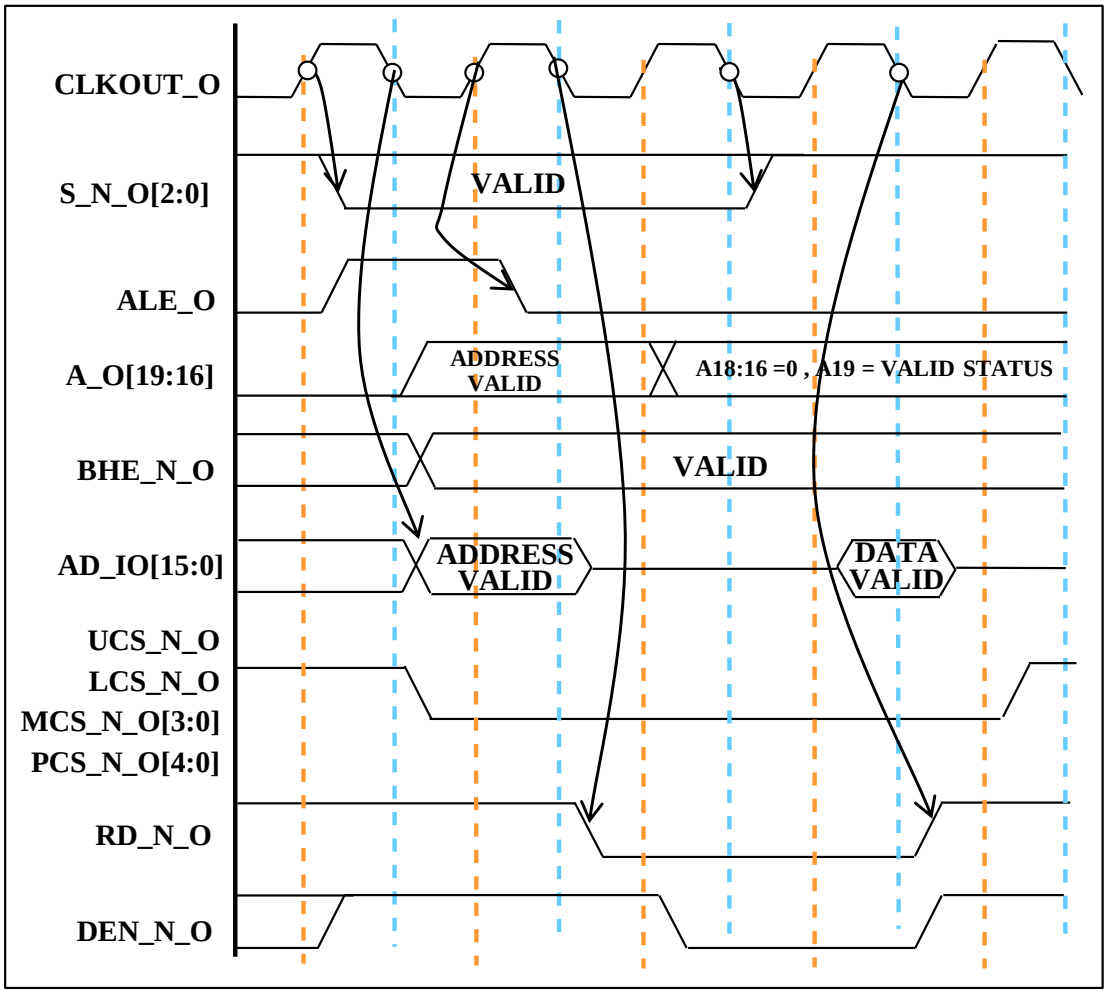

Figure 5: CPU Read Cycle

3.3 Interrupt Acknowledge Cycle

3.3.1 Interrupt Acknowledge Cycle

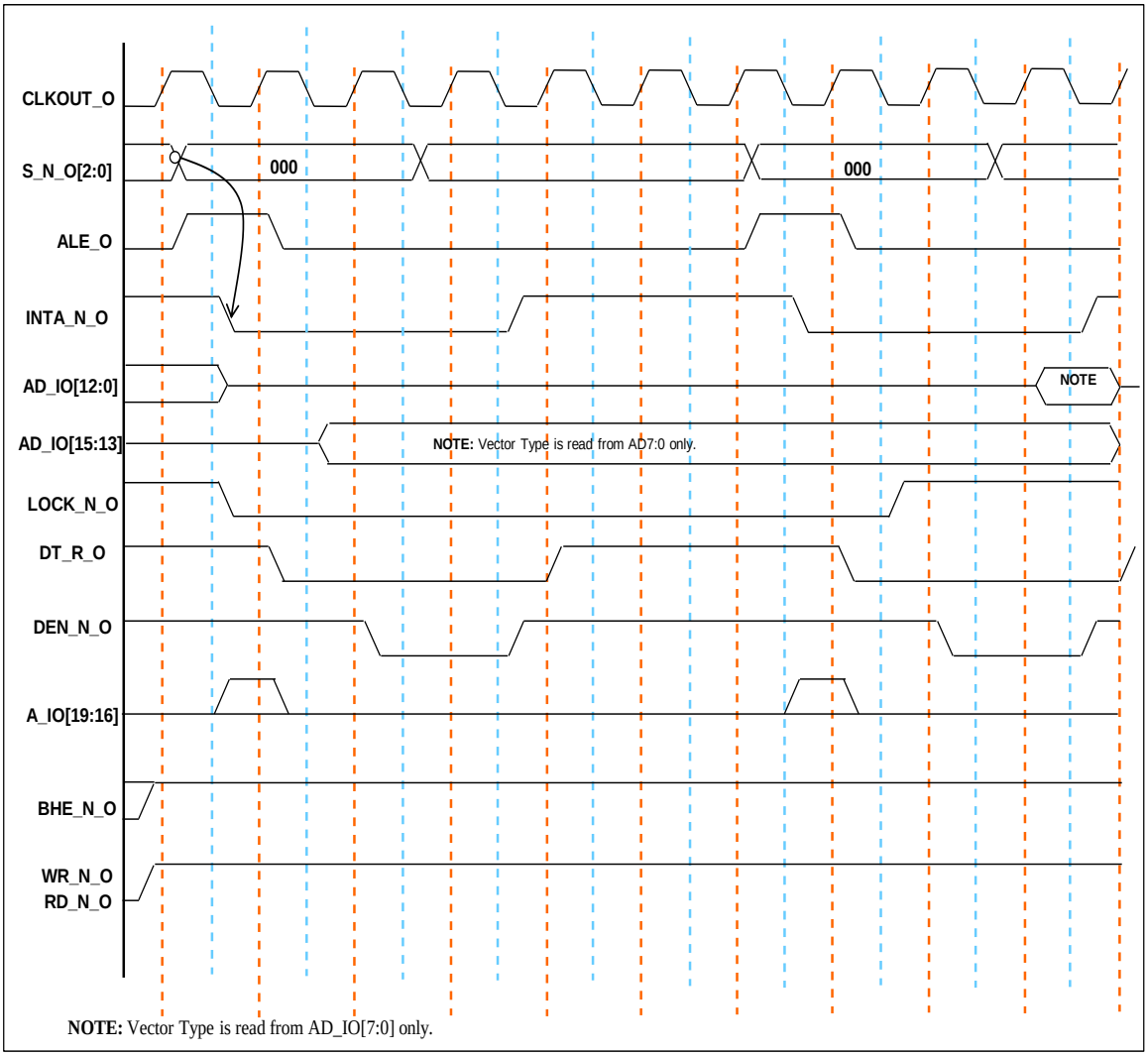

Figure 6: Interrupt Acknowledge Cycle

3.4 HOLD/HACK Cycle

3.4.1 HOLD/HACK Cycle

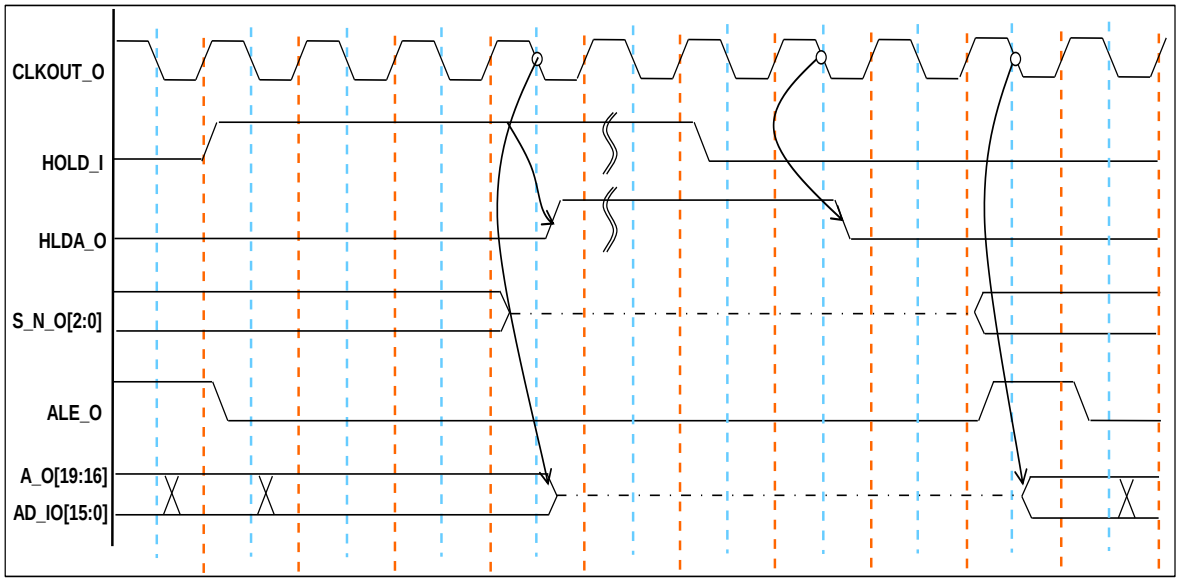

Figure 7: HOLD/HACK Cycle

3.5 HALT Cycle

3.5.1 HALT Cycle

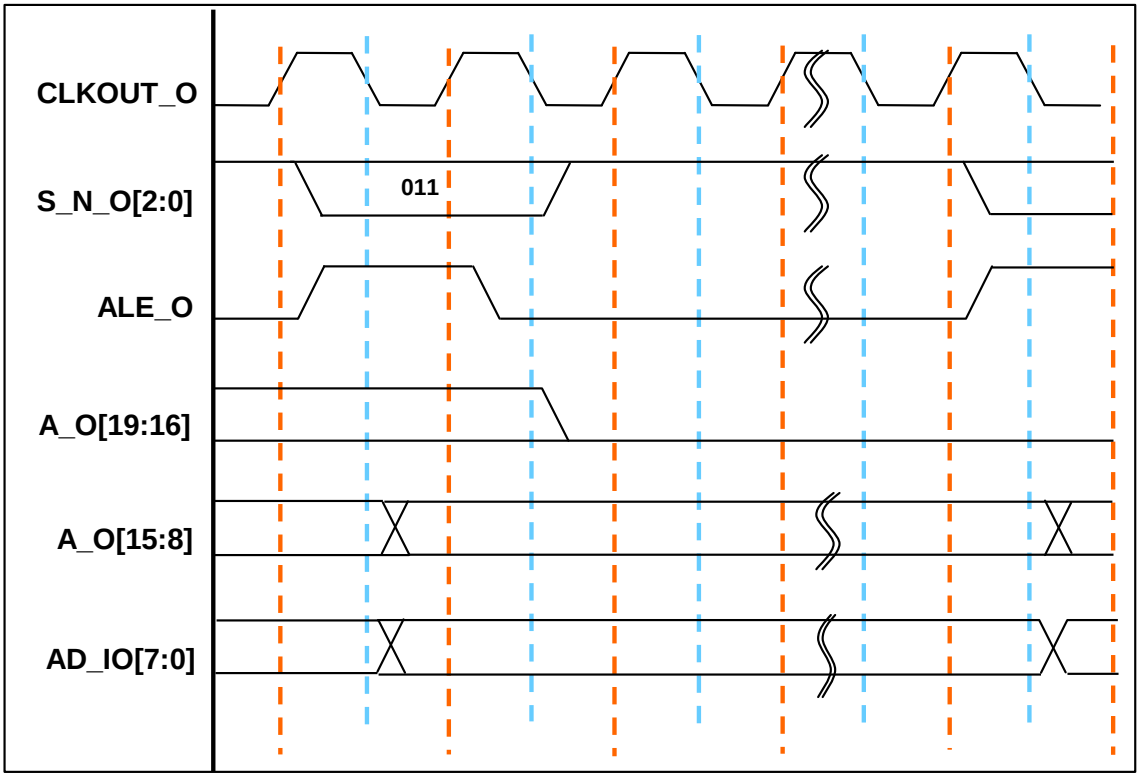

Figure 8: HALT Cycle

4 Implementation Results

The table below shows the utilization summary from the implementation of 80186EC Core for different FPGA devices.

Table 3: Device Utilization Summary for Actel ProASIC3

Logic Utilization	Used
Number of Core SEQ	3661
Number of Core COMB	17991
RAM/FIFO	1
Number of IOs	80

Table 4: Device Utilization Summary for Xilinx Spartan6

Logic Utilization	Used
Number of Slice Registers	3449
Number of Slice LUTs	6612
DSP48A1s	2
Number of IOs	80

Table 5: Device Utilization Summary for Altera Cyclone IV E

Logic Utilization	Used
Number of Logic Elements combinational	9467
Number of Logic Elements registers	3599
Embedded Multiplier 9-bit elements	4
Number of Pins	80

Table 6: Device Utilization Summary for Lattice XP2

Logic Utilization	Used
Number of Slice registers	3808
Number of Slice LUTs	9833
DSP Components MULT18X18C	2
Number of PIO	80