Data Sheet For Serial FPDP IP Core

iW-ASCDK-DS-01-R1.0

REL 1.2

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1. General Description

The ANSI/VITA 17.1-2003, or Serial Front Panel Data Port (FPDP), standard provides a relatively simple protocol for point-to-point data links between a sensor and a processor, using more than 99 percent of the available throughput with a minimum of protocol overhead. In addition to link efficiency, the simplicity of the protocol makes it easy to implement a Serial FPDP endpoint in an FPGA. The Serial FPDP standard supports three data rates: 1.0625 Gbaud, 2.125 Gbaud, and 2.500 Gbaud. Control and data packets are encoded using 8B/10B encoding, resulting in data transfers at 247 megabytes per second using a 2.5 GBd serial link after encoding and protocol overhead. Serial FPDP links support a wide range of physical interfaces with the most common option being 2.5 gigabits per second multimode fiber.
iWave Serial Front Panel Data Port (sFPDP) IP core for FPGA is based on the ANSI/VITA 17.1-2003 standard. This intellectual property core can be implemented on any transceiver based Xilinx/Altera/Lattice FPGAs.

2. Features

The following are the main features of the Serial FPDP IP core:

- Compliant with ANSI/VITA 17.1-2003 Serial FPDP standard
- Supported link speeds
  - 1.0625 Gbaud
  - 2.125 Gbaud
  - 2.5 Gbaud
- Data Frames supported
  - Unframed Data
  - Single Frame Data
  - Fixed Size Repeating Frame Data
  - Dynamic Size Repeating Frame Data
- System Configurations supported
  - Basic System
  - Flow Control
  - Bi-directional Data Flow
  - Copy Mode
  - Copy/Loop Mode
- Host-Bus interface
  - Parallel FPDP
- Configurable parameters
  - Transmit FIFO depth
  - Receive FIFO depth
  - Transmit FIFO watermark to assert SUSPEND output
  - Receive FIFO watermark for STOP/GO signal generation
  - Transceiver Interface Data Width

3. Block Diagram

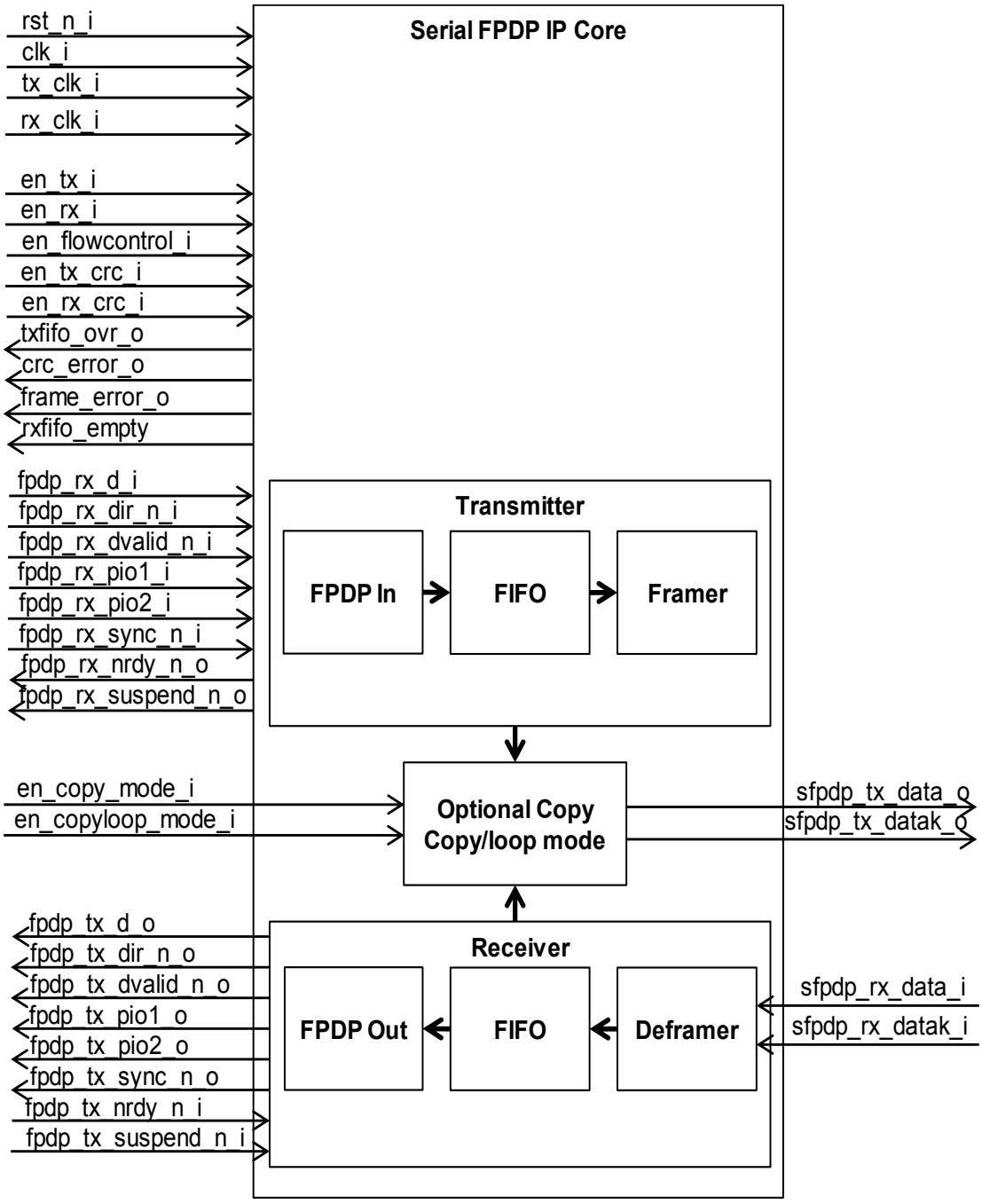

Figure 1: Serial FPDP IP Core Block Diagram

4. IO Signals

Table 1: Serial FPDP IP Core IO Signals

Signal	Dir	Width	Description
Clock & Reset Signals			
rst_n_i	I	1	Reset
fpdp_clk_i	I	1	FPDP Clock
sfpdp_clk_i	I	1	sFPDP Clock
Control & Status Signals			
en_tx_i	I	1	Transmitter Enable When HIGH enables transmission of sFPDP frames.
en_rx_i	I	1	Receiver Enable When HIGH enables receiving of sFPDP frames.
en_flowcontrol_i	I	1	Flow Control Enable When HIGH enables flow.
en_copy_mode_i	I	1	Copy Mode Enable When HIGH enables copy mode of operation.
en_copyloop_mode_i	I	1	Copy/Loop Mode Enable When HIGH enables copy/loop mode of operation.
en_tx_crc_i	I	1	Transmitter CRC enable When HIGH enables generation of CRC in transmit sFPDP frames.
en_rx_crc_i	I	1	Receiver CRC enable When HIGH enables checking of CRC in receive sFPDP frames.
rx_crc_error_o	O	1	Receive CRC Error When HIGH indicates sFPDP frame received with CRC error. Signal driven from sfpdp_clk domain.
remote_txfifo_ovr_o	O	1	Remote Transmit FIFO Overflow When HIGH indicates Transmit FIFO Overflow received from remote transmitter. Signal driven from sfpdp_clk domain.
FPDP Signals			

Signal	Dir	Width	Description
fpdp_rx_d_i	I	32	D[31:0] from FPDP
fpdp_rx_dir_n_i	I	1	DIR* from FPDP
fpdp_rx_sync_n_i	I	1	SYNC* from FPDP
fpdp_rx_dvalid_n_i	I	1	DVALID* from FPDP
fpdp_rx_pio1_i	I	1	PIO1 from FPDP
fpdp_rx_pio2_i	I	1	PIO2 from FPDP
fpdp_rx_nrdy_n_o	O	1	NRDY* to FPDP
fpdp_rx_suspend_n_o	O	1	SUSPEND* to FPDP
fpdp_tx_d_o	O	32	D[31:0] to FPDP
fpdp_tx_dir_n_o	O	1	DIR* to FPDP
fpdp_tx_sync_n_o	O	1	SYNC* to FPDP
fpdp_tx_dvalid_n_o	O	1	DVALID* to FPDP
fpdp_tx_pio1_o	O	1	PIO1 to FPDP
fpdp_tx_pio2_o	O	1	PIO2 to FPDP
fpdp_tx_nrdy_n_i	I	1	NRDY* from FPDP
fpdp_tx_suspend_n_i	I	1	SUSPEND* from FPDP
Transceiver Signals			
sfpdp_tx_data_o	O	32	Transmit Data
sfpdp_tx_datak_o	O	4	Transmit Control Enable
sfpdp_rx_data_i	I	32	Receive Data

Signal	Dir	Width	Description
sfpdp_rx_datak_i	I	4	Receive Control Enable

5. Functional Description

The main blocks in Serial FPDP IP core are:

- **Transmitter**: On the transmit side, the parallel FPDP data is converted to Serial FPDP. It consist of mainly 3 modules.
  - **FPDP In**: Used to receive data from host bus (FPDP bus).
  - **FIFO**: Used to store the data from FPDP data frame.
  - **Framer**: Used to frame sFPDP data frames and send to transceiver.
- **Receiver**: On the receive side, the Serial FPDP data is converted back into the FPDP parallel data stream. It consist of mainly 3 modules.
  - **Deframer**: Used to defame the data frames coming for sFPDP link.
  - **FIFO**: Used to store the data from decoded sFPDP data frame.
  - **FPDP Out**: Used to drive the data to host-bus using FPDP bus

6. Timing Waveforms

Below waveforms shows the timing diagram of Host-Bus interface

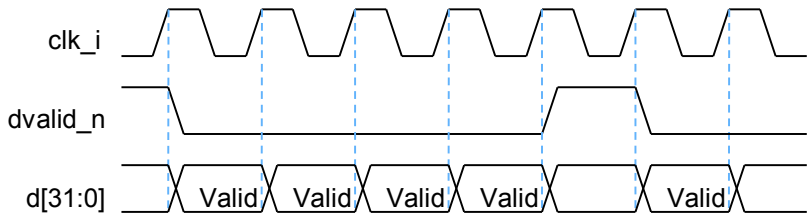

Figure 2: Unframed Data

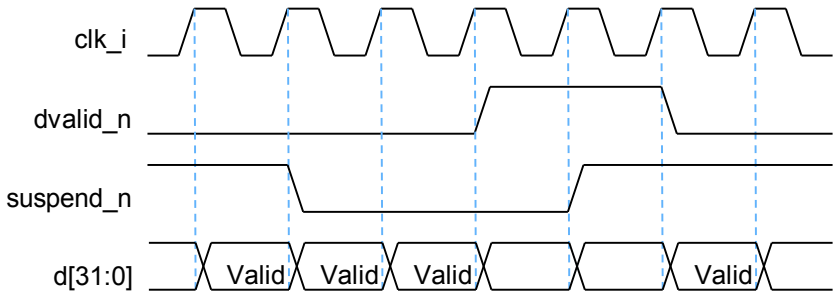

Figure 3: SUSPEND Timing

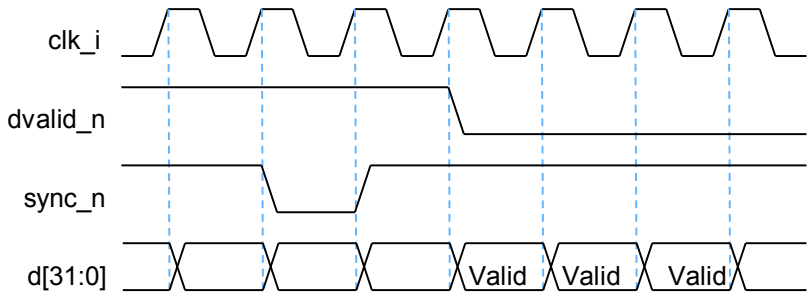

Figure 4: Single Frame Data

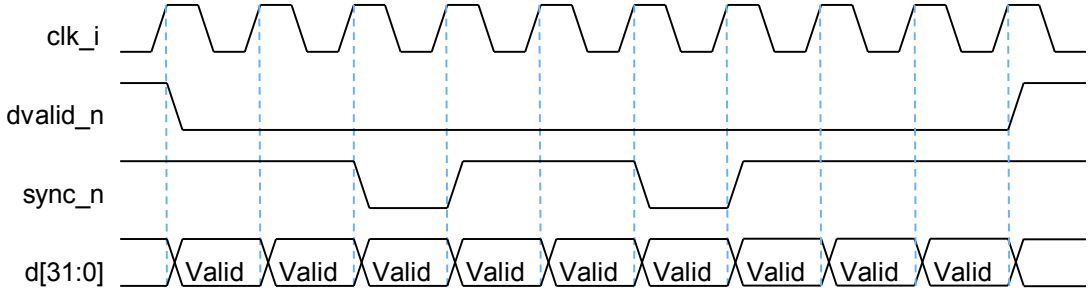

Figure 5: Repeating Frame Data

7. Resource Utilization

The table below shows the utilization summary from the implementation of Serial FPDP IP core for different FPGA devices. IP configured for following

1. Tx FIFO depth 1024
2. Rx FIFO depth 1024
3. Transceiver interface data width 16-bit

Table 2: Device Utilization Summary for Xilinx Spartan-6 LXT

Logic Utilization	Used
Slice Registers	893
Slice LUTs	1032
RAMB16BWERs	4

Table 3: Device Utilization Summary for Xilinx Kintex 7 XC7K70T

Logic Utilization	Used
Slice Registers	893

Slice LUTs	915
36K BlockRAMs	2

Table 4: Device Utilization Summary for Altera Cyclone IV GX

Logic Utilization	**Used**
Logic Cells	1402
Dedicated Logic Registers	777
M9Ks	9

Table 5: Device Utilization Summary for Altera Stratix IV GX

Logic Utilization	**Used**
Combinational ALUTs	809
Dedicated Logic Registers	773
M9Ks	9

Table 6: Device Utilization Summary for Lattice ECP3

Logic Utilization	**Used**
LUT4s	1100
Registers	730
Block RAMs	4