Data Sheet for SDIO to UART Bridge

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	07th Sept'12	Internal review feedback updated	VC

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1 Introduction

1.1 Purpose

This document describes the Technical Specification of the SDIO Device core. It includes the overall architectural description, detailed functional specifications and interface definitions for the SDIO to UART Bridge.

1.2 Features

The following are the main features of the SDIO to UART Bridge:

- Compliant with SD Physical Specification Version 2.00 and SDIO Specification Version 2.00.
- Supports SPI, 1-bit and 4bit SD modes.
- Supports SDIO Interrupt feature
- Supports all mandatory SDIO Commands/Response types
  - SPI Mode : CMD0, CMD5, CMD52, CMD53, CMD59
  - SD Mode : CMD0, CMD3, CMD5, CMD7, CMD52, CMD53.
- CRC7 checking/generation for Command/Response
- CRC16 checking/generation for Data transfer.
- Supports High Speed Mode (up to 50Mhz) of operation.
- Data Transfer in Multi Byte and Multi Block mode using CMD53.
- SDIO only implementation, Combo card features are not supported
- Optional Code Storage Area(CSA) is not supported
- Suspend/Resume Features not supported
- Supports UART16550 function:
  - Programmable baud generator divides any input clock by 1 to (2^{16} - 1) and generates the 16x clock.
  - MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD)
  - 5, 6, 7, or 8-bit characters
  - Even, odd, or no-parity bit generation and detection
  - 1, 1/2, or 2-stop bit generation
  - Baud generation (DC to 1.5M baud)
  - Line break generation and detection
  - Independently controlled transmit, receive, line status, and data set interrupts

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
CIA	Common I/O Area
CIS	Card Information Structure
CRC	Cyclic Redundancy Check
CSA	Code Storage Area
FIFO	First In First Out queue
FPGA	Field Programmable Gate Array
FSM	Finite State machine
GPIO	General purpose Input/output
LSB	Least Significant Byte
MSB	Most Significant Byte
OCR	Operations Conditions Register
RAM	Random Access Memory
RCA	Relative Card Address
SDIO	Secure Digital Input Output
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

2 SDIO to UART Bridge

2.1 Block Diagram

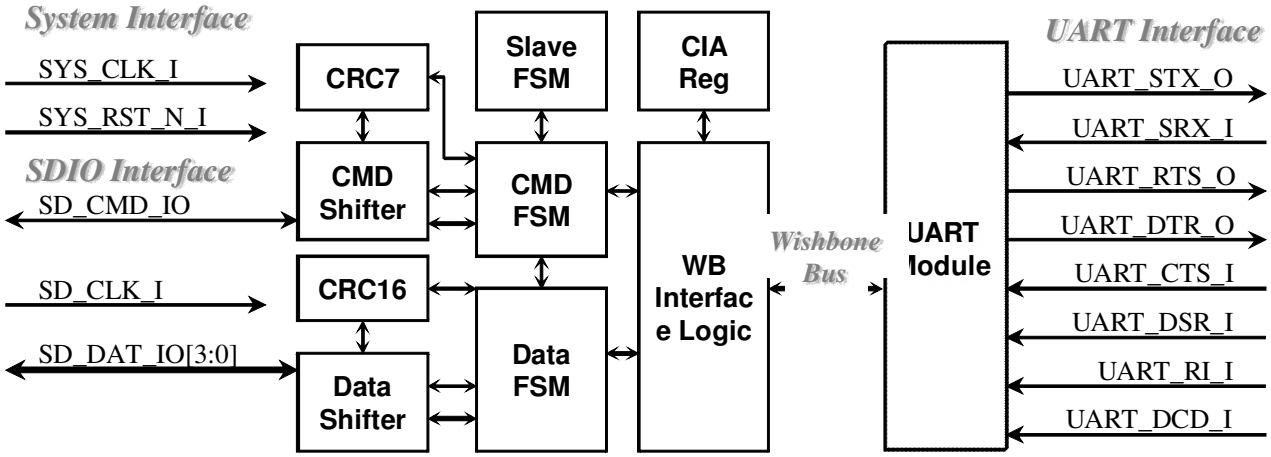

Figure 1: SDIO to UART Bridge Block Diagram

2.2 Description

The main blocks in SDIO to UART Bridge are

- **SDIO Slave**: This module has Logic that implements the SDIO Slave device. Here the Physical bus interface takes care o the Command and Data bus interface. This module supports CRC checking and generation for both Command and Data. SDIO Function0 registers and other registers are supported as per the SDIO specification. A Wishbone interface is supported to interface Device Function Area.
- **UART Module**: The UART (Universal Asynchronous Receiver/Transmitter) core provides serial communication capabilities, which allow communication with modem or other external devices, like another computer using a serial cable and RS232 protocol. This core is designed to be maximally compatible with the industry standard National Semiconductors' 16550A device

2.3 I/O Signals

Table 2: System Interface IO Signal Description

Signal	I/O	Width	Description
SYS_RST_N_I	I	1	System Reset. Active Low Asynchronous reset input.
SYS_CLK_I	I	1	System Clock. Clock input to the FPGA This clock is used for the UART Logic.

Table 3: SDIO Interface IO Signal Description

Signal	I/O	Width	Description
SD_CLK_I	I	1	SDIO Bus Clock input.
SD_CMD_IO	I/O	1	SDIO Command SDIO bi-directional line for command and response token.
SD_DAT_IO[3:0]	I/O	4	SDIO Data SDIO bi-directional lines for data read and write. SD_DAT_IO[1] line is also used by card to interrupt the host.

Table 4: UART Interface IO Signal Description

Signal	I/O	Width	Description
UART_STX_O	O	1	UART Serial output Transmit serial Data output to the communications link
UART_SRX_I	I	1	UART Serial input Receive Data input from the communication link

Signal	I/O	Width	Description
UART_RTS_O	O	1	UART Request to Send When low, this informs the MODEM or data set that the UART is ready to exchange data. The RTS output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register.
UART_DTR_O	O	1	UART Data Terminal Ready When low, this informs the MODEM or data set that the UART is ready to establish a communications link.
UART_CTS_I	I	1	UART Clear To Send When low, this indicates that the MODEM or data set is ready to exchange data. The CTS signal is a MODEM status input.
UART_DSR_I	I	1	UART Data Set Ready When low, this indicates that the MODEM or data set is ready to establish the communications link with the UART. The DSR signal is a MODEM status input.
UART_RI_I	I	1	UART Ring Indicator When low, this indicates that a telephone-ringing signal has been received by the MODEM or data set.
UART_DCD_I	I	1	Data Carrier Detect When low, indicates that the data carrier has been detected by the MODEM or data set. The DCD signal is a MODEM status input. DCD has no effect on the receiver

3 Timing Waveforms

3.1 SDIO Interface

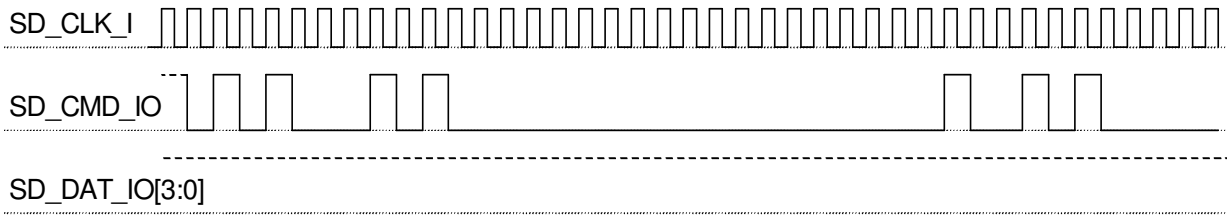

Figure 2: Command Write

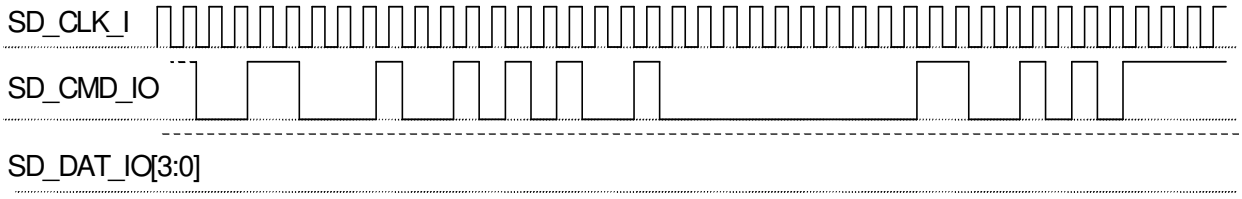

Figure 3: Response Read

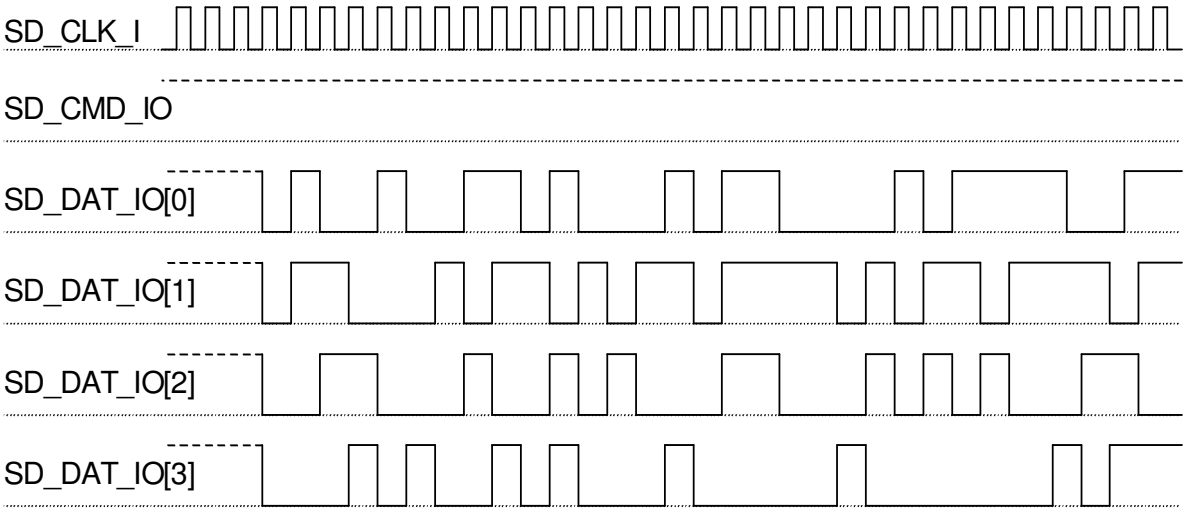

Figure 4: Data Write 4-bit mode(Data Transfer)

3.2 Wishbone Interface

3.2.1 Classic Cycle

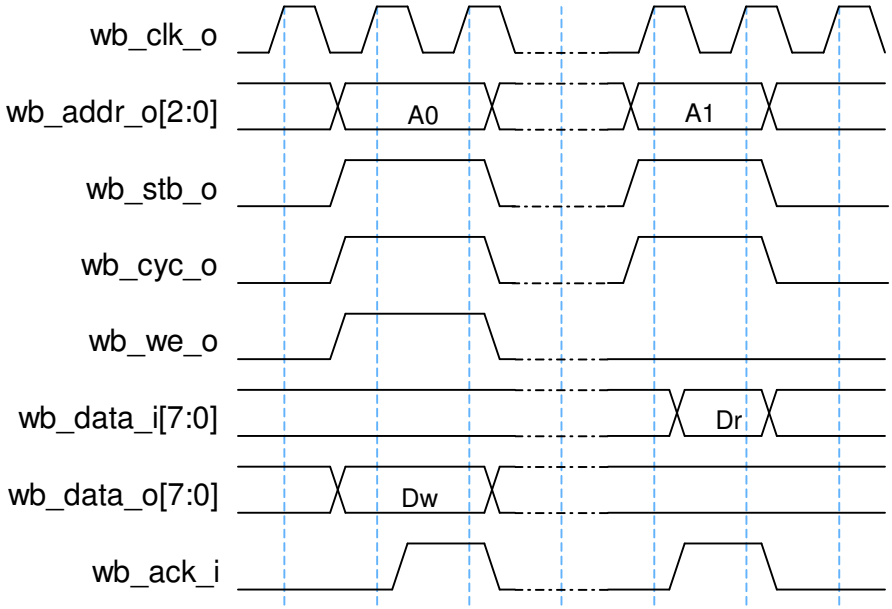

Figure 5: Wishbone Interface Classic Cycle Read/Write Timing Diagram

3.2.2 Burst Write Cycle

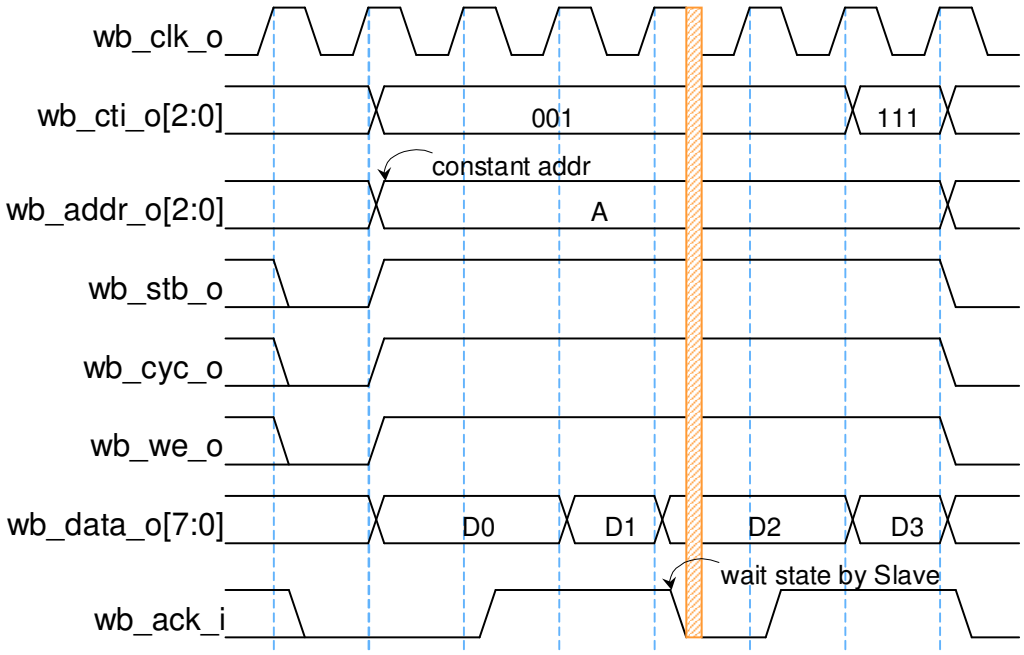

Figure 6: Wishbone Interface Burst Write Timing Diagram

3.2.3 Burst Read Cycle

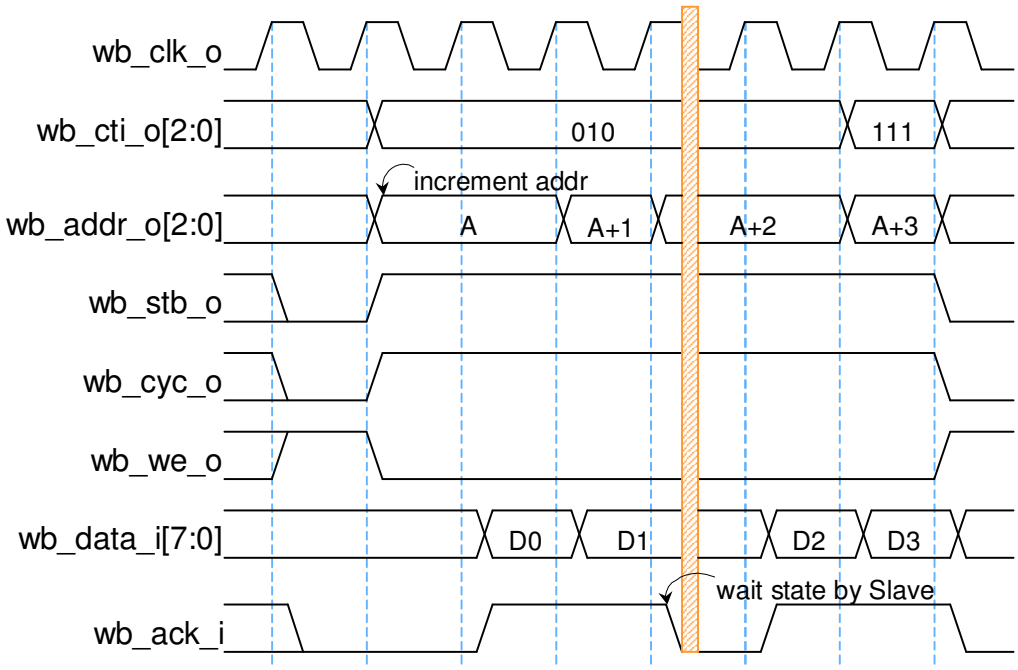

Figure 7: Wishbone Interface Burst Read Timing Diagram