Data Sheet for PCIe to UART Bus Controller

DOCUMENT REVISION HISTORY

Revision	Date	Change Description	Author
1.0	22nd Jan 2009	Draft version	CP
REL 1.0	16th Aug 2012	Removed implementation results	VC

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1 Introduction

1.1 Purpose

The purpose of this document is to describe the technical specifications of PCIe to UART bus controller implemented on the FPGA.

1.2 Features

The following are the main features of the PCIe to UART Bus Controller:

- System Interface
  - 100MHz external reference clock for synchronous clocking of PCI express Interface
  - Supports interface to external active low reset signal
- PCI Express Interface
  - Compliant with the PCI Express base specification v1.1
  - Lane width supported x1
  - Link speed supported 2.5 Gbps
  - User interface width supported 32-bit
- PCI Express Application Interface
  - Target only support
  - Memory BAR0 supported for UART controller.
- UART Interface
  - The UART bridge uses IO mapped interface
  - Full duplex asynchronous communication
  - Baud rate of 115200 with a single odd parity, stop & start bit
  - Supports transmit & receive synchronous FIFO of size 16 byte depth

1.3 Acronyms and Abbreviations

Table 1: Acronyms & Abbreviations

Term	Meaning
FPGA	Field Programmable Gate Arrays
BAR	Base Address Register
PHY	Physical Layer
UART	Universal Asynchronous Receiver Transmitter
PIO	Programmed Input Output
TLP	Transaction Layer Packet
SCU	Serial Control Unit

2 PCIe to UART Bus Controller

2.1 Block Diagram

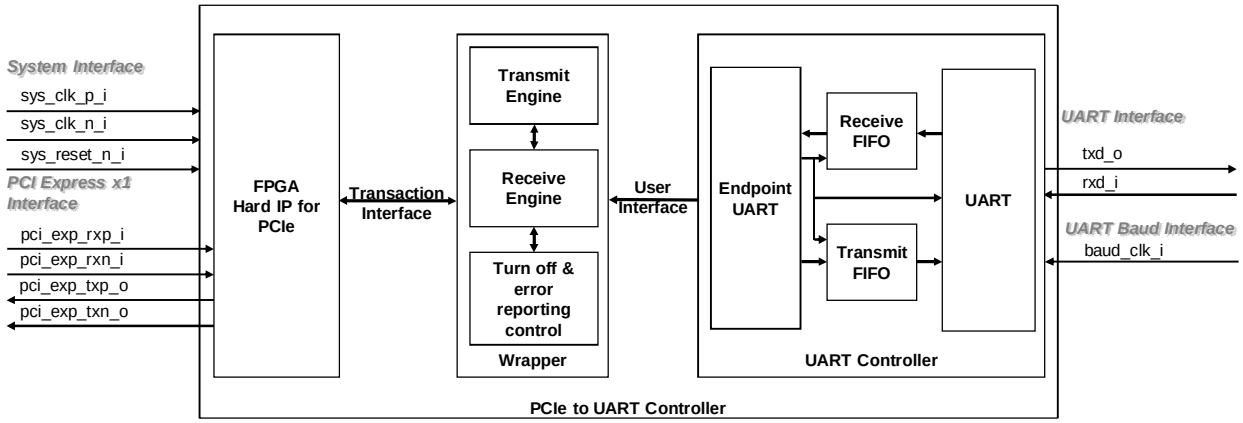

Figure 1: PCIe to UART bus Controller Block Diagram

2.2 Description

- **PCIe Endpoint**: This is a hard macro IP from Xilinx/Altera. It implements Gen1 x1 PCIe endpoint.
- **Transmit Engine:** This module handle the Transmit TLP packet to PCIe Hard IP.
- **Receive Engine:** This module handle the Receive TLP packet from PCIe Hard IP.
- **UART Controller:** The UART controller is implemented in user interface side of the PIO design. The UART controller consists of Endpoint UART module, simple UART Module, synchronous FIFO module on both transmit & receive path.

2.3 I/O Description

Table 2: System Interface IO Signals

Signal	I/O	Width	Description
sys_clk_p_i	I	1	Reference clock Positive: 100 MHz
sys_clk_n_i	I	1	Reference clock Negative: 100 MHz
sys_reset_n_i	I	1	Asynchronous signal. This signal is used to reset the PCI Express block, the GTP transceiver, the block RAM, and the PLL. The minimum pulse width for this input signal is 1500 ns.

Table 3: PCIe Interface IO Signals

Signal	Dir	Width	Description
pci_exp_txp_o	O	1	PCI Express Transmit Positive: Serial Differential Output 0 (+)
pci_exp_txn_o	O	1	PCI Express Transmit Negative: Serial Differential Output 0 (–)
pci_exp_rxp_i	I	1	PCI Express Receive Positive: Serial Differential Input 0 (+)
pci_exp_rxn_i	I	1	PCI Express Receive Negative: Serial Differential Input 0 (-)

Table 4: UART Interface Signal Description

Signal	Dir	Width	Description
TXD_O	O	1	Transmit signal
RXD_I	I	1	Receive signal
BAUD_CLK_I	I	1	Baud clock signal

3 Timing Waveforms

3.1 UART Waveforms

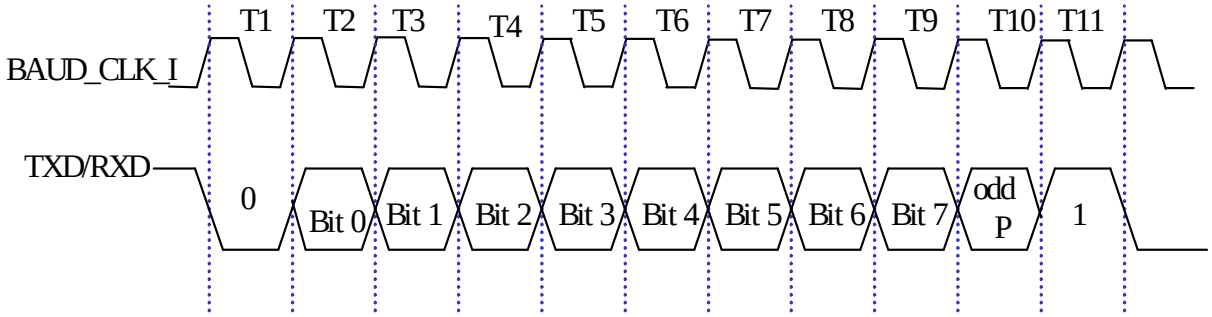

Figure 2: UART Transmit/Receive waveform