iWave's Serial Front Panel Data Port core:
Cost-effective embedded solution for Medical imaging, Video, DSP & much more

The Serial Front Panel Data Port (sFPDP) is used in a wide range of high-performance embedded systems like Radar/Sonar, Digital Signal Processing, Medical Imaging and Video Production for sensor-to-processor interfaces. While Ethernet is a good choice for many military applications, Serial FPDP offers major advantages for streaming high-bandwidth sensor data.

iWave's Serial FPDP is a high-speed low-latency data-streaming serial communication protocol for use in high-speed real-time data transfer applications. It is a simple protocol for point-to-point data links between a sensor and a processor, using more than 99 percent of the available throughput with a minimum of protocol overhead. In addition to link efficiency, the simplicity of the protocol makes it easy to implement a Serial FPDP endpoint in an FPGA.

Many kinds of high-performance embedded computing systems in many applications have an appetite for high speed data transfer from the sensors. For such applications, Serial Front Panel Data Port (FPDP) or ANSI/VITA 17.1-2003 provides a simple point-to-point protocol with high throughput and minimum latency.

sFPDP has been used with great success in medical applications, where the sensor translates ultrasonic pulses into strains in single-mode optical fibers. At the sensor, each channel of data is generated by an embedded module that contains a FPGA device. Within the FPGA device, sensor data is provided to a FIFO interface that generates Serial FPDP data streams. It provides good packetization support with maximum payload size of 2,048 bytes and use the 2.5 Gbit/s and non-standard higher bit rate such as 3.125, 4.25, 5.0, or 6.4 Gbit/s all of which can be implemented using the transceiver based FPGA devices. By using Serial FPDP’s synchronization mechanism, Multichannel processing can be achieved. The data can be transmitted to multiple destinations using ‘Copy Mode’ option of the sFPDP.

Serial FPDP interface with an FPGA-based I/O module can be used in many applications which require maximum throughput with minimum processor overhead. Serial FPDP can be used between API (Application Programming Interface) and PCI-X or PCI Express interface.

The sFPDP data streams are received using an I/O module which includes a software driver and API library that provides a high-level interface to the user’s software application. This data stream is decoded and transferred to the processor memory through a PCI-X or PCI Express interface.

In some applications since Serial FPDP has a built-in synchronization feature, the I/O module can use Direct Memory Access (DMA) to transfer a data block directly into user memory which avoids the need for a software memory copy. This reduces both processor overhead and system latency. (continued on p2)
iWave’s Serial FPDP IP core for FPGA is based on the ANSI/VITA 17.1-2003 standard. The Serial FPDP standard supports three data rates: 1.0625 Gbaud, 2.125 Gbaud and 2.500 Gbaud. Control and data packets are encoded using 8B/10B encoding, resulting in data transfers at 247 megabytes per second using a 2.5 GBd serial link after encoding and protocol overhead. Serial FPDP links support a wide range of physical interfaces with the most common multimode fibre option of 2.5 gigabits per second (Gbps).

This sFPDP core can be used in point-to-point or loop topologies, uni-directional or bi-directional links and it easily supports different types of data with efficient data framing options for dataflow control, copy mode and copy/loop mode. These modes offer great flexibility in data transfer and allow for multiple end-points which are especially useful when simultaneously recording and processing data. It supports unframed, single frame, fixed size repeating frame and dynamic size repeating frame data. SFPDP design can be configured for ANY Transceiver Interface data width supported by the FPGA.

The simple architecture of iWave’s Serial FPDP IP core has Parallel FPDP bus as host interface. User control and status information are provided through control & status Interface. Transceiver interface supported is either 32-bit or 16-bit. Transceiver Data width can be configured via parameter. The Host-Bus, Parallel FPDP, supplies data to a Transmit FIFO and the Serial FPDP logic removes this data from this FIFO, encodes it, serializes it, and transmits it across the link using the framing protocol. The receiver performs in a similar but reverse manner.

The Serial FPDP IP core is provided in simple verilog source, which has been fully verified using system verilog. The design consists of configurable parameter which provides flexibility to the design. This Serial FPDP IP Core use transceiver available inside FPGA for physical layer. This flexible and simple architecture can be implemented in any transceiver based Xilinx/Altera/Lattice FPGA.

--- Preeti Naik

For Additional details about the core: www.iwavesystems.com/?q=node/252

--- Crest

iWave’s i.MX50x SOC:
An industry-first to integrate ARM Cortex-A8 with E-Ink hardware display controller

The i.MX50x processor delivers a low-power, streamlined solution for customers seeking ARM Cortex-A8 performance levels with flexible design features. It boasts, Ethernet, Dual USB, Dual SD, micro USB Device, VGA out, Audio IN/OUT & Serial interfaces, enabling developers to quickly prototype their application needs around i.MX50x processor while optimizing the development effort and “time to market” of their products.

The i.MX50x System-on-Chip was the first SoC to integrate advanced ARM Cortex-A8 technology with a hardware-based display controller from E-Ink. Offering high resolution, easy readability and exceptional energy efficiency, EPDs allow system designers to create exciting new display-based products that deliver ultra-low power consumption and extremely long battery life. i.MX50x based QSb is ideal for applications like Industrial HMIs. In any automation design the interaction between human–machine plays a vital role for effective operation and control/remote monitoring of the machine and also to collect the feedback from the machine not only aids in smooth running of the machine but also assists the operator in making optimum operational decisions for which “always-on” functionality is essential. An integrated, enhanced LCD interface offers maximum display flexibility supporting even the simultaneous deployment of EPD and LCD displays in a single end product. The i.MX50x supports LCD displays with resolution up to 1280 x 1024 pixels (SGXA) and also supports resistive touch.

Code Optimization techniques for better CPU utilization
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In today’s competitive embedded world one of the most important factors while designing any system would be customizing the software for a better CPU utilization.

The CPU (Central Processing Unit) is the most important part of a system because it will act as brain of the system. So better use of the brain (CPU) will directly result in better performance.

As an example if a hard disk is transferring data over the interface to the rest of the system, it uses some of the system’s resources.

One of these critical resources is how much CPU time is required for a particular transfer. Because higher the percentage of the CPU used by the data transfer the less execution time CPU can devote to other tasks. This time utilization is generally known as CPU utilization. The CPU time is often measured in clock ticks or as a percentage of the CPU’s capacity. It is used to measure the CPU workload of a program.

CPU utilization will provide the details regarding how much CPU is busy at that moment. In short the CPU utilization will be defined as “keeping CPU free as much as possible”.

The current embedded field is dominated by RTOS such as WinCE, RTLinux, VxWorks, Threadx because of their own special qualities. The major feature of all RTOS is multithreading.

In multithreading system there will be multiple threads running at the same time to handle various real time tasks. So sharing CPU among the multiple running threads is an important task handled by the operating system. Because of which CPU utilization is a critical factor for any operating system that should be optimized.

The improvement in CPU utilization will result in better performance of any applications running on that operating system. The performance variation can be better visualized in GUI (Graphical User Interface) related applications by the response of the application to the user. Thus CPU utilization is one of the critical factors to be addressed. While writing any software/application in C++ for any system there are some simple techniques/guidelines if followed will result in better CPU utilization.

“Code optimization” is one of the most efficient ways to optimize the CPU utilization in software. If simple but powerful C++ points are taken care a better CPU utilization can be achieved. This article highlights such simple yet powerful techniques and details 10 points for achieving a better CPU utilization.

Youkoso irasshai mashita!

Welcome to iWave Japan!

iWave CEO, M.A. Mohamed Saliya and President A. Khan (second and third from left) with iWave Japan President Osamu Kanno (second from right) and Project Manager Jishad (far right) at the 2011 Embedded Technology Show in Yokohama.

iWave Japan Inc. was established in Yokohama, in September 2007, complementing the Japanese branch of iWave Systems Technologies Pvt. Ltd. which has been in Japan since 2000.

The founder-President of iWave Japan is Osamu Kanno. He has a Masters degree in Electronics from National Iwate University and long experience of electronic devices sales. Another key person for iWave in Japan is Project Manager Jishad. He graduated from Kannur University, India and is fluent in Japanese.

In its decade and more in Japan, iWave has served a number of prestigious clients including Nippon Signals, Japan’s Railways and Aerospace departments.

iWave Japan coordinates with iWave Systems Technologies, and takes part in FTF(Freescale Technology Forum) at Tokyo, ET(Embedded Technology) at Yokohama and ESEC (Embedded Systems Expo) at Tokyo every year.

iWave shines at Indian DwF events, with range of market-ready solutions

iWave participated in the Designing with Freescale (DwF) events at Chennai, Hyderabad, Pune & Delhi this year with great success. The audience consisted predominantly of industrial and automotive developers, who showed keen interest in our platforms and solutions for the Freescale 50x, 53x and 6x processors.

In fact, iWave was the only design house at these events showcasing ready-to-deploy and market-oriented solutions and reference designs.

And another first for iWave: We showcased the only solutions with respect to i.MX6 Q7 SOM incorporating i.MX6-the popular Freescale chip for multimedia applications!

Meet iWave engineers and executives at these international shows in 2012:

- FTF Americas 2012
  - San Antonio, Texas (USA)
  - June 18-21 2012

- FTF Japan 2012
  - October 20-23 2012
  - Tokyo

- Designing with Freescale Market Solutions Seminar
  - Paris, France
  - October 16 2012

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