

iWSPI4.2G1 – UTOPIA POS-PHY 4.2 Interface

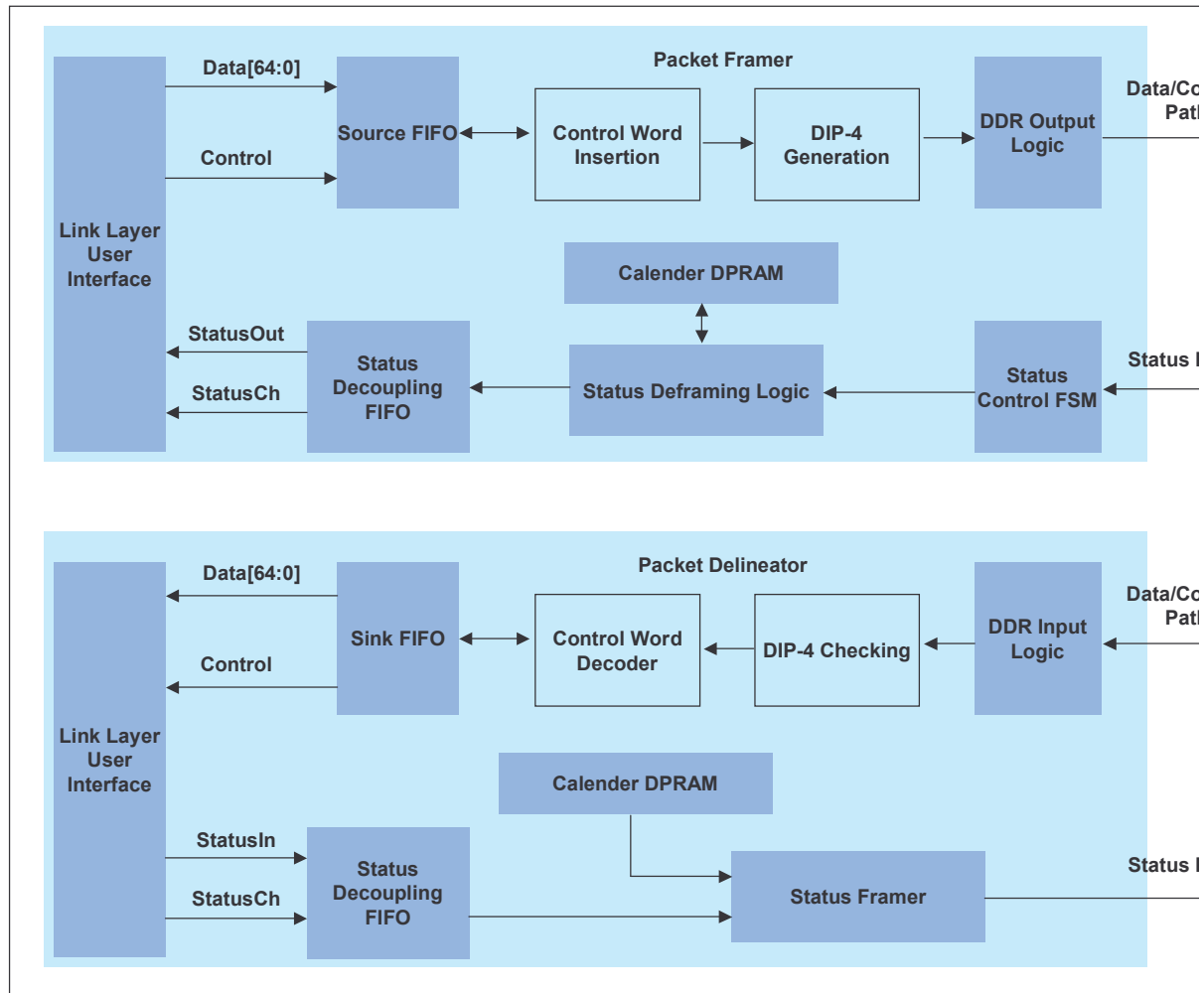
Overview

The SPI 4.2 interface core enables the interconnection of physical layer devices to link layer devices in 10 Gb/s POS, ATM, and Ethernet applications.

Features

- ◆ Compatible with ATM Forum UTOPIA level-4 , POS-PHY level-4 protocol specifications and Custom bus protocol.
- ◆ Complies with OIF-SPI4-02.0 System Packet Interface (SPI-4) Level4 Phase-2 standard
- ◆ Supports OC-192 data rates of 10Gbps
- ◆ Support for single-channel operation
- ◆ Split (Source/Sink) configurations allowing for flexible system transmit and receive architectures
- ◆ Automatic transmission of source data based on FIFO condition
- ◆ Provides user-controlled forced insertion of idle cycles or training sequences, inserted on next credit boundary
- ◆ Internal data path demultiplex to 64bits in order to support the back-end logic
- ◆ DIP-4 and DIP-2 parity generation and checking

Block Diagram



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Benefits

- ◆ Eases Soc integration
- ◆ Configurable for ease of use

Applications

- ◆ Used to connect network processors with OC-192 framers and mappers as well as Gigabit and 10 Gigabit Ethernet data link MACs
- ◆ Suited for line cards in gigabit routers and optical cross connect switches

Deliverables

- ◆ Technical Specification
- ◆ RTL Verilog Synthesisable Code
- ◆ Comprehensive Test Environment
- ◆ Technical Support and Maintenance

About Us

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