

iWPPHIG1 – Parallel Port Host Interface FPGA

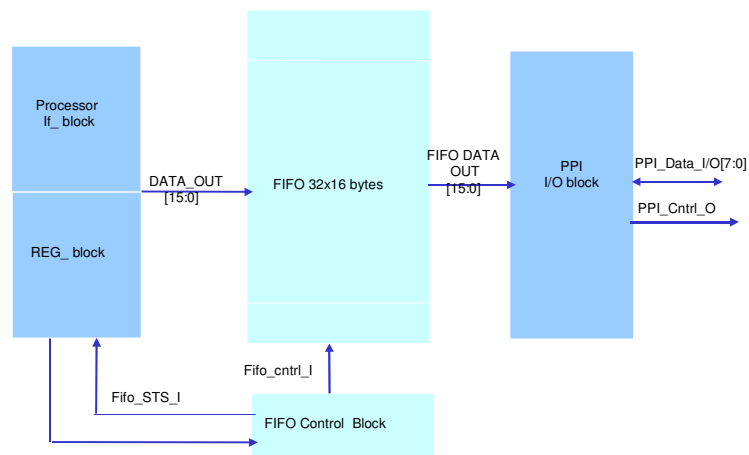
Overview

A parallel Port Interface is provided to download and upload the MP3 data from the PC to MP3 Reference Design Board. The main function of Parallel port interface module is to receive the 8-bit data input from 25-pin connector and store the data in a FIFO. On receiving a block of bytes a DMA Request (Channel 0) is initiated to the processor, which is then stored in the On-board SDRAM memory.

Features

- ◆ Synchronous Design
- ◆ Synthesizable RTL Code
- ◆ Well-Commented code for clarity
- ◆ Approximately 17429 (FPGA) Gates
- ◆ Available in Verilog
- ◆ Functional Partitioning
- ◆ Designed by Hardware Engineers for Hardware Engineers
- ◆ The maximum data transfer can be achieved is 5Mbps
- ◆ This core supports the both the upload and download of data from the on board SDRAM to the host system
- ◆ Register set easily expandable

Block Diagram



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Benefits

- ◆ Embedded applications in networking and Telecommunication Systems
- ◆ High speed, high performance peripheral applications

Deliverables

- ◆ Technical Specification
- ◆ RTL Verilog Synthesisable Code
- ◆ Comprehensive Test Environment
- ◆ Constraint Files
- ◆ Technical Support and Maintenance

About Us

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