

Introduction

iWave Systems has introduced an IP Core for x86 processor, which operates at 33MHz with the slowest Spartan-3 device. It is the first product, which helps to reduce system development time giving a high reliability general-purpose microprocessor. It is compatible with compilers like Lattice C Compiler for DOS & OS/2 version 4.11. This FPGA IP core is an ideal platform and excellent choice for industries using 80186/80188 processors and a perfect alternative for the similar obsolete processors from manufacturers such as Intel, NEC and AMD.

Features

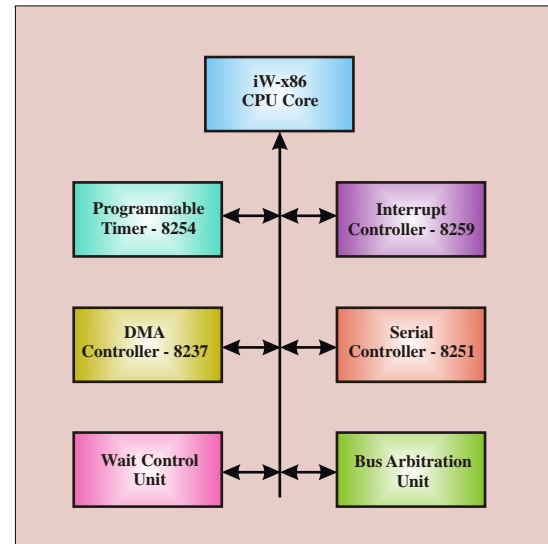
- ✘ Non multiplexed 20-bit address and 16-bit data bus support
- ✘ Arithmetic Logic Unit
- ✘ 1M-byte memory space divided into 4 segments
- ✘ 64 K-byte IO space
- ✘ DMA Controller with 4 channels
- ✘ Programmable Interrupt Controller
- ✘ Serial Controller Unit similar to 8251 with Full duplex double buffer system
- ✘ One 16-bit Timer/Counter operating in 6 different count modes
- ✘ Bus arbitration unit
- ✘ Programmable Wait State generator
- ✘ Clock Generator
- ✘ RTL code in verilog format

Description

The iW-x86 processor is fully binary compatible to the well known 80186 Processor from Intel. This new core is an excellent choice for many embedded controller applications and it provides a cost-effective alternative for replacing x86 processors that are no longer manufactured. This IP core is available as synthesizable circuit description.

Figure-1 shows iW-x86 processor. This core has non-multiplexed 20-bit address bus and 16-bit data bus, which eliminates the need to have address latch enable logic externally and allow easy connection to memory. It supports 16-bit execution unit using familiar x86 instruction set and has 1Mbytes address space. The core incorporates 4-channel DMA controller with two configurable bus modes and 3 transfer modes for efficient data transfers, one programmable interrupt controller compatible with 8259, capable of handling 8 external requesters with the capability of defining priorities and masking at individual levels allowing complex priority schemes. One real time programmable timer compatible with 8254, incorporating three counter/timer channels. It offers wait control unit, which automatically inserts up to 8 wait states in CPU and DMAU bus cycle. It also offers a variable-rate asynchronous serial controller compatible with 8251, which gives RS-232 protocol support and incorporates a baud rate generator selectable as transmitter / receiver clock. The bus arbitration unit performs the arbitration for the internal bus mastership between CPU and DMA with priority.

Figure-1 : iW-x86 Processor Block Diagram



Applications

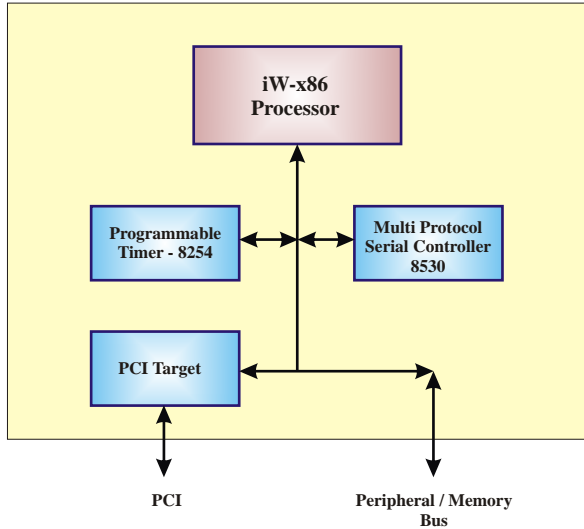
- ✘ Quick migration of 80186 based design to an FPGA platform.
- ✘ Deliver Retrofit of existing systems, maintaining the I/O compatibility.
- ✘ Replacement for 80186 Processor and ASICs.
- ✘ It is an excellent choice for embedded applications, catering for the growing needs of industrial, automotive and communication system solutions.
- ✘ Extensive use has been in medical instruments designed to perform routine clinical measurements (endoscopes, breathing aids...)

Example Application

The design has been optimized for the requirement of a SOC design flow, the block diagram shown in the fig-2 is an example application which includes additional peripherals like PCI Target Controller, programmable timer and Multi Protocol Serial Controller. PCI target controller to manage 32-bit data transfer between the PCI and the user Interface, MPSC which is general purpose communication controller consisting of two sets of bi-directional parallel/serial converter for data communication supporting the character oriented protocol and bit oriented protocol communication features and the Timer/Counter unit identical with the one used in processor. The iW-x86 SOC reduces system size and weight while dramatically reducing the number of components in the system by eliminating the reliance on the component that are or may become obsolete.

This fast-running version raises the high end of our IP product line, improves the reliability and ensures the long-term availability and tremendous support.

Figure-2 : iW-x86 SOC Block Diagram



Case Study

How we helped our customer to migrate from a legacy platform to iW-x86 core based FPGA platform

Background: No software source code for the legacy platform was available and the ASIC with proprietary libraries, which is not supported and legacy platform had obsolete peripherals

The old board had an 80186 processor with one ASIC, one Multi Protocol Serial Communication Controller, PCI Target controller and FIFO SRAMs. iWave made it possible for the customer to migrate from 80186 based design to an FPGA Platform by maintaining the IO compatibility and met the full set of functional and performance requirement. The protocol application testing for the core is performed for 10 different legacy protocol firmware support and found all the 10 applications working in the new platform successfully without any complication.

Device Utilization Summary

Processor

IP	Xilinx Device	Fmax (MHz)	Slices	4 input LUTs	Gate count	IOB	GCLK	BRAM	MULT / DSP48	DCM	Power (mW)	Design Tool
x86 Processor	XC3S1500	40	6823 (51%)	11542 (43%)	125833	115 (35%)	3 (100%)	0	2 (6%)	0	519	ISE 9.2.03i

Individual Cores

IP	Xilinx Device	Slices	4 input LUTs	BRAM	MULT/ DSP48	DCM	Design Tool
CPU core	XC3S1500	3982 (33%)	7203 (27%)	0	2 (6%)	0	ISE 9.2.03i
8254 equivalent timer	XC3S1500	340 (3%)	517 (2%)	0	0	0	ISE 9.2.03i
8259 equivalent interrupt controller	XC3S1500	296 (2%)	456 (2%)	0	0	0	ISE 9.2.03i
8237 equivalent DMA controller	XC3S1500	1719 (13%)	2730 (10%)	0	0	0	ISE 9.2.03i
8251 equivalent serial controller	XC3S1500	121 (1%)	187 (1%)	0	0	0	ISE 9.2.03i
Miscellaneous Peripherals	XC3S1500	365 (3%)	449 (2%)	0	0	0	ISE 9.2.03i

Additional Peripherals

IP	Example Device	Slices	4 input LUTs	BRAM	MULT/DSP48	DCM	Design Tool
8530 equivalent Multi protocol serial controller	XC3S1500	3364 (25%)	5381 (20%)	0	0	0	ISE 9.2.03i
PCI target controller	XC3S1500	125 (1%)	155 (1%)	0	0	0	ISE 9.2.03i

Verification Methods

Verification considerations are a fundamental constraint on the design process. Rigorous code coverage has been done for this IP core. The code has been verified through extensive simulation to cover the processor design corners. Around 10,000 test cases have been run to confirm that the IP core meets functional and timing requirements. We have also bundled all the test vectors and test benches so that the customer can verify that the required functionality is available in the core.

It has also been compared with its counterpart 80C186 in same hardware modeling environment and verified to be good.

Conclusion

iWave systems offers x86 processor which is ideal for applications that have traditionally used the 16-bit 80186 processor, as it is fully software compatible with the x86 standard, offering a solution to problems of processor obsolesces. iW-x86 SOC is designed to deliver a competitive advantage in terms of productivity and time to market. Solutions based on the iW-x86 core are customizable according to customer applications and needs. Also we have developed a 16-bit microprocessor, which is compatible with Intel 80188EB microprocessor. iWave systems's customers have a confidence that their use of our commercial IP will be one of their best investment decision.

About iWave Systems

iWave Systems Technologies is an embedded Hardware and Software Turnkey Design Services company, focused on providing integrated solutions for developing innovative products and systems in the areas of Communication, Consumer electronics and Multimedia. iWave offers complete turnkey solutions for systems engineering and product development.